HT32L62141
Datasheet

32-Bit Arm® Cortex®-M0+ Smoke Detector Microcontroller, 64 KB Flash and 8 KB SRAM with Smoke Detector, Buzzer Driver, 1 Msps ADC, PDMA, DIV, USART, UART, SPI, I²C, MCTM, GPTM, SCTM, BFTM, CRC, UID, RTC and WDT

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1 General Description

The Holtek HT32L62141 device is high performance, ultra-low power consumption 32-bit microcontroller based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer and including advanced debug support.

The device operates at a frequency of up to 48 MHz with a Flash accelerator to obtain maximum efficiency. It provides 64 KB of embedded Flash memory for code / data storage and 8 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as PDMA, Hardware Divider DIV, ADC, I²C, USART, UART, SPI, MCTM, GPTM, SCTM, BFTM, CRC-16/32, 96-bit Unique ID, RTC, WDT and SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in ultra-low power applications.

The device integrates a smoke detector and a buzzer driver with boost. The smoke detector incorporates a smoke detector AFE and two programmable constant current channels. It communicates via one-wire interface. The driver consists of a buzzer driver with boost and a buzzer watchdog timer (BWDT). The buzzer driver can drive either an external-drive 2-pin buzzer or a self-driving 3-pin buzzer. The boost provides power to driver the buzzer driver and supports the MCU failure alarm function.

The above features ensure that the device is suitable for use in the smoke detector applications.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 48 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets, single-cycle I/O ports, hardware multiplier and low latency interrupt respond time.

On-Chip Memory

- 64 KB on-chip Flash memory for instruction/data and option byte storage
- 8 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor access and debug access share the single external interface to external AHB peripherals. The processor access takes priority over debug access. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 in the Overview chapter shows the memory map of the device, including code, SRAM, peripheral and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and a cache buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a cache buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor
  - Power On Reset / Power Down Reset – POR / PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- External 32,768 Hz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ± 1 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock pre-scaler, clock multiplexers, APB clock divider and gating circuitry. The clocks of the AHB, APB and Cortex®-M0+ are derived from the system clock (CK_SYS) which can source from the HSI, HSE, LSI, LSE or system PLL. The Watchdog Timer and Real-Time Clock (RTC) use either the LSI or LSE as their clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 2.2 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- V_{DD} power supply for RTC
- V_{DD} and V_{CORE} power domains
- Six power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Deep-Sleep3, Power-Down, Deep Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2, Deep-Sleep3, Power-Down and Deep Power-Down modes. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Smoke Detector – SD

- Smoke detector AFE including two OPAs
- Dual-channel sink current generator for constant current output
- One-wire communication interface

The integrated programmable sink current generator and smoke detector AFE can implement smoke detection function without connecting the external components. The sink current range is adjustable within two ranges: 20 mA ~ 275 mA and 50 mA ~ 305 mA with 1 mA/step. The relevant parameters can be configured by the one-wire communication interface.

Buzzer Driver – BD

- Integrated 2-pin and 3-pin buzzer drivers
- Integrated a boost converter
- Buzzer watchdog timer (BWDT) for MCU failure alarm function

The buzzer driver can drive either an external-driving 2-pin buzzer or a self-driving 3-pin buzzer, depending on the mode pin setting and the boost provides power to driver the buzzer driver. In normal operation, the MCU repeatedly toggles the WDI pin within t_{WDI} to reset the BWDT counter. if MCU fails to toggle the WDI pin, a timeout occures, and the buzzer driver activates and alarms.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger sources and types
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge or both edges
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 8 external analog input channels
- Build-in reference voltage (V_{REF}) for internal analog input channel
- External reference voltage input possibility
- Conversion range: $V_{REF+} \sim V_{SSA}$

A 12-bit multi-channel Analog to Digital Converter is integrated in the devices. There are multiplexed channels, which include up to 8 external analog signal channels and 4 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset thresholds. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

The internal voltage reference (V_{REF}) which can provide a stable reference voltage for the A/D Converter is internally connected to the ADC input channel. The precise voltage of the V_{REF} is individually measured for each part by Holtek during production test.

I/O Ports – GPIO

- Up to 30 GPIOs
- Port A, B, C are mapped to 16-line EXTI interrupts
- Almost all I/O pins have configurable output driving current
- Almost all I/O pins are 5 V-tolerant except for pins shared with analog inputs

There are up to 30 General Purpose I/O pins, GPIO, for the implementation of logic input / output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

Motor Control Timer – MCTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels

- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Supports 3-phase motor control and hall sensor interface
- Break input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer Module, MCTM, consists of a single 16-bit up/down counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR), 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module, GPTM, consists of one 16-bit up/down-counter, four 16-bit Capture / Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control / status registers. It can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation or PWM output generation. The GPTM supports an Encoder Interface using a quadrature decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit auto-reload up-counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single Channel Timer Module, SCTM, consists of one 16-bit up-counter, one 16-bit Capture / Compare Register (CCR), one 16-bit Counter Reload Register (CRR) and several control / status registers. They can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as PWM output.

Basic Function Timer – BFTM

- 32-bit compare match count-up counter - no I/O control
- One shot mode - counter stops counting when compare match occurs
- Repetitive mode - counter restarts when compare match occurs

The Basic Function Timer Module, BFTM, is a simple 32-bit up-counting counter designed to measure time intervals, generate one shots or generate repetitive interrupts. The BFTM can operate in two functional modes which are repetitive and one shot modes. In the repetitive mode, the counter will be restarted at each compare match event. The BFTM also supports a one shot mode which will force the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Provides reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuitry that can be used to detect a system lock-up due to software trapped in a deadlock. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter before it reaches a delta value. It means that the counter reload must occur when the Watchdog timer value has a value within a limited window using a specific method. The Watchdog Timer counter can be stopped when the processor is in the debug mode. The register write protection function can be enabled to prevent an unexpected change in the Watchdog timer configuration.

Real-Time Clock – RTC

- 24-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real-Time Clock, RTC, includes an APB interface, a 24-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the V_{DD} power domain except for the APB interface. The APB interface is located in the V_{CORE} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{CORE} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode using address mask function

The I²C is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bidirectional data line between the master and slave devices and is used for data transmission and reception. The I²C also has an arbitration detection and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave modes. The SPI interface uses 4 pins, among which are serial data input and output lines MISO and MOSI, the clock line SCK, and the slave select line SEL. One SPI device acts as a master who controls the data flow using the SEL and SCK signals to indicate the start of the data communication and the data sampling rate. To receive the data bits, the streamlined data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but with the reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to (f_{PCLK}/16) MHz for asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Supports LIN (Local Interconnect Network) mode
- Supports single-wire mode
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes an 8-level transmitter FIFO, (TX_FIFO) and an 8-level receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of the transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to f_{PCLK}/16 MHz
- Full duplex communication
- Supports LIN (Local Interconnect Network) mode
- Supports single-wire mode
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8 or 9-bit character
  - Parity: Even, odd or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bits generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun, and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Cyclic Redundancy Check – CRC

- Supports CRC16 polynomial: 0x8005,
  $X^{16}+X^{15}+X^{2}+1$
- Supports CCITT CRC16 polynomial: 0x1021,
  $X^{16}+X^{12}+X^{5}+1$
- Supports IEEE-802.3 CRC32 polynomial: 0x04C11DB7,
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^{8}+X^{7}+X^{5}+X^{4}+X^{2}+X+1$
- Supports 1's complement, byte reverse & bit reverse operation on data and checksum
- Supports byte, half-word & word data size
- Programmable CRC initial seed value
- CRC computation executed in 1 AHB clock cycle for 8-bit data and 4 AHB clock cycles for 32-bit data
- Supports PDMA to complete a CRC computation of a block of memory

The CRC calculation unit is an error detection technique test algorithm which is used to verify data transmission or storage data correctness. A CRC calculation takes a data stream or a block of data as its input and generates a 16- or 32-bit output remainder. Ordinarily, a data stream is suffixed by a CRC code and used as a checksum when being sent or stored. Therefore, the received or restored data stream is calculated by the same generator polynomial as described above. If the new CRC code result does not match the one calculated earlier, that means the data stream contains a data error.

Peripheral Direct Memory Access – PDMA

- 6 channels with trigger source grouping
- 8-bit, 16-bit and 32-bit width data transfer
- Supports linear address, circular address and fixed address modes
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger sources:
  ADC, SPI, USART, UART, I^2C, MCTM, GPTM and software request

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to connect each data movement operation.

Hardware Divider – DIV

- Signed / unsigned 32-bit divider
- Calculate in 8 clock cycles, load in 1 clock cycle
- Division by zero error Flag

The divider is the truncated division and requires a software triggered start signal by controlling register the “START” bit in the control register. The divider calculation complete flag will be set to 1 after 8 clock cycles, however, if the divisor register data is zero during the calculation, the division by zero error flag will be set to 1.

Unique Identifier – UID

- Total 96-bit UID is unique and not duplicate with other HT32 MCU devices
- It is unchangeable and determined by MCU manufacturer

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watch points

Package and Operation Temperature

- 64-pin LQFP package
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32L62141
Main Flash (KB)		63
Option Bytes Flash (KB)		1
SRAM (KB)		8
Timers	MCTM	1
	GPTM	1
	SCTM	2
	BFTM	2
	RTC	1
	WDT	1
Communication	SPI	2
	USART	1
	UART	2
	I²C	2
Hardware Divider		1
PDMA		6 Channels
CRC-16/32		1
EXTI		16
12-bit ADC		1
Number of channels		8 External Channels
Smoke Detector Controller		1
Buzzer Driver		1
GPIO		Up to 30
CPU frequency		Up to 48 MHz
Operating voltage		2.2 V ~ 3.6 V
Operating temperature		-40 °C ~ 85 °C
Package		64-pin LQFP

Note: The functions listed here, except the Smoke Detector and Buzzer Driver, are compatible with the HT32L52241 device. Refer to the HT32L52231/HT32L52241 user manual for detailed functional description.

Block Diagram

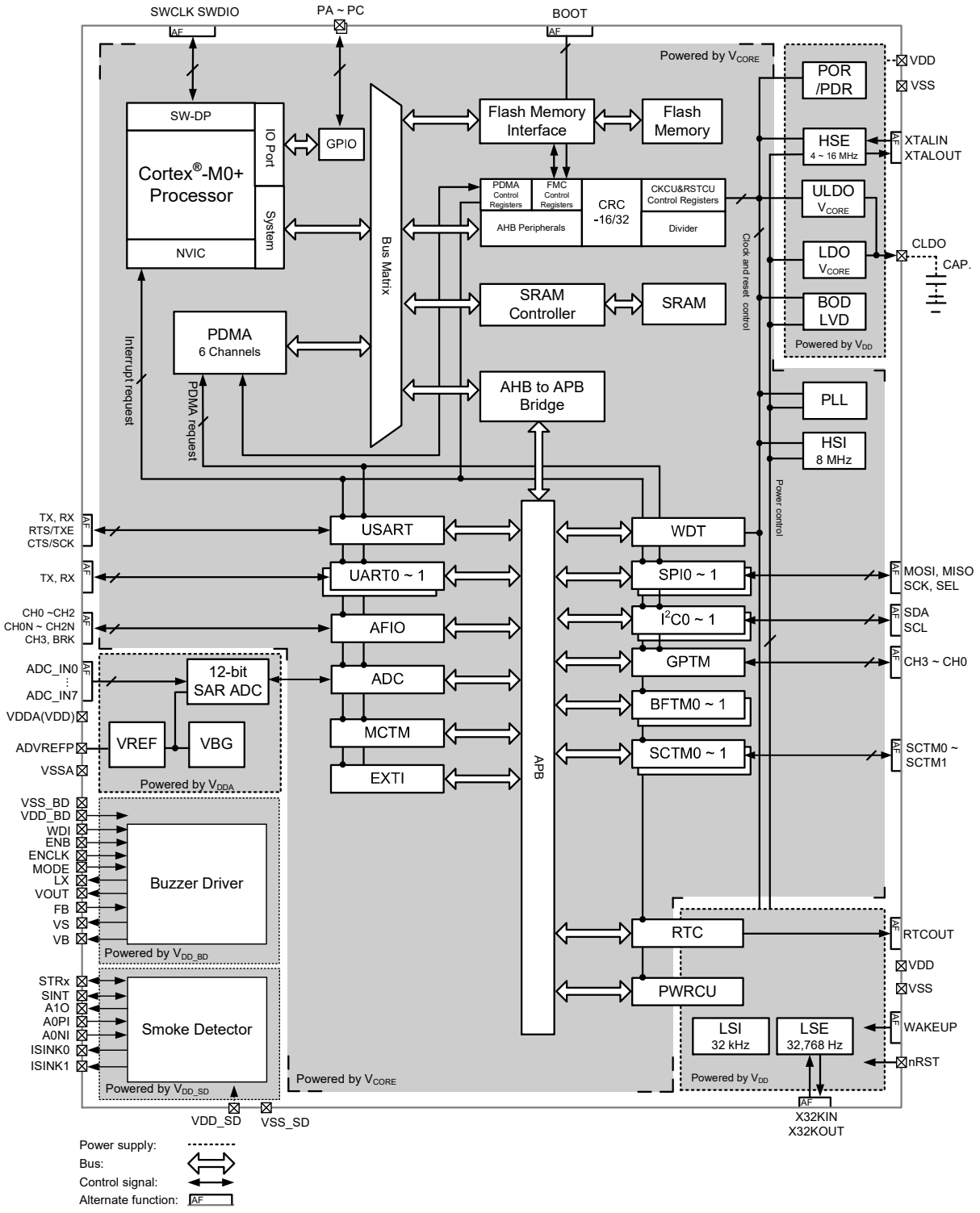


Figure 1. Block Diagram

Memory Map

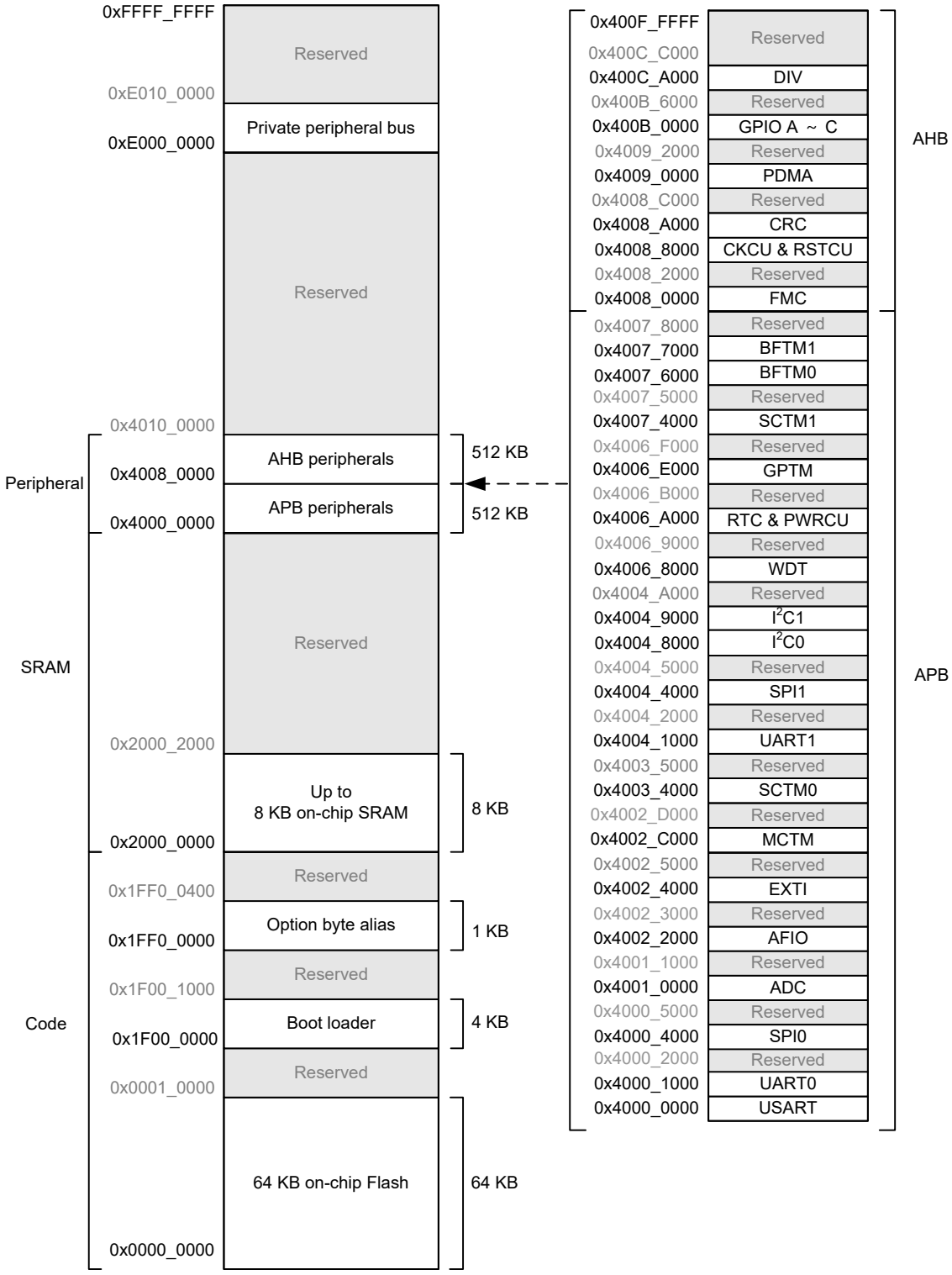


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART0	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI0	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4002_BFFF	Reserved	
0x4002_C000	0x4002_CFFF	MCTM	
0x4002_D000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_0FFF	Reserved	
0x4004_1000	0x4004_1FFF	UART1	
0x4004_2000	0x4004_3FFF	Reserved	
0x4004_4000	0x4004_4FFF	SPI1	
0x4004_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C0	
0x4004_9000	0x4004_9FFF	I^2C1	
0x4004_A000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	RTC & PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM0	
0x4007_7000	0x4007_7FFF	BFTM1	
0x4007_8000	0x4007_FFFF	Reserved	

Start Address	End Address	Peripheral	Bus
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x4008_BFFF	CRC	
0x4008_C000	0x4008_FFFF	Reserved	
0x4009_0000	0x4009_1FFF	PDMA	
0x4009_2000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIO A	
0x400B_2000	0x400B_3FFF	GPIO B	
0x400B_4000	0x400B_5FFF	GPIO C	
0x400B_6000	0x400C_9FFF	Reserved	
0x400C_A000	0x400C_BFFF	DIV	
0x400C_C000	0x400F_FFFF	Reserved	

Clock Structure

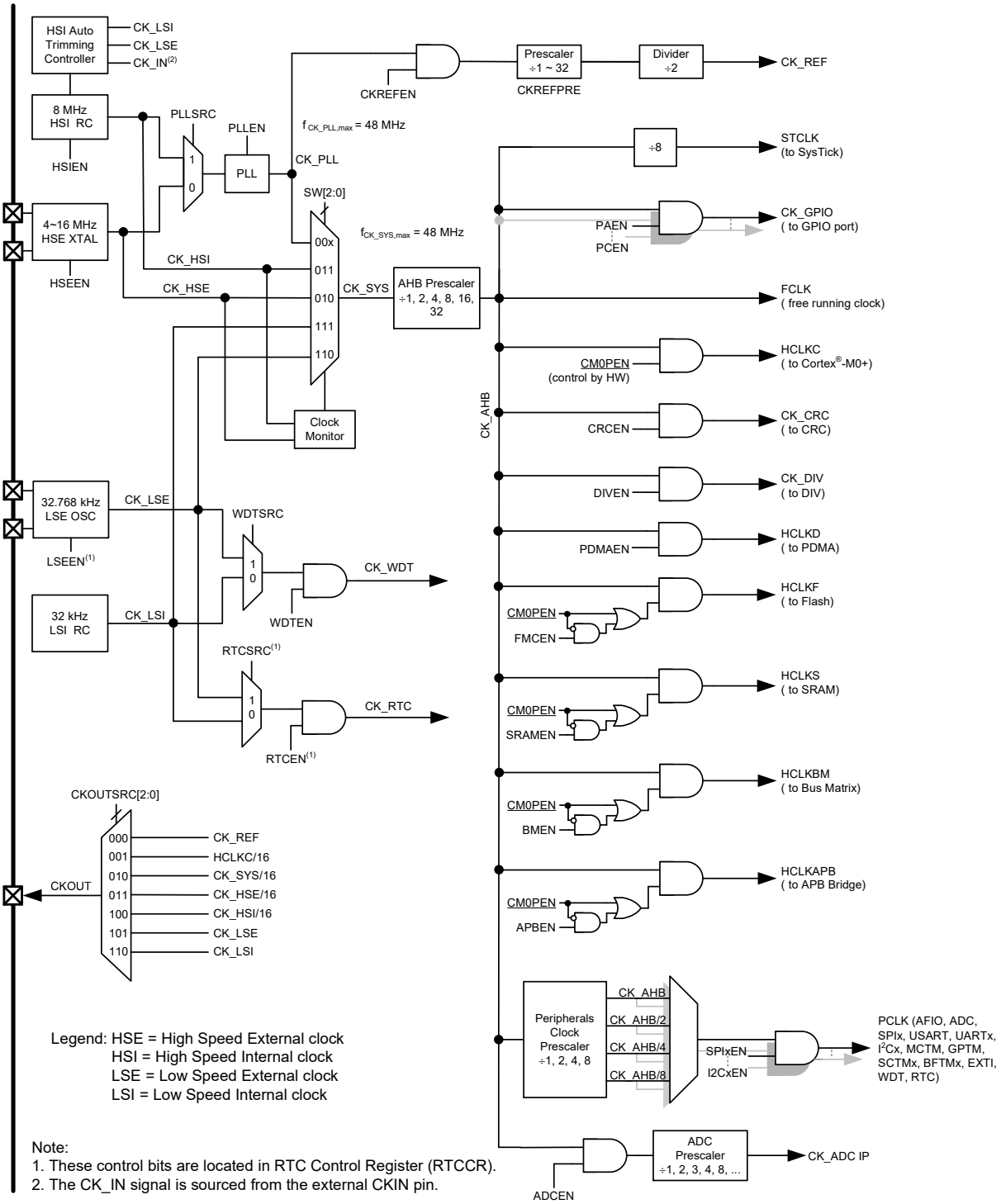


Figure 3. Clock Structure

4 Smoke Detector – SD

The smoke detector includes a smoke detector AFE, a sink current generator and one-wire interface.

The smoke Detector AFE which can be used for optical signal detection in Smoke Detector applications. The circuit consists of two fully integrated Operational Amplifiers. The optical signal can be detected and processed by the operational amplifiers.

The sink current generator could provide constant current no matter what the V_{ISINK} voltage is from 0.7 V to 4.5 V and the V_{DD_SD} voltage is from 2.2 V to 3.6 V. The constant current value is controlled by the ISGDATA0/ISGDATA1 register, and the sink current range is 50 mA ~ 305 mA and 20 mA ~ 275 mA with 1 mA/steps and 8-bit resolution.

Users can implement the smoke detection function through the one-wire interface. This simplifies and expedites smoke detector product development.

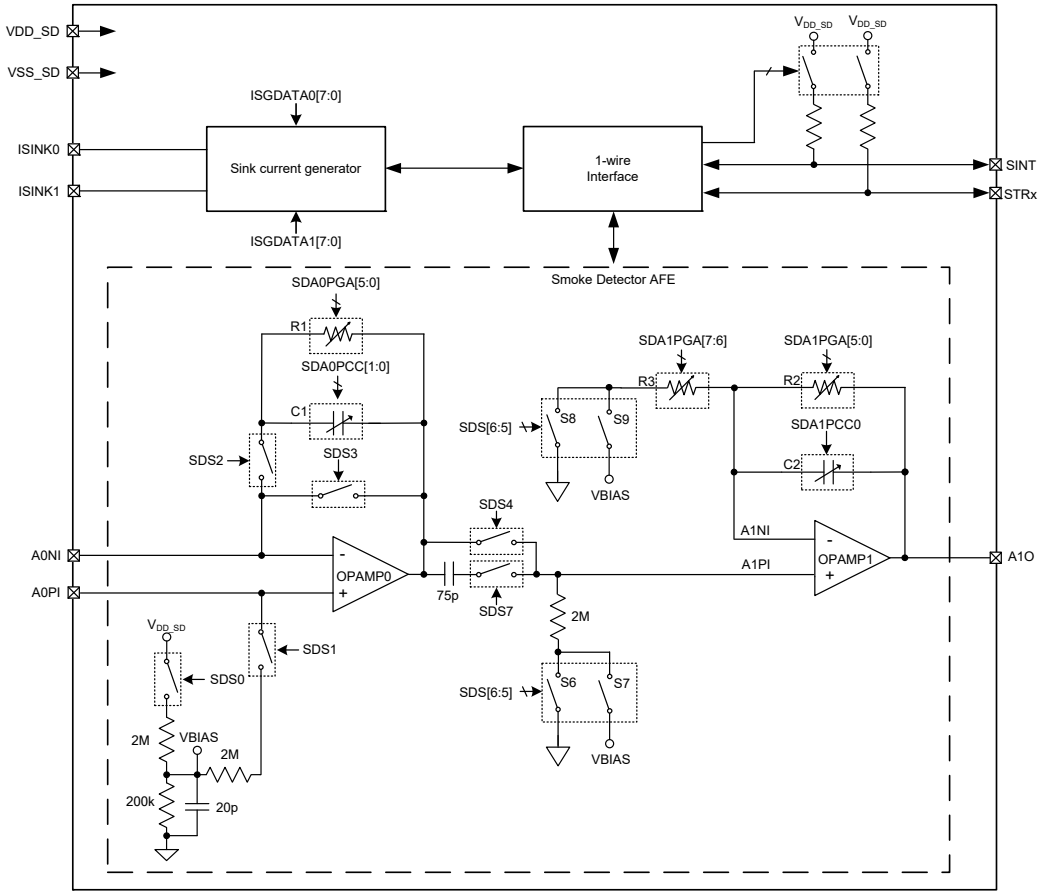


Figure 4. Smoke Detector Diagram

Note that although the SD OPAn bandwidth is determined by the SDAnBW1 ~ SDAnBW0 (n=0,1) bits there are some limitations when using the OPAn together with the A/D converter. As the OPAn bandwidth will result in a small current output, care must be taken for SD OPAn bandwidths.

SD OPAn BW	Max. ADC Clock (kHz)	SD OPAn BW	Max. ADC Clock (kHz)
SDAnBW[1:0]=00	15.625	SDAnBW[1:0]=10	2000
SDAnBW[1:0]=01	125	SDAnBW[1:0]=11	2000

Smoke Detector Interface

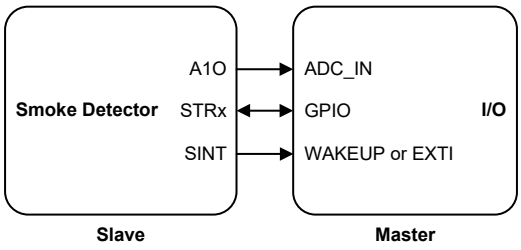


Figure 5. Smoke Detector Connection

The smoke detector connection is shown in the figure above. The A1O pin is the smoke detector AFE output, which can be connected to any A/D analog input pin. The STRx pin is the one-wire communication pin, which can be connected to any general purpose I/O port without interrupt requirement. The SINT pin is used to generate a wake-up signal, which should be connected to any WAKUP or EXTI line.

The SINT pin is valid only when the smoke detection period or time base wake-up period is larger than 0. If the period is set to 0, it is disabled, refer to the "Parameter Configuration" for details. The smoke detection period and the time base wake-up period which allow to be set with different values, are distinguished by the STRx pulse, SINT pulse and their respective low level duration. The wake-up pulse width is fixed at 15μs and the wake-up duration can be modified by relevant running variables. The wake-up signal for each case are as follows:

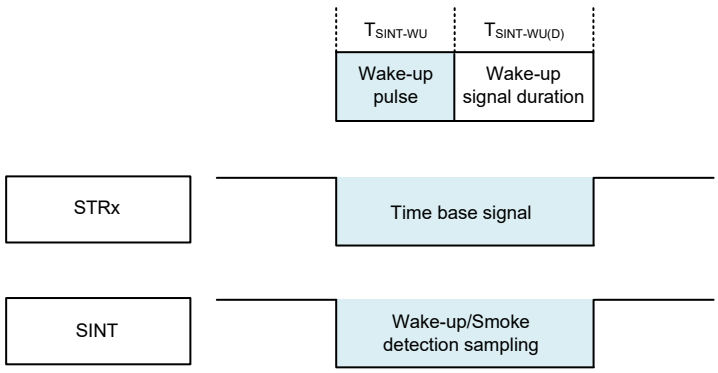


Figure 6. Smoke Detection Wake-up and Time Base Wake-up

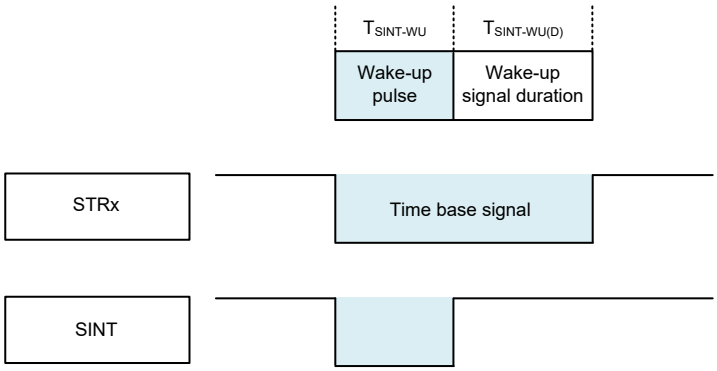


Figure 7. Time Base Wake-up

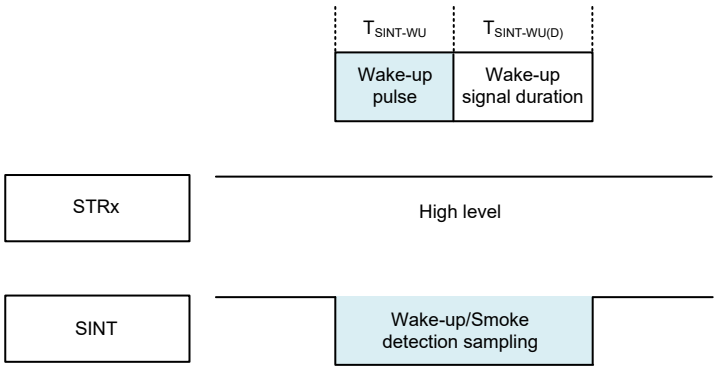


Figure 8. Smoke Detection Wake-up

Generally, after the smoke detection period is configured, the smoke detector will trigger the wake-up/synchronous sampling timing periodically, notifying the device to perform an interrupt sampling (passive). To enable active trigger sampling, the device can send a low pulse with a width greater than 40 μs to the STRx pin. This actively triggers the configured smoke sampling timing without waiting for the detection period to start. Too small a pulse width will be recognized as a one-wire communication request, refer to the “One-wire Communication Protocol”.

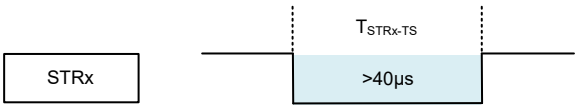


Figure 9. Active Trigger Sampling

Wake-up / Synchronous Sampling Timing – Method A

The smoke detection generally works in pulse mode with low power consumption. There are strict timing requirements for the AFE operation and ISINK emission, otherwise it will cause additional power consumption. In addition to the wake-up function, the SINT pin also has a synchronisation function. If the channels A and B are enabled using relevant running variables and the detection period setting is larger than 0, the SINT pin will generate sampling pulses with a pulse width of 15 μs after executing the wake-up function to notify the A/D converter to perform sampling. Each channel has two sampling pulses, corresponding to the A1O output in the ISINK off state and the A1O output in the ISINK on state. The specific time can be modified by the relevant running variables. The following is the timing when both channels A and B are enabled.

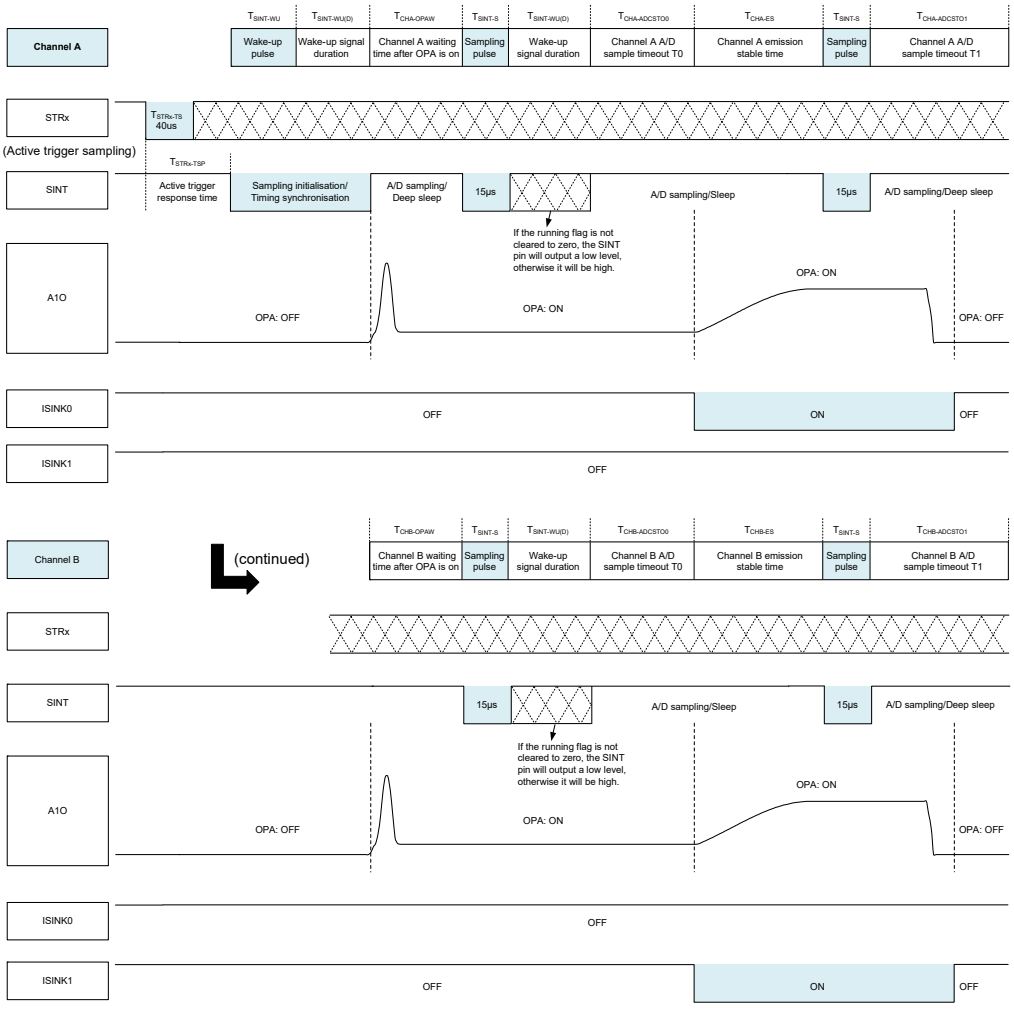


Figure 10. Wake-up / Synchronous Sampling Timing – Method A

Note: 1. It is necessary to enable the channel A and channel B using the running variables and set the smoke detection period to be larger than 0 to generate a synchronous pulse. Refer to the parameter configuration section for details.

2. If only one of channel A and B is enabled, there is only one channel timing.

3. The STRx timing is not required for non-active trigger sampling. The smoke detection period setting is greater than 0.

Wake-up / Synchronous Sampling Timing – Method B

There is an additional ISINK early shutdown function for the method B to avoid unnecessary power consumption, such as delay waiting. During the ISINK emission, after the smoke detector has sent the sampling pulse, the SINT pin will remain pulled high. At this time, if the A/D sampling has been completed, send a control low pulse via the SINT pin, the ISINK can be turned off in advance without waiting until the A/D sampling timeout ends. If no such low pulse is sent, it is method A. Note that the A/D sampling time (SINT high level width) should not be less than 5 μs and the control low pulse width should not be less than 5 μs, otherwise they will not be recognized. The following is the timing when both channels A and B are enabled.

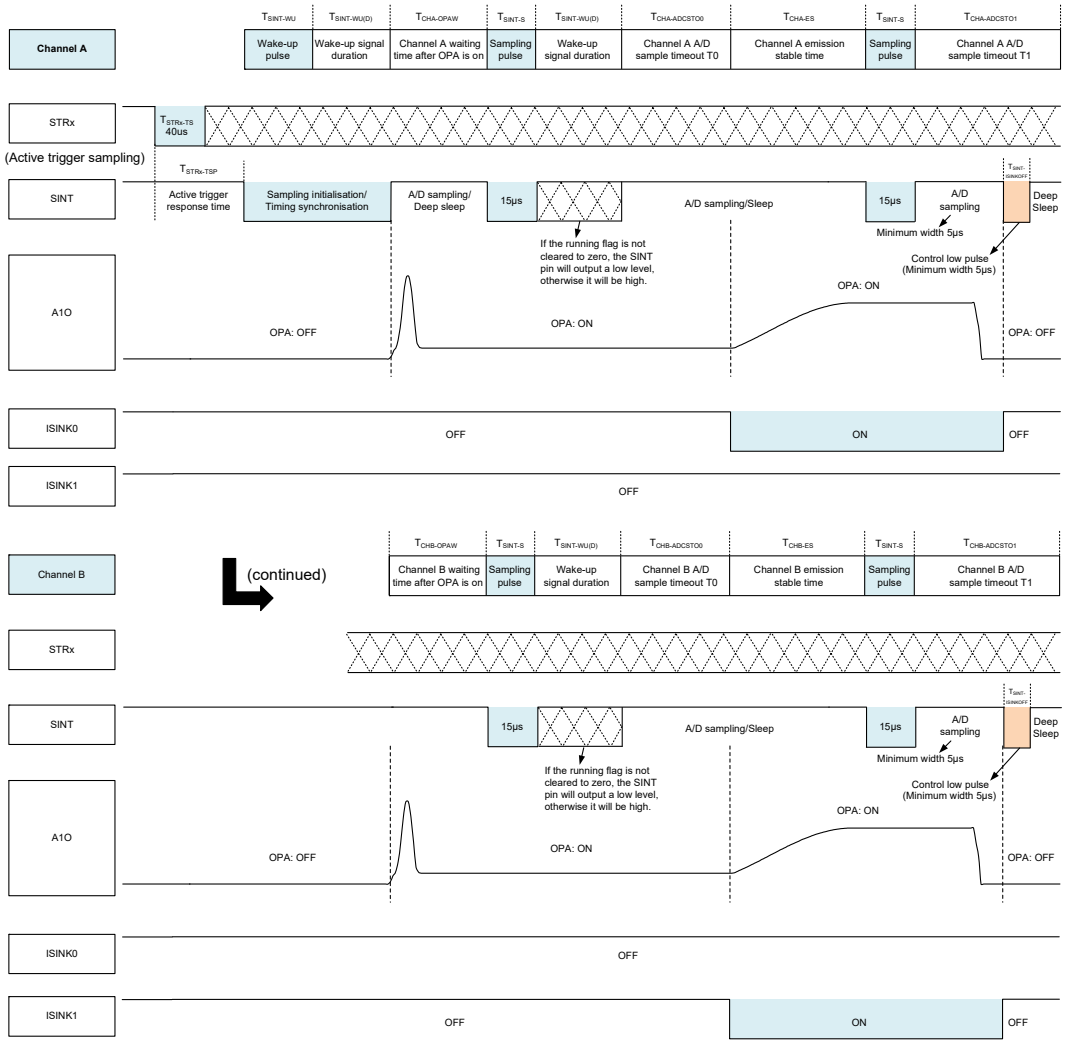


Figure 11. Wake-up / Synchronous Sampling Timing – Method B

Note: 1. It is necessary to enable the channel A and channel B using the running variables and set the smoke detection period to be larger than 0 to generate a synchronous pulse. Refer to the parameter configuration section for details.

2. If only one of channel A and B is enabled, there is only one channel timing.

3. The STRx timing is not required for non-active trigger sampling. The smoke detection period setting is greater than 0.

One-wire Communication Protocol

The one-wire communication can only be initiated by the master. A complete communication process includes a request signal, a request response signal, a data start signal, data 0, data 1, a parity bit (even parity) and a last bit response. The parity bit is data 0 or 1. Note that if the initial low level time is larger than 40 μs, it is an active trigger sampling rather than a communication request. The request response signal is used to determine whether the slave is online and the last bit response is determined by the salve after verifying the previous data, by which the master can know whether the slave has received the data correctly, the master can consider retransmission if there is an abnormality.

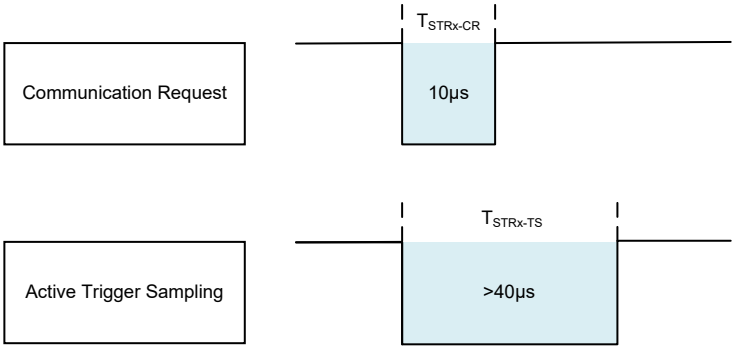


Figure 12. Communication Request and Active Trigger Sampling

Note: If the initial low level time is larger than 40 μs, it is an active trigger sampling timing rather than an one-wire communication request.

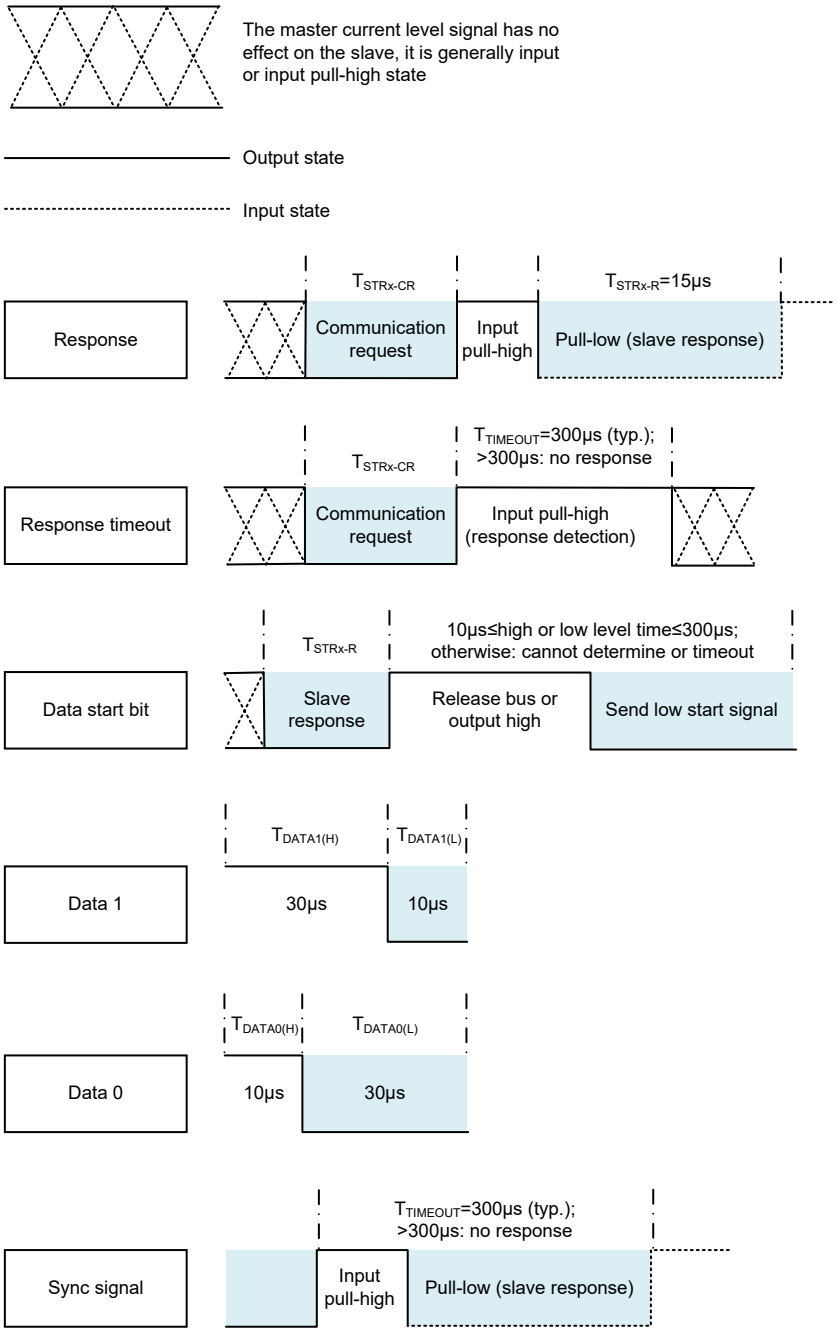


Figure 13. One-wire Communication Protocol

Data Frame

The order of data transmission is the LSB first. The bit 7, which is the MSB of the address byte, is used to distinguish the read or write instruction. When this bit is 0, it indicates a send instruction; when this bit is 0, it indicates a receive instruction. The parity bit is the even parity of the address byte and data byte. If the address byte is 0x01 and the data byte is 0x77, the parity bit is 1.

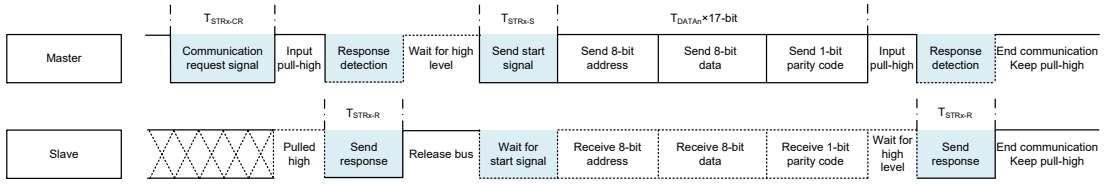


Figure 14. Send One Frame of Data

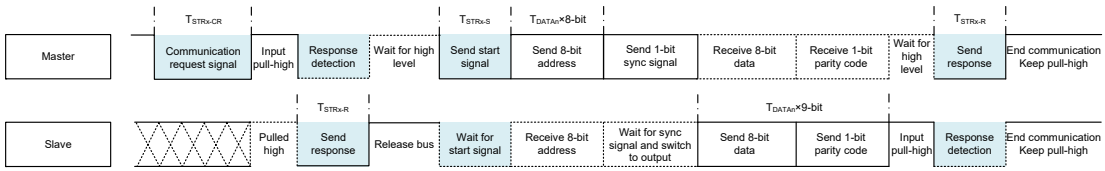


Figure 15. Receive One Frame of Data

Parameter Configuration

The smoke detector has two channels, A and B. Channel A employs ISINK0 for smoke detection, while channel B employs ISINK1. The AFE parameters and emission current of each channel are independent. After the master has configured the corresponding parameters and enabled the channel, it does not need to execute communicate processing again. The smoke detector will automatically send out a wake-up signal, configure AFE, turn on ISINK with the set parameters and then enter low-power standby mode. This mode can effectively avoid frequent communication from the master and therefore reduce standby power consumption. The specific operation timing are shown in the above section. The following data are all 8-bit wide.

Table 3. Running Variable Mode Parameter Configuration List

Function	Address	Type	Initial Value	Description
Write protection	0x1A	R/W	0x00	A value of 0xA5 should be written to this address to write to the running variable. If the write value is any value other than 0xA5, writing to the variable is prohibited.
Wake-up signal duration (low level)	0x00	R/W	0x00	$T_{SINT\text{-}WU(D)}$ = (1.5 + 1.5 N) × 4 μs. When it is 0x00, N = 255.
Channel A SDSW0	0x01	R/W	0x00	Refer to the Smoke Detector SDSW0 register.
Channel A SDSW1	0x1B	R/W	0x00	Refer to the Smoke Detector SDSW1 register.
Channel A SDPGAC0	0x02	R/W	0x00	Refer to the Smoke Detector SDPGAC0 register.
Channel A SDPGAC1	0x03	R/W	0x00	Refer to the Smoke Detector SDPGAC1 register.
Channel A ISGDATA0 (emission current)	0x04	R/W	0x00	Refer to the Smoke Detector ISGDATA0 register.
Channel A waiting time after OPA is on	0x05	R/W	0x00	$T_{CHA\text{-}OPAW}$ = (1.5 + 1.5 N) × 4 μs. When it is 0x00, N = 255.
Channel A emission stable time	0x06	R/W	0x00	$T_{CHA\text{-}ES}$ = (1.5 + 1.5 N) × 2 μs. When it is 0x00, N = 255.
Channel A A/D sample timeout time	0x07	R/W	0x00	T0: $T_{CHA\text{-}ADCSTO0}$ = (1.5 + 1.5N) μs. When it is 0x00, N = 255. T1: $T_{CHA\text{-}ADCSTO1}$ = (2.5 + 2.5N) μs. When it is 0x00, N = 255.
Channel B SDSW0	0x08	R/W	0x00	Refer to the Smoke Detector SDSW0 register.
Channel B SDSW1	0x1C	R/W	0x00	Refer to the Smoke Detector SDSW1 register.
Channel B SDPGAC0	0x09	R/W	0x00	Refer to the Smoke Detector SDPGAC0 register.
Channel B SDPGAC1	0x0A	R/W	0x00	Refer to the Smoke Detector SDPGAC1 register.
Channel B ISGDATA1 (emission current)	0x0B	R/W	0x00	Refer to the Smoke Detector ISGDATA1 register.
Channel B waiting time after OPA is on	0x0C	R/W	0x00	$T_{CHB\text{-}OPAW}$ = (1.5 + 1.5N) × 4 μs. When it is 0x00, N = 255.
Channel B emission stable time	0x0D	R/W	0x00	$T_{CHB\text{-}ES}$ = (1.5 + 1.5N) × 2 μs. When it is 0x00, N = 255.
Channel B A/D sample timeout time	0x0E	R/W	0x00	T0: $T_{CHB\text{-}ADCSTO0}$ = (1.5 + 1.5N) μs. When it is 0x00, N = 255. T1: $T_{CHB\text{-}ADCSTO1}$ = (2.5 + 2.5N) μs. When it is 0x00, N = 255.
Channel A enable	0x0F	R/W	0x00	When it is 0x00, channel A is disabled. When it is larger than 0, channel A is enabled.
Channel B enable	0x10	R/W	0x00	When it is 0x00, channel B is disabled. When it is larger than 0, channel B is enabled.
Smoke detection period	0x11	R/W	0x00	T_{SD} = N, Unit: s. When it is 0x00, it is disabled.
Time base wake-up period	0x12	R/W	0x00	T_{TB} = N, Unit: s. When it is 0x00, it is disabled.
Running flag	0x1D	R/W	0xBA	After power on, it defaults to 0xBA and needs to be cleared to zero by writing to 0x00. If the flag is not 0x00, the wake-up pin will output a low level during the wake-up signal of the sampling sequence, otherwise it will be high. It indicates whether the operating state is normal. Refer to the Wake-up / Synchronous Sampling Timing for details. During the normal operation, the flag remains at the last value written.

Function	Address	Type	Initial Value	Description
OPA calibration	0x1E	R/W	0x00	Write a 0xA0 value to trigger the OPA calibration, with a calibration end value of 0x55. The OPA does not respond to communication during calibration, the calibration takes about 300ms.
SDA0VOS	0x5D	R/W	XX	Refer to the Smoke Detector SDA0VOS register.
SDA1VOS	0x5F	R/W	XX	Refer to the Smoke Detector SDA1VOS register.

Note: For active trigger sampling, setting the smoke detection period and time base wake-up period to 0x00 prevents conflicts between the wake-up and active trigger sampling signals, ensuring proper smoke detector operation.

Smoke Detector Registers

The overall operation of the smoke detector AFE circuit is controlled using a series of registers. The SDSW0 register is used to control the switches on or off thus controlling the Operational Amplifier operating mode. The SDSW1 register is used to select the SD OPA0 and OPA1 compensation capacitance values. The SDPGAC0 and SDPGAC1 registers are used to select the R1, R2 and R3 resistance. The SDAnC register where n = 0 ~ 1, is used to control the SD OPAn enable / disable and bandwidth functions. The SDAnVOS register is used to select and control the SD OPAn input offset voltage calibration function. The sink current generator could provide constant current no matter what V_{ISINK} voltage is ranging from 0.7 V to 4.5 V. The constant current value is controlled by the ISGDATA0 / ISGDATA1 register and the sink current range is 50 mA ~ 305 mA and 20 mA ~ 275 mA with 1 mA/steps and 8-bit resolution.

Table 4. Smoke Detector Register List

Register Name	Bit							
	7	6	5	4	3	2	1	0
SDSW0	SDS7	SDS6	SDS5	SDS4	SDS3	SDS2	SDS1	SDS0
SDSW1	D7	—	SDA0PCC1	SDA0PCC0	—	—	—	SDA1PCC0
SDPGAC0	—	—	SDA0PGA5	SDA0PGA4	SDA0PGA3	SDA0PGA2	SDA0PGA1	SDA0PGA0
SDPGAC1	SDA1PGA7	SDA1PGA6	SDA1PGA5	SDA1PGA4	SDA1PGA3	SDA1PGA2	SDA1PGA1	SDA1PGA0
SDA0VOS	D7	D6	SDA0OF5	SDA0OF4	SDA0OF3	SDA0OF2	SDA0OF1	SDA0OF0
SDA1VOS	D7	D6	SDA1OF5	SDA1OF4	SDA1OF3	SDA1OF2	SDA1OF1	SDA1OF0
ISGDATA0	D7	D6	D5	D4	D3	D2	D1	D0
ISGDATA1	D7	D6	D5	D4	D3	D2	D1	D0

- **SDSW0 Register**

Bit	7	6	5	4	3	2	1	0
Name	SDS7	SDS6	SDS5	SDS4	SDS3	SDS2	SDS1	SDS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	0	0	0	0	0	0	0

Bit 7 **SDS7**: Switch on / off control
0: Off
1: On

Bit 6 ~ 5 **SDS6 ~ SDS5**: Mode control
00: External mode
01: AC coupling mode
10: External mode
11: DC coupling mode (SDS1 can't ON at the same time)

Bit 4 **SDS4**: Switch on / off control
0: Off
1: On

Bit 3 **SDS3**: Switch on / off control
0: Off
1: On

Bit 2 **SDS2**: Switch on / off control
0: Off
1: On

Bit 1 **SDS1**: Switch on / off control
0: Off
1: On

Bit 0 **SDS0**: Switch on / off control
0: Off
1: On

- **SDSW1 Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	—	SDA0PCC1	SDA0PCC0	—	—	—	SDA1PCC0
R/W	R/W	—	R/W	R/W	—	—	—	R/W
POR	0	—	0	0	—	—	—	0

Bit 7 **D7**: This bit must be set to "0"

Bit 6 Unimplemented, read as "0"

Bit 5 ~ 4 **SDA0PCC1 ~ SDA0PCC0**: SD OPA0 Compensation capacitor control bits
00: 20 pF
01: 15 pF
10: 10 pF
11: 20 pF

Bit 3 ~ 1 Unimplemented, read as "0"

Bit 0 **SDA1PCC0**: SD OPA1 Compensation capacitor control bit
0: 30 pF
1: 15 pF

- **SDPGAC0 Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	SDA0PGA5	SDA0PGA4	SDA0PGA3	SDA0PGA2	SDA0PGA1	SDA0PGA0
R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
POR	—	—	0	0	0	0	0	0

Bit 7 ~ 6 Unimplemented, read as "0"

Bit 5 ~ 0 **SDA0PGA5 ~ SDA0PGA0**: R1 resistance control
R1 = (SDA0PGA[5:0] × 100 kΩ)
These bits are used to select the R1 resistance value. Note that R1 ≠ 0 Ω when these bits are set to "000000" due to the switch on-resistance.

• SDPGAC1 Register

Bit	7	6	5	4	3	2	1	0
Name	SDA1PGA7	SDA1PGA6	SDA1PGA5	SDA1PGA4	SDA1PGA3	SDA1PGA2	SDA1PGA1	SDA1PGA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 6 **SDA1PGA7 ~ SDA1PGA6**: R3 resistance control
00: 10 kΩ
01: 20 kΩ
10: 30 kΩ
11: 40 kΩ

Bit 5 ~ 0 **SDA1PGA5 ~ SDA1PGA0**: R2 resistance control
R2 = SDA1PGA[5:0] × 100 kΩ
These bits are used to select the R2 resistance value. Note that R2 ≠ 0 Ω when these bits are set to "000000" due to the switch on-resistance.

• SDA0VOS Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	SDA0OF5	SDA0OF4	SDA0OF3	SDA0OF2	SDA0OF1	SDA0OF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7 ~ 6 **D7 ~ D6**: These bits must be set to "00"

Bit 5 ~ 0 **SDA0OF5 ~ SDA0OF0**: SD OPA0 input offset voltage calibration control

• SDA1VOS Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	SDA1OF5	SDA1OF4	SDA1OF3	SDA1OF2	SDA1OF1	SDA1OF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7 ~ 6 **D7 ~ D6**: These bits must be set to "00"

Bit 5 ~ 0 **SDA1OF5 ~ SDA1OF0**: SD OPA1 input offset voltage calibration control

• ISGDATA0 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **D7 ~ D0**: Sink current generator control for ISINK0 pin
Current value (mA) = 50 + 1 × (D[7:0])
Note: When ISGS0 = 0, ISGDATA0[7:0] must set to 0 to prevent leakage current.

● **ISGDATA1 Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 ~ 0 **D7 ~ D0**: Sink current generator control for ISINK1 pin
Current value (mA) = 20 + 1 × (D[7:0])
Note: When ISGS1 = 0, ISGDATA1[7:0] must set to 0 to prevent leakage current.

5 Buzzer Driver – BD

The buzzer driver includes a boost converter and a buzzer watchdog timer (BWDT). The buzzer driver is used to drive either an external-driving 2-pin buzzer or a self-driving 3-pin buzzer. The block diagram is shown as below.

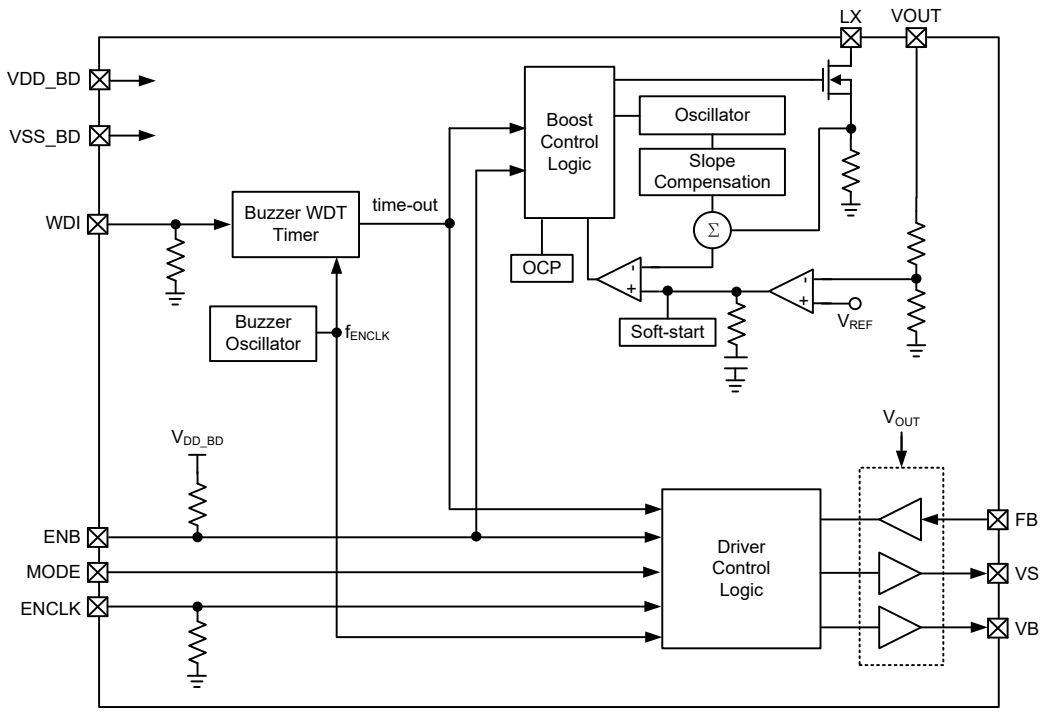


Figure 16. Buzzer Driver Block Diagram

The BWDT provides MCU failure alarm function, MCU must periodically toggle the WDI pin within t_{WDI} to reset the BWDT counter. If MCU fails to toggle the WDI pin, a timeout occurs, and the buzzer driver activate and alarm.

In normal mode, BWDT time-out flag = 0, it is controlled by ENB and ENCLK. When BWDT time-out flag = 1, ENB and ENCLK are invalid. The buzzer driver control table is shown as below.

Table 5. Buzzer Driver Control

BWDT Time-out Flag	ENB	MODE	ENCLK	Function Description
0	0	0	0	Boost on, 3-pin buzzer mode
0	0	0	1	Boost on, Buzzer off
0	0	1	x	Boost on, 2-pin buzzer mode ENCLK is buzzer clock input
0	1	x	x	Boost off, Buzzer off
1	x	0	x	Boost on, 3-pin buzzer mode
1	x	1	x	Boost on, 2-pin buzzer mode Buzzer clock is from BWDT

"x": Don't care

The WDI timing is shown in the figure below.

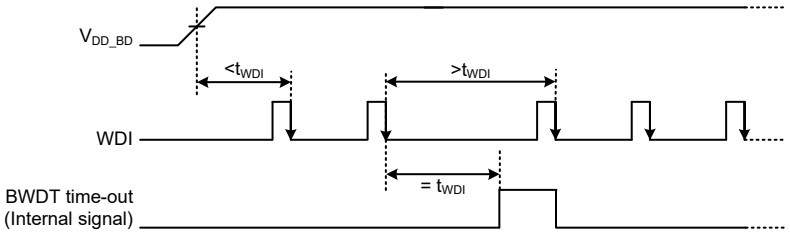


Figure 17. WDI Timing

6 Pin Assignment

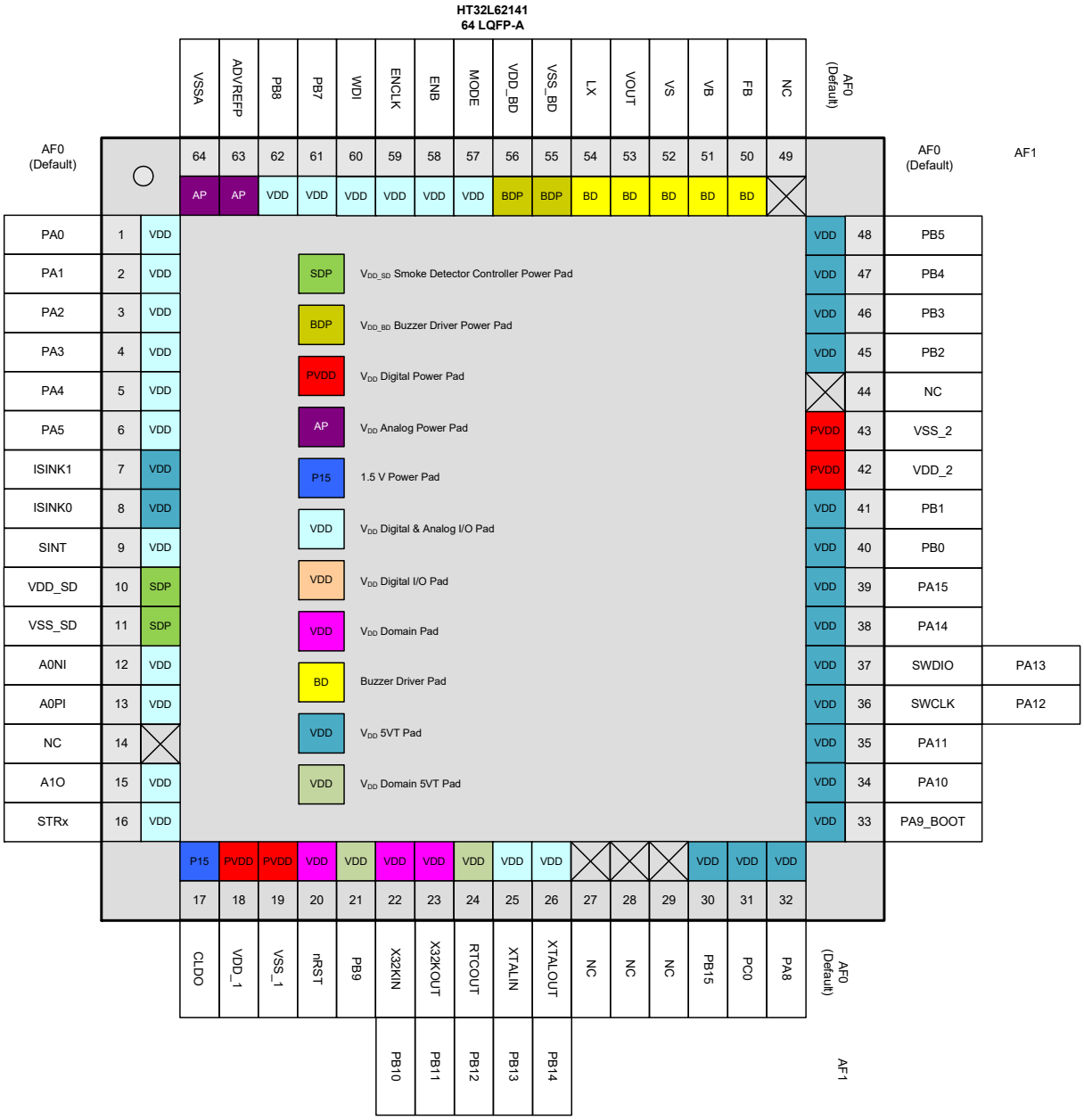


Figure 18. 64-pin LQFP Pin Assignment

Table 6. Pin Assignment

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64LQFP	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
1	PA0		ADC_ IN2		GT_ CH0	SPI1_ SCK	USR_ RTS	I2C1_ SCL								VBG
2	PA1		ADC_ IN3		GT_ CH1	SPI1_ MOSI	USR_ CTS	I2C1_ SDA								
3	PA2		ADC_ IN4		GT_ CH2	SPI1_ MISO	USR_ TX									
4	PA3		ADC_ IN5		GT_ CH3	SPI1_ SEL	USR_ RX									
5	PA4		ADC_ IN6		GT_ CH0	SPI0_ SCK	UR1_ TX	I2C0_ SCL								
6	PA5		ADC_ IN7		GT_ CH1	SPI0_ MOSI	UR1_ RX	I2C0_ SDA								
7	ISINK1															
8	ISINK0															
9	SINT															
10	VDD_SD															
11	VSS_SD															
12	A0NI															
13	A0PI															
15	A1O															
16	STRx															
17	CLDO															
18	VDD_1															
19	VSS_1															
20	nRST															
21	PB9				MT_ CH3											WAKEUP1
22	X32KIN	PB10			GT_ CH0	SPI1_ SEL	USR_ TX							SCTM0		
23	X32KOUT	PB11			GT_ CH1	SPI1_ SCK	USR_ RX							SCTM1		
24	RTCOUT	PB12				SPI0_ MISO	UR0_ RX							SCTM0		WAKEUP0
25	XTALIN	PB13			MT_ CH1		UR0_ TX	I2C0_ SCL								
26	XTALOUT	PB14			MT_ CH1N		UR0_ RX	I2C0_ SDA								
30	PB15				MT_ CH0	SPI0_ SEL		I2C1_ SCL								
31	PC0				MT_ CH0N	SPI0_ SCK		I2C1_ SDA						SCTM1		
32	PA8						USR_ TX							SCTM0		
33	PA9_ BOOT					SPI0_ MOSI								SCTM1		CKOUT
34	PA10				MT_ CH1	SPI0_ MOSI	USR_ RX									
35	PA11				MT_ CH1N	SPI0_ MISO								SCTM0		
36	SWCLK	PA12														
37	SWDIO	PA13														

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
64LQFP	System Default	GPIO	ADC	N/A	MCTM /GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
38	PA14				MT_ CH0	SPI1_ SEL	USR_ RTS	I2C1_ SCL								
39	PA15				MT_ CH0N	SPI1_ SCK	USR_ CTS	I2C1_ SDA						SCTM1		
40	PB0				MT_ CH1	SPI1_ MOSI	USR_ TX	I2C0_ SCL								
41	PB1				MT_ CH1N	SPI1_ MISO	USR_ RX	I2C0_ SDA						SCTM0		
42	VDD_2															
43	VSS_2															
45	PB2				MT_ CH2	SPI0_ SEL	UR1_ TX									CKIN
46	PB3				MT_ CH2N	SPI0_ SCK	UR1_ RX							SCTM1		
47	PB4				MT_ BRK	SPI0_ MOSI	UR1_ TX							SCTM0		
48	PB5				GT_ CH2	SPI0_ MISO	UR1_ RX									
50	FB															
51	VB															
52	VS															
53	VOUT															
54	LX															
55	VSS_BD															
56	VDD_BD															
57	MODE															
58	ENB															
59	ENCLK															
60	WDI															
61	PB7		ADC_ IN0		MT_ CH1	SPI0_ MISO	UR0_ TX	I2C1_ SCL								
62	PB8		ADC_ IN1		MT_ CH1N	SPI0_ SEL	UR0_ RX	I2C1_ SDA								
63	ADVREFP															
64	VSSA															
14, 27~29, 44, 49	NC															

Table 7. Pin Description

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64LQFP					Default Function (AF0)
1	PA0	AI/O	33V	4/8/12/16 mA	PA0
2	PA1	AI/O	33V	4/8/12/16 mA	PA1
3	PA2	AI/O	33V	4/8/12/16 mA	PA2
4	PA3	AI/O	33V	4/8/12/16 mA	PA3
5	PA4	AI/O	33V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
6	PA5	AI/O	33V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
7	ISINK1	AO	5V	—	Sink current source 1
8	ISINK0	AO	5V	—	Sink current source 0
9	SINT	I/O	33V	—	Smoke detector wake-up pin
10	VDD_SD	P	—	—	Voltage for Smoke Detector
11	VSS_SD	P	—	—	Ground reference for Smoke Detector
12	A0NI	AI	33V	—	Smoke detector OPA0 negative input
13	A0PI	AI	33V	—	Smoke detector OPA0 positive input
15	A1O	AO	33V	—	Smoke detector OPA1 output
16	STRx	I/O	33V	—	Smoke detector one-wire communication pin
17	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connect a 2.2 μF capacitor as close as possible between this pin and VSS_1.
18	VDD_1	P	—	—	Voltage for digital I/O
19	VSS_1	P	—	—	Ground reference for digital I/O
20	nRST(3)	I	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
21	PB9(3)	I/O (V_{DD})	5VT	4/8/12/16 mA	PB9
22	PB10(3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KIN
23	PB11(3)	AI/O (V_{DD})	33V	4/8/12/16 mA	X32KOUT
24	PB12(3)	I/O (V_{DD})	5VT	4/8/12/16 mA	RTCOUT
25	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
26	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
30	PB15	I/O	5VT	4/8/12/16 mA	PB15
31	PC0	I/O	5VT	4/8/12/16 mA	PC0
32	PA8	I/O	5VT	4/8/12/16 mA	PA8
33	PA9	I/O	5VT_PU	4/8/12/16 mA	PA9_BOOT
34	PA10	I/O	5VT	4/8/12/16 mA	PA10
35	PA11	I/O	5VT	4/8/12/16 mA	PA11
36	PA12	I/O	5VT_PU	4/8/12/16 mA	SWCLK
37	PA13	I/O	5VT_PU	4/8/12/16 mA	SWDIO
38	PA14	I/O	5VT	4/8/12/16 mA	PA14
39	PA15	I/O	5VT	4/8/12/16 mA	PA15
40	PB0	I/O	5VT	4/8/12/16 mA	PB0
41	PB1	I/O	5VT	4/8/12/16 mA	PB1
42	VDD_2	P	—	—	Voltage for digital I/O
43	VSS_2	P	—	—	Ground reference for digital I/O

Pin Number	Pin Name	Type(1)	I/O Structure(2)	Output Driving	Description
64LQFP					Default Function (AF0)
45	PB2	I/O	5VT	4/8/12/16 mA	PB2
46	PB3	I/O	5VT	4/8/12/16 mA	PB3
47	PB4	I/O	5VT	4/8/12/16 mA	PB4
48	PB5	I/O	5VT	4/8/12/16 mA	PB5
50	FB	AI	9V	—	Feedback input in the 3-pin buzzer mode, force to ground in the 2-pin buzzer mode
51	VB	AO	9V	—	Complementary output for buzzer driver
52	VS	AO	9V	—	Output for buzzer driver
53	VOUT	AO	9V	—	Boost converter output
54	LX	AO	9V	—	Power switch output
55	VSS_BD	P	—	—	Buzzer driver positive power supply
56	VDD_BD	P	—	—	Buzzer driver negative power supply, ground
57	MODE	I	33V	—	2-pin buzzer mode or 3-pin buzzer mode selection pin, connect to VDD_BD or VSS_BD
58	ENB	I	33V	—	Control buzzer driver on/off
59	ENCLK	I	33V	—	2-pin buzzer clock input and buzzer on/off
60	WDI	I	33V	—	BWDT input with pull-down resistor. The buzzer will active when BWDT time-out.
61	PB7	AI/O	33V	4/8/12/16 mA	PB7
62	PB8	AI/O	33V	4/8/12/16 mA	PB8
63	ADVREFP	P	—	—	Analog voltage for ADC
64	VSSA	P	—	—	Ground reference for the ADC
14, 27 ~ 29, 44, 49	NC	—	—	—	No connected

Note: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, V_{DD} = V_{DD} Power
2. 33V = 3.3 V-tolerant, 5VT = 5 V-tolerant, 9V = 9 V-tolerant.
3. These pins are located at the V_{DD} power domain.
4. In the Boot loader mode, only the UART interface can be used for communication.

7 Electrical Characteristics

Power Supply Scheme

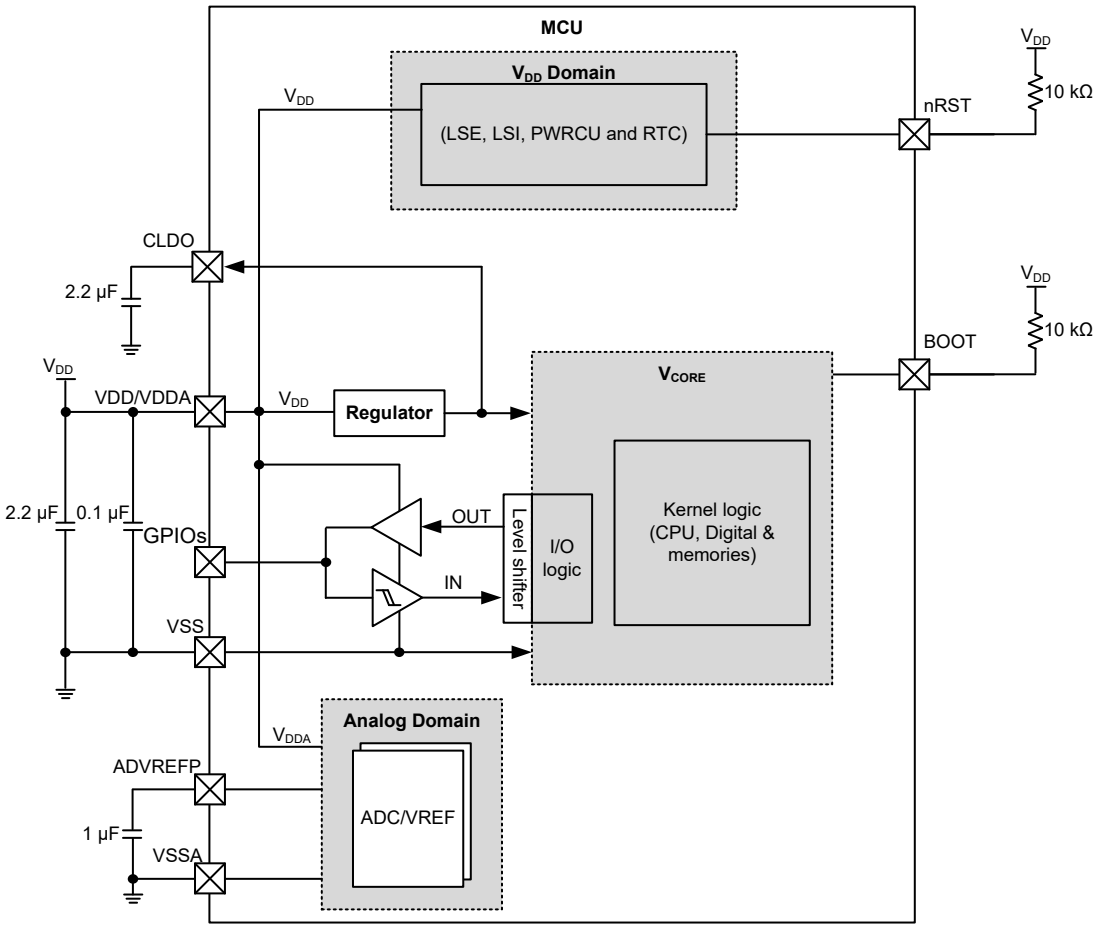


Figure 19. Power Supply Scheme

Note: 1. All regulator capacitors must be placed as close to the MCU as possible.
2. It is recommended that the pull-up resistor of the BOOT pin is 10 kΩ.
3. It is recommended that the pull-up resistor of the nRST pin is 10 kΩ.

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DD_SD}	External Smoke Detector Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DD_BD}	External Buzzer Driver Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{OUT} , LX, FB, VS, VB	Boost Supply Voltage	V_{SS_BD} - 0.3	V_{SS_BD} + 18	V
V_{SINK0}, V_{SINK1}	Sink0 and Sink1 Supply Voltage	V_{SS_SD} - 0.3	V_{SS_SD} + 6	V
V_{IN}	Input Voltage on 5 V-tolerant I/O	V_{SS} - 0.3	V_{SS} + 5.5	V
	Input Voltage on Other I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW

Recommended DC Operating Conditions

Table 9. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	I/O Operating Voltage	—	2.2	3.3	3.6	V
V_{DD_SD}	External Smoke Detector Supply Voltage	—	2.2	3.3	3.6	V
V_{DD_BD}	External Buzzer Driver Main Supply Voltage	—	2.2	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.0	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 10. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.2 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.2 V Regulator input	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

On-Chip Ultra-low Power LDO Voltage Regulator Characteristics

Table 11. ULDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ULDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.2 V Regulator input @ I_{ULDO} = 2 mA and voltage variant = ±5 %, after trimming	1.425	1.5	1.57	V
I_{ULDO}	Output Current	V_{DD} = 2.2 V ~ 3.6 V Regulator input @ V_{ULDO} = 1.5 V	—	2	5	mA
C_{ULDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	1	2.2	—	μF

Power Consumption

The current consumption is influenced by several parameters and factors, including the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The MCU is configured under the following conditions for current consumption measured:

- All I/O pins are set to a high-impedance (floating) state.
- All peripherals are disabled unless specifically stated otherwise.
- The Flash memory access time is optimized using the minimum wait states number, depending on the f_{HCLK} frequency.
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$.

Table 12. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Supply Current (Run Mode)	48 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz	All peripherals enabled	9.2	9.8	—	mA
				All peripherals disabled	3.9	4.2	—	
		32 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 32 MHz	All peripherals enabled	6.5	6.9	—	
				All peripherals disabled	3.0	3.2	—	
		16 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 16 MHz	All peripherals enabled	3.4	3.6	—	
				All peripherals disabled	1.60	1.73	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = off	All peripherals enabled	1.67	1.79	—	
				All peripherals disabled	0.82	0.89	—	
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz, LDO off, ULDO on	All peripherals enabled	7.0	7.6	—	μA
				All peripherals disabled	3.5	3.9	—	

Symbol	Parameter	f_{HCLK}	Conditions		Typ.	Max. @ T_A		Unit
						25 °C	85 °C	
I_{DD}	Supply Current (Sleep Mode)	48 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 48 MHz	All peripherals enabled	6.8	7.3	—	mA
				All peripherals disabled	0.81	0.90	—	
		32 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 32 MHz	All peripherals enabled	4.8	5.1	—	
				All peripherals disabled	0.68	0.77	—	
		16 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 16 MHz	All peripherals enabled	2.5	2.7	—	
				All peripherals disabled	0.56	0.65	—	
		8 MHz	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = off	All peripherals enabled	1.24	1.34	—	
				All peripherals disabled	295.9	345.7	—	μA
		32 kHz	V_{DD} = 3.3 V, LSI = 32 kHz, LDO off, ULDO on	All peripherals enabled	5.3	7.0	—	
				All peripherals disabled	1.41	1.75	—	
	Supply Current (Deep-Sleep 1 Mode)	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		1.15	1.48	—	μA
	Supply Current (Deep-Sleep 2 Mode)	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI on, RTC on		1.15	1.48	—	μA
	Supply Current (Deep-Sleep 3 Mode)	—	V_{DD} = 3.3 V, HSI/HSE/PLL clock off, LDO off, ULDO on, LSE off, LSI off, RTC off		0.54	0.86	—	μA
	Supply Current (Power-Down mode)	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC on		0.86	0.93	—	
			V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI on, RTC off		0.75	0.81	—	μA
	Supply Current (Deep Power-Down Mode)	—	V_{DD} = 3.3 V, LDO and ULDO off, LSE off, LSI off		0.12	0.14	—	

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSE means 32.768 kHz low speed external oscillator. LSI means 32 kHz low speed internal oscillator.
3. RTC means real-time clock.
4. Code = while (1) {208 NOP} executed in Flash.
5. The LVD or BOD function can only be used when the MCU is in the Run or Sleep mode. These functions are not available in the Deep-Sleep or Power-Down mode.

Reset and Supply Monitor Characteristics

Table 13. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	0.6	—	3.6	V
V_{POR}	Power On Reset Threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.40	1.55	1.65	V
V_{PDR}	Power Down Reset Threshold (Falling Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.27	1.45	1.57	V
$V_{PORHYST}$	POR Hysteresis	—	—	100	—	mV
t_{POR}	Reset Delay Time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.

2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO and ULDO will be turned off.

Table 14. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed	V_{DD} Falling edge	1.62	1.68	1.74	V
			V_{DD} Rising edge	1.68	1.74	1.8	
$V_{BODHYST}$	BOD Hysteresis	V_{DD} = 2.2 V	—	—	60	—	mV
V_{LVD}	Voltage of Low Voltage Detection	V_{DD} Falling edge	LVDS = 000	1.67	1.75	1.83	V
			LVDS = 001	1.87	1.95	2.03	V
			LVDS = 010	2.07	2.15	2.23	V
			LVDS = 011	2.27	2.35	2.43	V
			LVDS = 100	2.47	2.55	2.63	V
			LVDS = 101	2.67	2.75	2.83	V
			LVDS = 110	2.87	2.95	3.03	V
			LVDS = 111	3.07	3.15	3.23	V
$V_{LVDHYST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	200	—	μs
I_{DDLVD}	Operation Current (2)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.

2. Bandgap current is not included.

3. LVDS field is in the PWRCU LVDCSR register.

External Clock Characteristics

Table 15. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	—	2.2	—	3.6	V
f_{HSE}	HSE Frequency	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 00 V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEGAIN = 11	—	—	160	Ω
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Table 16. Low Speed External Clock (LSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	—	2.2	—	3.6	V
f_{CK_LSE}	LSE Frequency	V_{DD} = 2.2 V ~ 3.6 V	—	32.768	—	kHz
R_F	Internal Feedback Resistor	—	—	10	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V	30	—	TBD	kΩ
C_L	Recommended Load Capacitances	V_{DD} = 3.3 V	6	—	TBD	pF
I_{DDLSE}	Oscillator Supply Current (High Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L ≥ 7 pF, V_{DD} = 2.2 V ~ 2.7 V, T_A = -40 °C ~ 85 °C	—	3.3	6.3	μA
	Oscillator Supply Current (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, R_{ESR} = 50 kΩ, C_L < 7 pF, V_{DD} = 2.2 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	—	1.8	3.3	μA
	LSE Oscillator Power Down Current	—	—	—	0.01	μA
t_{SULSE}	LSE Oscillator Startup Time (Low Current Mode)	f_{CK_LSE} = 32.768 kHz, V_{DD} = 2.2 V ~ 3.6 V	500	—	—	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE / LSE clock in the PCB layout.

1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 17. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	—	2.2	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V, T_A = 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated HSI Oscillator Frequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-1	—	1	%
		V_{DD} = 2.2 V ~ 3.6 V, T_A = -20 °C ~ 60 °C	-1.5	—	2	%
		V_{DD} = 2.2 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-2.5	—	2.5	%
Duty	Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	HSI Oscillator Power Down Current	f_{HSI} = 8 MHz	—	—	0.05	μA
t_{SUHSI}	HSI Oscillator Startup Time	f_{HSI} = 8 MHz	—	—	10	μs

Table 18. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Voltage	T_A = -40 °C ~ 85 °C	2.2	—	3.6	V
f_{LSI}	LSI Frequency	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Oscillator Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V	—	—	100	μs

System PLL Characteristics

Table 19. System PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 20. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 21. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O 5 V-tolerant I/O Reset pin	V_I = V_{SS}, On-chip pull-up resistor disabled	—	—	3	μA
I_{IH}	High Level Input Current	3.3 V I/O 5 V-tolerant I/O Reset pin	V_I = V_{DD}, On-chip pull-down resistor disabled	—	—	3	μA
V_{IL}	Low Level Input Voltage	3.3 V I/O 5 V-tolerant I/O Reset pin		- 0.3	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.3	V
		5 V-tolerant I/O				5.5	
		Reset pin				V_{DD} + 0.3	
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O 5 V-tolerant I/O Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 5 V-tolerant I/O	4 mA drive, V_{OL} = 0.4 V	4	—	—	mA
		3.3 V I/O 5 V-tolerant I/O	8 mA drive, V_{OL} = 0.4 V	8	—	—	mA
		3.3 V I/O 5 V-tolerant I/O	12 mA drive, V_{OL} = 0.4 V	12	—	—	mA
		3.3 V I/O 5 V-tolerant I/O	16 mA drive, V_{OL} = 0.4 V	16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 5 V-tolerant I/O	4 mA drive, V_{OH} = V_{DD} - 0.4 V	4	—	—	mA
		3.3 V I/O 5 V-tolerant I/O	8 mA drive, V_{OH} = V_{DD} - 0.4 V	8	—	—	mA
		3.3 V I/O 5 V-tolerant I/O	12 mA drive, V_{OH} = V_{DD} - 0.4 V	12	—	—	mA
		3.3 V I/O 5 V-tolerant I/O	16 mA drive, V_{OH} = V_{DD} - 0.4 V	16	—	—	mA
V_{OL}	Low Level Output Voltage	3.3 V I/O 5 V-tolerant I/O	4 mA drive, I_{OL} = 4 mA	—	—	0.4	V
		3.3 V I/O 5 V-tolerant I/O	8 mA drive, I_{OL} = 8 mA	—	—	0.4	V
		3.3 V I/O 5 V-tolerant I/O	12 mA drive, I_{OL} = 12 mA	—	—	0.4	V
		3.3 V I/O 5 V-tolerant I/O	16 mA drive, I_{OL} = 16 mA	—	—	0.4	V

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{OH}	High Level Output Voltage	3.3 V I/O	4 mA drive, I_{OH} = 4 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
		3.3 V I/O	8 mA drive, I_{OH} = 8 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
		3.3 V I/O	12 mA drive, I_{OH} = 12 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
		3.3 V I/O	16 mA drive, I_{OH} = 16 mA	V_{DD} - 0.4	—	—	V
		5 V-tolerant I/O					
R_{PU}	Internal Pull-up Resistor	3.3 V I/O @ 3.3 V		—	60	—	kΩ
		5 V-tolerant I/O @ 3.3 V					
R_{PD}	Internal Pull-down Resistor	3.3 V I/O @ 3.3 V		—	60	—	kΩ
		5 V-tolerant I/O @ 3.3 V					

ADC Characteristics

Table 22. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.0	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V, 1 Msps	—	0.4	0.5	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.01	μA
f_{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	13	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 2	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin / pad capacitance included	—	4	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity Error	f_S = 750 ksps, V_{DDA} = 2.5 V ~ 3.6 V, ADCLVM = 0	—	±2	±5	LSB
		f_S = 750 ksps, V_{DDA} = 2.0 V ~ 3.5 V, ADCLVM = 1				
DNL	Differential Non-linearity Error	f_S = 750 ksps, V_{DDA} = 2.5 V ~ 3.6 V, ADCLVM = 0	—	±1	—	LSB
		f_S = 750 ksps, V_{DDA} = 2.0 V ~ 3.5 V, ADCLVM = 1				
E_O	Offset Error	—	—	—	±10	LSB

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

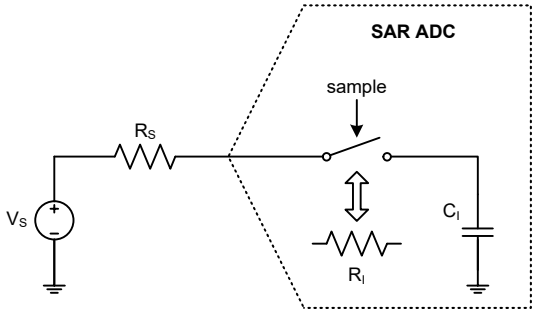


Figure 20. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0 V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

VDDA Monitor Characteristics

Table 23. VDDA Monitor Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
R	V_{DDA} Resistor Bridge	—	—	50	—	kΩ
Q	V_{DDA} Measurement Ratio	—	—	2	—	—
E_R	Ratio Error	—	-1	—	+1	%
t_{SVDDA}	ADC Sampling Time when Reading the V_{DDA}	—	5	—	—	μs

Note: Data based on characterization results only, not tested in production.

Bandgap Voltage Characteristics

Table 24. Bandgap Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.0	3.3	3.6	V
V_{BG}	Bandgap Reference Voltage	V_{DDA} = 2.0 V ~ 3.6 V @ T_A = -40 °C ~ 85 °C	1.206	1.218	1.23	V
I_{BG}	Bandgap Voltage Current	V_{DDA} = 3 V @ T_A = -40 °C ~ 85 °C	—	57	90	μA
I_{BG_BUF}	Bandgap Buffer Current	V_{DDA} = 3 V @ T_A = -40 °C ~ 85 °C, VREFEN = 1	—	75	120	μA
t_{BGST}	Bandgap Voltage Stable Time	V_{DDA} = 3.3 V @ T_A = -40 °C ~ 85 °C	—	5	20	μs
t_{SBG}	ADC Sampling Time when Reading Bandgap Voltage	—	5	—	—	μs
I_{BGPD}	Bandgap Voltage Power Down Current	—	—	—	0.01	μA

Note: Data based on characterization results only, not tested in production.

Internal Reference Voltage Characteristics

Table 25. Internal Reference Voltage Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—		2.3	—	3.6	V
V_{REF}	Internal Reference Voltage after Factory Trimming at 25 °C Temperature	V_{DDA} ≥ 2.3 V	VREFSEL[1:0] = 00	1.94	2.0	2.06	V
		V_{DDA} ≥ 2.8 V	VREFSEL[1:0] = 01	2.425	2.5	2.575	
		V_{DDA} ≥ 3.0 V	VREFSEL[1:0] = 10	2.619	2.7	2.781	
		V_{DDA} ≥ 3.3 V	VREFSEL[1:0] = 11	2.91	3.0	3.09	
C_L	Load Capacitor	—		0.1	2.2	4.7	μF
ACC_{VREF}	Reference Voltage Accuracy after Trimming	V_{DDA} = 2.3 V ~ 3.6 V, V_{REF} = 2.0 V, T_A = -40 °C ~ 85 °C		-1.5	—	1.5	%
t_{STABLE}	Reference Voltage Stable Time	V_{DDA} = 3.3 V, V_{BG} has been stabled, C_L = 2.2 μF, T_A = -40 °C ~ 85 °C, VREFOE = 1		—	—	350	μs
I_{DD}	Operating Current	V_{DDA} = 3.3 V, V_{REF} = 2.0 V, T_A = -40 °C ~ 105 °C, VREFOE = 1		—	20	30	μA
I_{DDPWD}	Reference Voltage Power Down Current	—		—	—	0.01	μA

SCTM / GPTM / MCTM Characteristics

Table 26. SCTM / GPTM / MCTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for SCTM / GPTM / MCTM	—	—	—	48	MHz
t_{RES}	Timer Resolution Time	—	1	—	—	$1/f_{TM}$
f_{EXT}	External Signal Frequency on Channel 0 ~ 3	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

Smoke Detector Characteristics

Table 27. Smoke Detector Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD_SD}	Operating Voltage	—	2.2	3.3	3.6	V
V_{IL}	Input Low Voltage for STRx and SINT Pins	—	0	—	0.2 V_{DD_SD}	V
V_{IH}	Input High Voltage for STRx and SINT Pins	—	0.8 V_{DD_SD}	—	V_{DD_SD}	V
R_{PU}	Internal Pull-up Resistor for STRx and SINT Pins	V_{DD_SD} = 3.3 V	—	60	—	kΩ
I_{OL}	Sink Current for STRx and SINT Pins	V_{OL} = 0.1 V_{DD_SD}, V_{DD_SD} = 3.3 V	16	32	—	mA
I_{OH}	Source Current for STRx and SINT Pins	V_{OH} = 0.9 V_{DD_SD}, V_{DD_SD} = 3.3 V	-4	-8	—	mA
I_{SINK0}	Sink Current for ISINK0 Pin	V_{ISINK0} = 3.0 V, ISGDATA0[7:0] = 00000000B	43.5	50	56.5	mA
		T_A = -40 °C ~ 85 °C, V_{ISINK0} = 1.0 V ~ 4.5 V ISGDATA0[7:0] = 00000000B	41	50	59	
		T_A = -40 °C ~ 85 °C, V_{ISINK0} = 0.7 V ~ 1.0 V ISGDATA0[7:0] = 00000000B	37.5	50	52.5	
		V_{ISINK0} = 3.0 V, ISGDATA0[7:0] = 11111111B	265	305	345	
		T_A = -40 °C ~ 85 °C, V_{ISINK0} = 1.0 V ~ 4.5 V ISGDATA0[7:0] = 11111111B	250	305	360	
		T_A = -40 °C ~ 85 °C, V_{ISINK0} = 0.7 V ~ 1.0 V ISGDATA0[7:0] = 11111111B	228	305	320	
I_{SINK1}	Sink Current for ISINK1 Pin	V_{ISINK1} = 3.0 V, ISGDATA1[7:0] = 00000000B	18.4	20	21.6	mA
		T_A = -40 °C ~ 85 °C, V_{ISINK1} = 1.0 V ~ 4.5 V ISGDATA1[7:0] = 00000000B	16.4	20	23.6	
		T_A = -40 °C ~ 85 °C, V_{ISINK1} = 0.7 V ~ 1.0 V ISGDATA1[7:0] = 00000000B	15	20	21	
		V_{ISINK1} = 3.0 V, ISGDATA1[7:0] = 11111111B	253	275	297	
		T_A = -40 °C ~ 85 °C, VISINK1 = 1.0 V ~ 4.5 V ISGDATA1[7:0] = 11111111B	225	275	324	
		T_A = -40 °C ~ 85 °C, VISINK1 = 0.7 V ~ 1.0 V ISGDATA1[7:0] = 11111111B	206	275	289	
T_{SST}	Power on Start Time	—	47	50	60	ms
$T_{SINT-WU}$	SINT Wake-up Pulse Time	—	12	15	18	µs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$T_{SINT-WU(D)}$	SINT Wake-up Signal Duration	Running variable[0x00] = 0x00	1382	1536	1690	μs
T_{SINT-S}	SINT Sampling Pulse Time	—	12	15	18	μs
$T_{CHn-OPAW}$	Channel n Waiting Time after OPA is on	n = A, running variable[0x05] = 0x00 n = B, running variable[0x0C] = 0x00	1382	1536	1690	μs
T_{CHn-ES}	Channel n Emission Stable Time	n = A, running variable[0x06] = 0x00 n = B, running variable[0x0D] = 0x00	691	768	845	μs
$T_{CHn-ADCSTO0}$	Channel n A/D Sample Timeout Time 0	n = A, running variable[0x07] = 0x00 n = B, running variable[0x0E] = 0x00	345	384	443	μs
$T_{CHn-ADCSTO1}$	Channel n A/D Sample Timeout Time 1	n = A, running variable[0x07] = 0x00 n = B, running variable[0x0E] = 0x00	576	640	704	μs
$T_{SINT-ISINKOFF}$	Trigger Time for the SINT Pin to Turn off the ISINK in Advance	—	5	—	—	μs
T_{SD}	Smoke Detection Period	Running variable [0x11] = 0x01	0.9	1	1.1	s
T_{TB}	Time Base Wake-up Period	Running variable [0x12] = 0x01	0.9	1	1.1	s
$T_{STRx-CR}$	STRx Communication Request Time	—	9	10	20	μs
T_{STRx-S}	STRx Send Start Signal Time	—	10	—	$T_{TIMEOUT}$	μs
$T_{STRx-TS}$	STRx Trigger Sampling Time	—	38	40	50	μs
$T_{STRx-TSP}$	STRx Trigger Response Time	—	—	60	80	us
T_{STRx-R}	STRx Slave Acknowledge Time	—	12	15	18	μs
$T_{DATA1(H)}$	Data 1 High-level Time	—	26	30	36	μs
$T_{DATA1(L)}$	Data 1 Low-level Time	—	8	10	12	μs
$T_{DATA0(H)}$	Data 0 High-level Time	—	8	10	12	μs
$T_{DATA0(L)}$	Data 0 Low-level Time	—	26	30	36	μs
$T_{TIMEOUT}$	Communication Timeout Time	—	—	454	520	μs
$T_{OPACALI}$	OPA Calibration Time	—	—	300	600	ms

Operational Amplifier Characteristics

Table 28. Operational Amplifier Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OPA}	Operating Current	No load	—	200	320	μA
V_{OS}	Input Offset Voltage	With calibration	-2	—	2	mV
I_{OS}	Input Offset Current	V_{IN} = 1/2 V_{CM}	—	1	10	nA
V_{CM}	Common Mode Voltage Range	—	V_{SS_SD}	—	V_{DD_SD} - 1.4	V
PSRR	Power Supply Rejection Ratio	—	50	70	—	dB
CMRR	Common Mode Rejection Ratio	—	50	80	—	dB
A_{OL}	Open Loop Gain	—	60	80	—	dB
SR	Slew Rate	R_{LOAD} = 1 MΩ, C_{LOAD} = 60 pF	600	1800	—	V/ms
GBW	Gain Bandwidth	R_{LOAD} = 1 MΩ, C_{LOAD} = 60 pF	800	2000	—	kHz
V_{OR}	Maximum Output Voltage Range	R_{LOAD} = 5 kΩ to V_{DD_SD}/2	V_{SS_SD} + 120	—	V_{DD_SD} - 140	mV

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{SC}	Output Short Circuit Current	R_{LOAD} = 5.1 Ω	±2	±20	—	mA

Note: Data based on characterization results only, not tested in production.

Buzzer Driver Characteristics

Table 29. Buzzer Driver Characteristics

V_{DD_BD} = 3.3 V, C_{IN} = 47 μF, LX = 10 μH, C_{OUT} = 2.2 μF and T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	No load, BWDT on, other circuits off	—	—	2	μA
I_{BD}	Operating Current	No load, BWDT on, Boost on, Regulator on, 2-pin buzzer mode, f_{ENCLK} = 4 kHz	—	2	4	mA
I_{LEAK}	Input Leakage Current	MODE = V_{DD_BD} or V_{SS_BD}	—	—	±1	μA
		ENB = V_{DD_BD}	—	—	-1	μA
		WDI, ENCLK = V_{SS_BD}	—	—	1	μA
R_{PH}	Pull-high Resistance	ENB	—	200	—	kΩ
R_{PL}	Pull-low Resistance	WDI, ENCLK	—	1	—	MΩ
t_{WDI}	WDI Period	V_{DD_BD} = 2.2 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	10.3	11.5	14.3	s
t_{WDTP}	WDT Reset Pulse Width	—	50	—	—	ns
V_{OUT}	Output Voltage	—	8.1	9	9.9	V
I_{OUT}	Output Current	—	50	—	—	mA
I_{OCP}	Over Current Protection	—	—	0.95	—	A
f_{SW}	Switch Frequency	—	0.8	1	1.2	MHz
I_{LFB}	FB Leakage Current	Buzzer off, FB = V_{SS_BD}	—	—	+1	μA
		Buzzer off, FB = V_{OUT}	—	-2.25	—	μA
V_{IH}	High-Level Input Voltage	FB	—	0.7 × V_{OUT}	V_{OUT}	—
V_{IL}	Low-Level Input Voltage	FB	V_{SS_BD}	0.3 × V_{OUT}	—	—
I_{OH}	VB, VS Source Current	V_{OUT} = 9 V, V_{OH} = 0.9 V_{OUT}	-70	-90	—	mA
I_{OL}	VB, VS Sink Current	V_{OUT} = 9 V, V_{OL} = 0.1 V_{OUT}	70	90	—	mA

I²C Characteristics

Table 30. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Plus Mode		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL And SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL And SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	START Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	START Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	STOP Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.

2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast plus mode, the peripheral clock frequency must be higher than 20 MHz.
5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

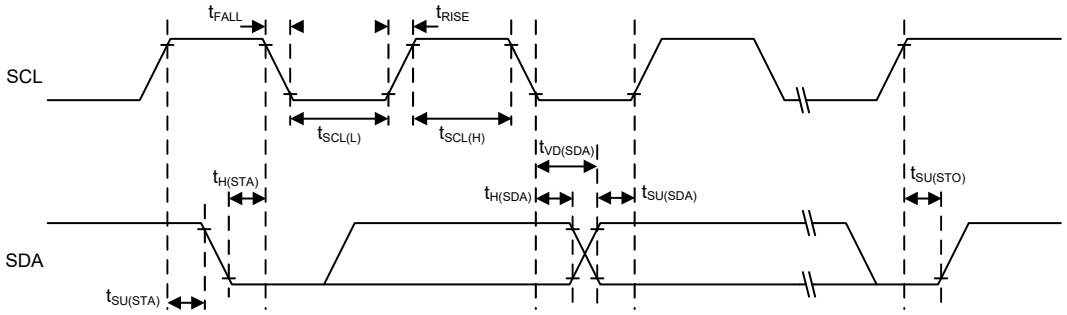


Figure 21. I²C Timing Diagrams

SPI Characteristics

Table 31. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master Mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	Master mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High And Low Time	—	$t_{SCK}/2$ - 2	—	$t_{SCK}/2$ + 1	ns
$t_{V(MO)}$	Data Output Valid Time	—	-	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave Mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	Slave mode, SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	$3 \times t_{PCLK}$	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	$2 \times t_{PCLK}$	—	—	Ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	$3 \times t_{PCLK}$	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

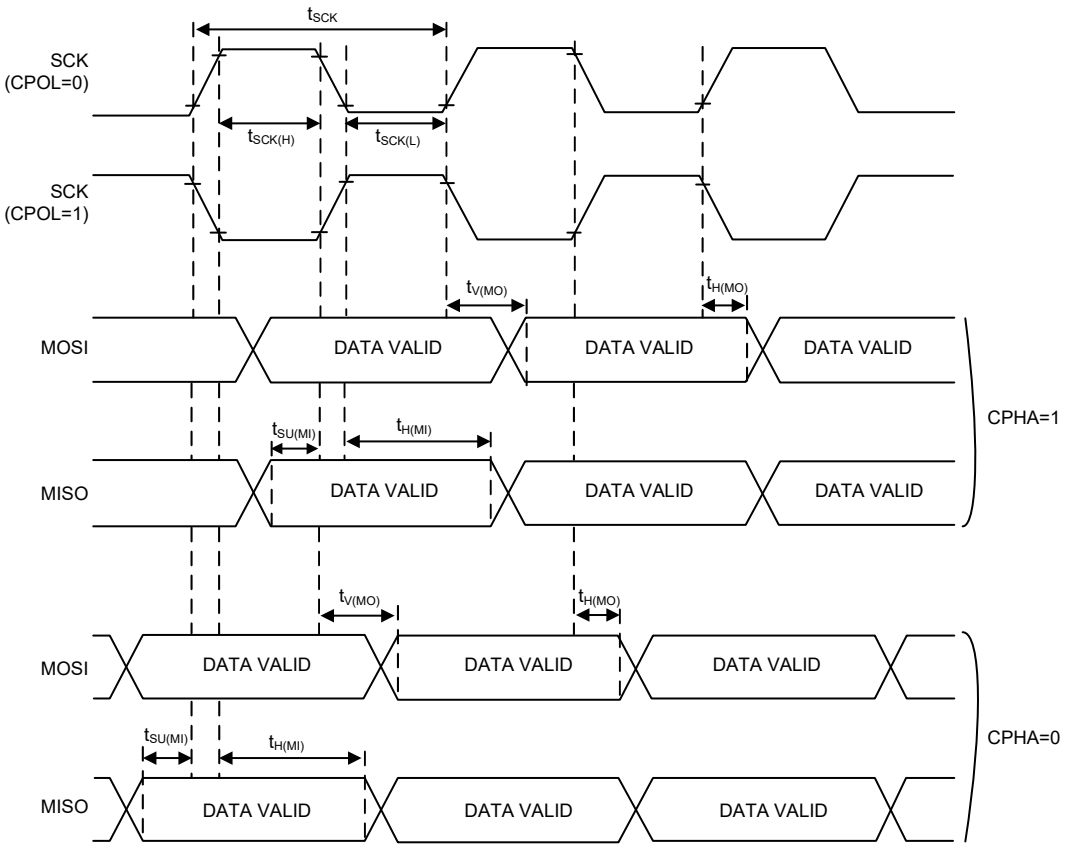


Figure 22. SPI Timing Diagrams – SPI Master Mode

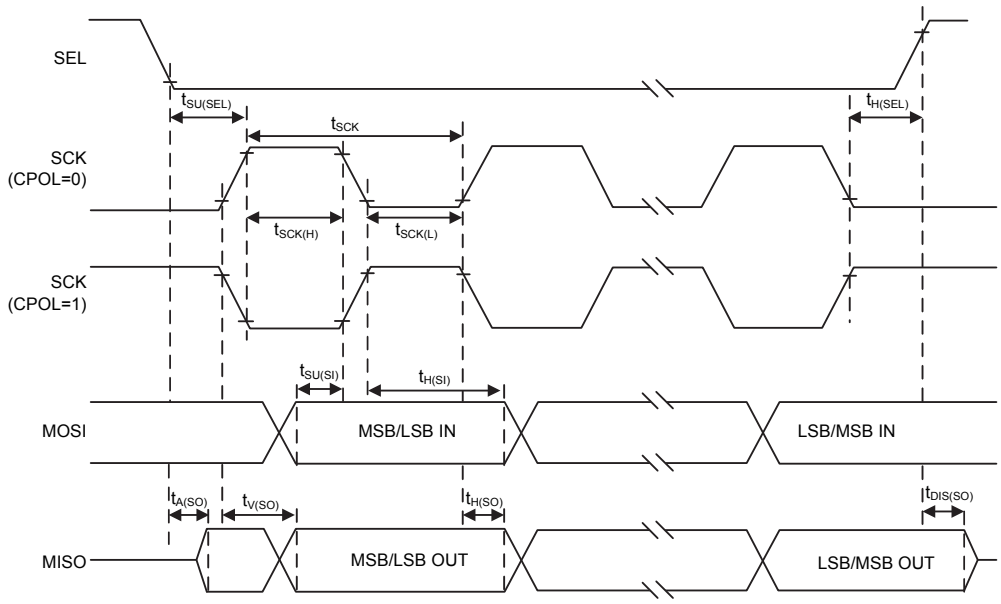


Figure 23. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

8 Application Circuits

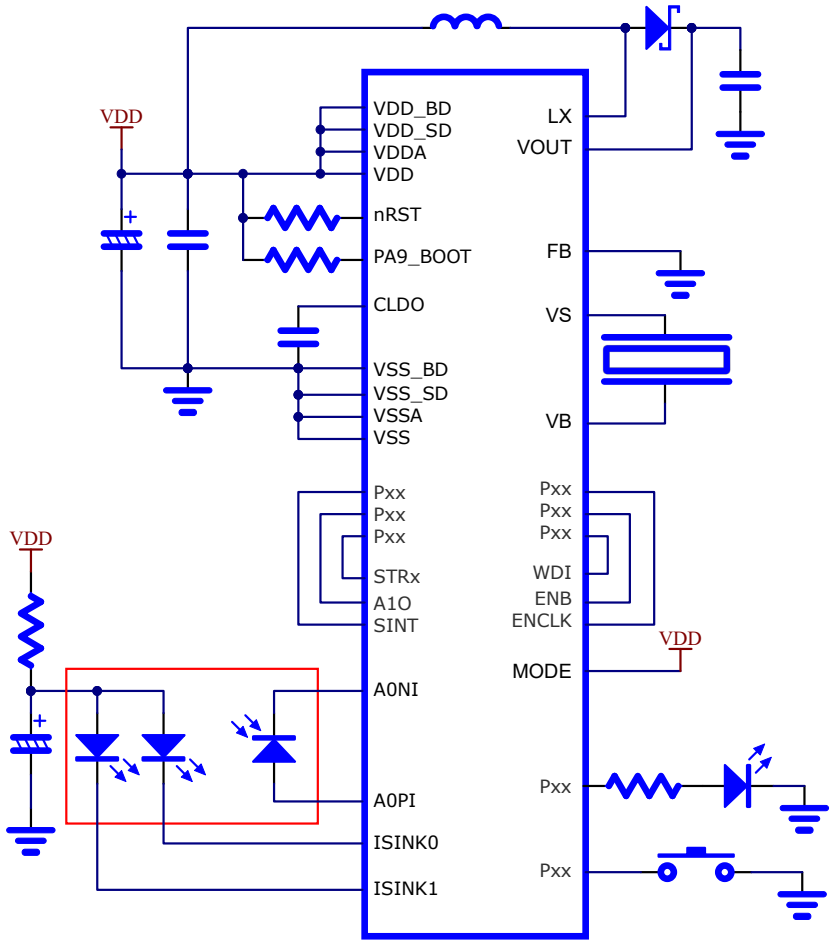


Figure 24. Application Circuits – 2-pin Buzzer Mode

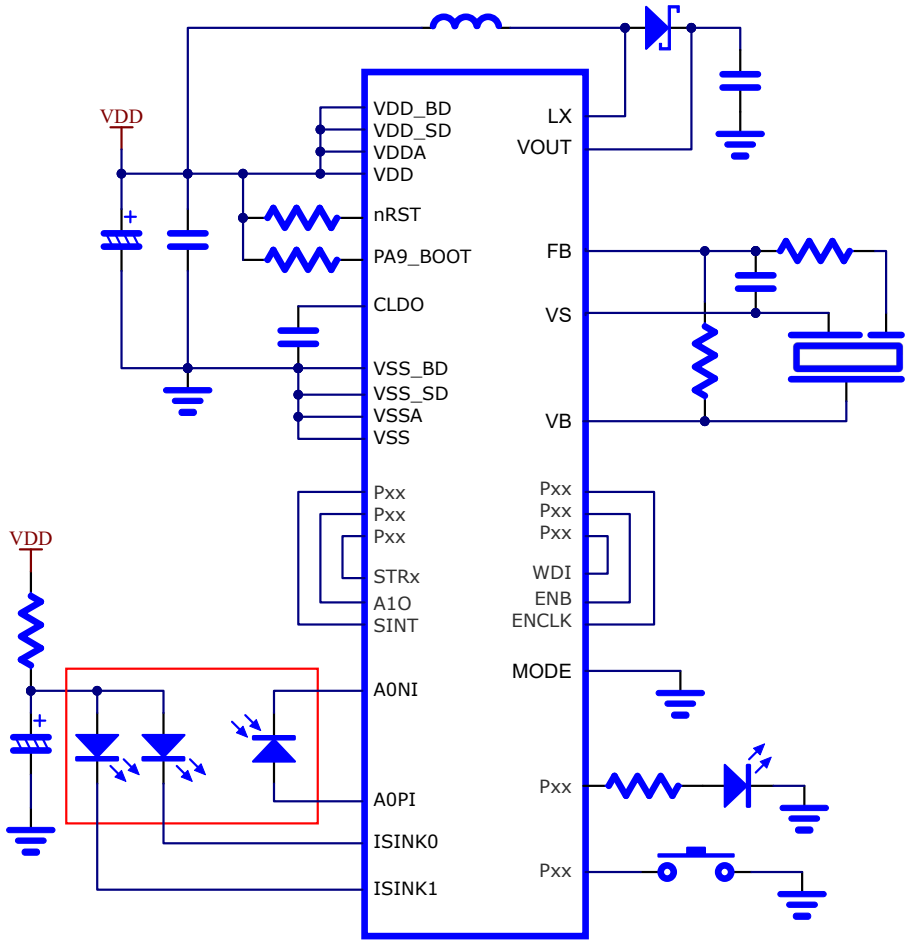


Figure 25. Application Circuits – 3-pin Buzzer Mode

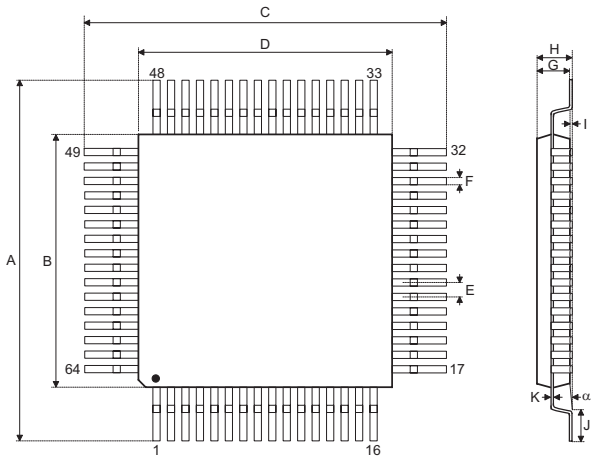
9 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

64-pin LQFP (7mm × 7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A		0.354 BSC	
B		0.276 BSC	
C		0.354 BSC	
D		0.276 BSC	
E		0.016 BSC	
F	0.005	0.007	0.009
G	0.053	0.055	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	0.024	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A		9.00 BSC	
B		7.00 BSC	
C		9.00 BSC	
D		7.00 BSC	
E		0.40 BSC	
F	0.13	0.18	0.23
G	1.35	1.40	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	0.60	0.75
K	0.09	—	0.20
α	0°	—	7°

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