Features

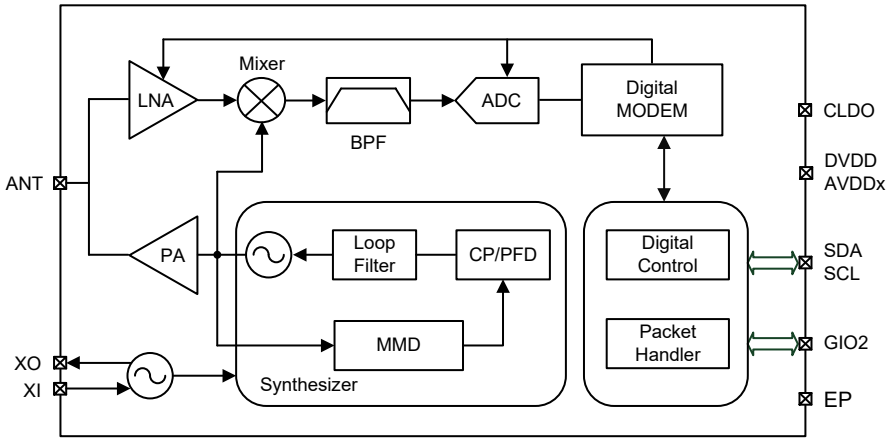
- Supports GFSK (BT=0.5) modulation with 1Mbps data rate, compliant with BLE standard
- Operating frequency: 2402/2426/2480MHz
- Operating voltage range: 1.9V~3.6V
- Programmable TX power: -10/-5/0/+5dBm (Max. +5dBm)
- Low current consumption
  - Low deep sleep current: 0.35μA
  - TX current consumption: 22mA @ 5dBm TX power
  - TX current consumption: 13.5mA @ -5dBm TX power
  - RX current consumption: 18.5mA
- Supports 32MHz crystal
- FCC/ETSI compliant
- Single-pin antenna interface
- Package type: 10-pin SOP-EP

General Description

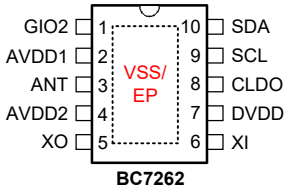
Bluetooth Beacon adopts BLE advertising feature to support new applications such as indoor navigation, healthcare, BLE advertising, sensing, security, remote control, light control, etc. The advertised packets are placed in the Channel 37, 38 and 39 to avoid the interference from WiFi channels at ISM band. The BC7262 is aimed for the Beacon device for various proximity aware applications.

The BC7262 is a low-cost 2.4GHz BLE Beacon transceiver. With an external 32MHz crystal (XO), an MCU and a few ceramic capacitors, it can implement a complete Beacon device. The output power level can be programmed from -10dBm to +5dBm for various applications. 18.5mA RX current consumption and maximum of +5dBm with 22mA TX current consumption can be achieved even for a small-size 10-pin SOP-EP package.

Block Diagram



Pin Assignment



BC7262
10 SOP-EP-A

Pin Description

Pin No.	Pin Name	Type	Pin Description
1	GIO2	DI/DO	General purpose pin
2	AVDD1	PWR	RF analog positive power supply
3	ANT	AI/AO	RF pin, connected to a matching circuit
4	AVDD2	PWR	RF analog positive power supply
5	XO	AO	Crystal output
6	XI	AI	Crystal input
7	DVDD	PWR	RF digital positive power supply
8	CLDO	PWR	LDO output, connected to a bypass capacitor
9	SCL	DI	I^2C clock input
10	SDA	DI/DO	I^2C data
	VSS/EP (Note)	PWR	Exposed pad, must be connected to ground

Legend: DI: Digital Input; DI/DO: Digital Input/Output; AI: Analog Input;
AO: Analog Output; PWR: Power

Note: 1. The VSS/EP pin is located at the exposed pad.
2. The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}-0.3V to V_{SS}+3.6V

Voltage on I/O Ports ..... V_{SS}-0.3V to V_{DD}+0.3V

Storage Temperature ..... -60°C to 150°C

Operating Temperature ..... -40°C to 85°C

ESD HBM ..... ≥±2kV

The device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C, V_{DD}=3.3V, GFSK modulation with matching circuit, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Supply Voltage	—	1.9	3.3	3.6	V
Digital I/Os						
V_{IH}	High Level Input Voltage	—	0.7×V_{DD}	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	0.3×V_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH}=-5mA	0.8×V_{DD}	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL}=5mA	0	—	0.2×V_{DD}	V
Current Consumption						
$I_{DeepSleep}$	Deep Sleep Mode Current	—	—	0.35	1.00	μA
$I_{LightSleep}$	Light Sleep Mode Current	X'tal on	—	1	—	mA

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{TX}	TX Mode Current	RF output power=-10dBm	—	11.5	—	mA
		RF output power=-5dBm	—	13.5	—	
		RF output power=0dBm	—	17	—	
		RF output power=5dBm	—	22	—	
I_{RX}	RX Mode Current	RX mode	—	18.5	—	mA

A.C. Characteristics

RF Characteristics

Ta=25°C, V_{DD}=3.3V, GFSK modulation with matching circuit, unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
RF Characteristics						
f_{RF}	RF Operating Frequency	CH37	—	2402	—	MHz
		CH38	—	2426	—	
		CH39	—	2480	—	
DR	Data Rate	GFSK modulation	—	1	—	Mbps
Transmitter Characteristics						
$t_{ST,TX}$	TX Settling Time	Light sleep mode to Transmit mode	—	TBD	—	μs
P_{OUT}	TX Output Power	—	-10	—	5	dBm
S.E.$_{TX}$	TX Spurious Emission	f < 1GHz	—	—	-36	dBm
		47MHz < f < 74MHz	—	—	-54	
		87.5MHz < f < 118MHz				
		174MHz < f < 230MHz				
		470MHz < f < 862MHz				
		2nd, 3rd Harmonic	—	—	-30	
		1.8GHz~1.9GHz	—	—	-47	
		5.15GHz~5.3GHz	—	—	-47	
Receiver Characteristics						
P_{Sens}	RX Sensitivity @ BER=0.1%	F_{DEV}=250kHz	—	-93	—	dBm
$P_{IN,max}$	Maximum Input Power	@BER < 0.1%	—	—	10	dBm
IR	Image Rejection	—	—	30	—	dB
S.E.$_{RX}$	Receiver Spurious	25MHz~1GHz	—	—	-57	dBm
		f > 1GHz	—	—	-47	
	RSSI Range	AGC on	-100	—	-20	dBm
LO Characteristics						
f_{LO}	RF Frequency Coverage Range	—	2400	—	2520	MHz
PN_{LO}	Phase Noise	@100kHz offset	—	-81	—	dBc/Hz
		@1MHz offset	—	-104	—	
Crystal (X'tal) Osicillator						
f_{XTAL}	X'tal Frequency	—	—	32	—	MHz
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C_{LOAD}	X'tal Capacitor Load	—	12	—	16	pF
TOL	X'tal Tolerance	—	-20	—	+20	ppm
t_{SU}	X'tal Startup Time	49US with a 12pF C_{LOAD}	—	—	1	ms
		3225 SMD with a 12pF C_{LOAD}	—	3	—	

I²C Characteristics

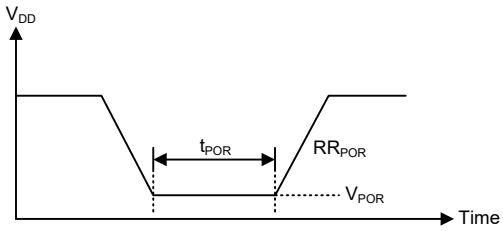
Ta=-40°C~85°C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCL}	Serial Clock Frequency	—	—	—	1	MHz
t_{BUF}	Bus Free Time between Stop and Start Condition	SCL=1MHz	250	—	—	ns
t_{LOW}	SCL Low Time	SCL=1MHz	500	—	—	ns
t_{HIGH}	SCL High Time	SCL=1MHz	500	—	—	ns
$t_{su(DAT)}$	Setup Time SDA → SCL	SCL=1MHz	100	—	—	ns
$t_{su(STA)}$	Start Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{su(STO)}$	Stop Condition Setup Time	SCL=1MHz	250	—	—	ns
$t_{h(DAT)}$	Hold Time SDA → SCL	SCL=1MHz	100	—	—	ns
$t_{h(STA)}$	Start Condition Hold Time	SCL=1MHz	250	—	—	ns
$t_{r(SCL)}$	Rise Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{f(SCL)}$	Fall Time of SCL Signal	SCL=1MHz	—	—	100	ns
$t_{r(SDA)}$	Rise Time of SDA Signal	SCL=1MHz	—	—	100	ns
$t_{f(SDA)}$	Fall Time of SDA Signal	SCL=1MHz	—	—	100	ns

Power-on Reset Electrical Characteristics

Ta=25°C

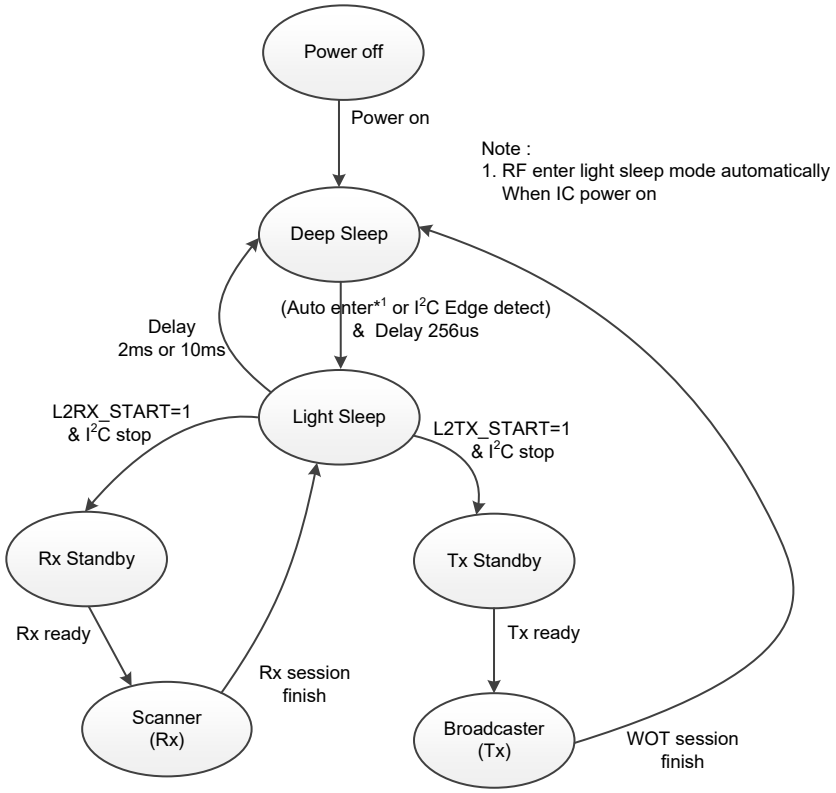
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	V_{DD} Start Voltage to Ensure Power-on Reset	—	—	—	—	100	mV
RR_{POR}	V_{DD} Rising Rate to Ensure Power-on Reset	—	—	0.035	—	—	V/ms
t_{POR}	Minimum Time for V_{DD} Stays at V_{POR} to Ensure Power-on Reset	—	—	1	—	—	ms



Functional Description

State Machine

The device provides six operating modes, Power Off mode, Deep Sleep mode, Light Sleep mode, Standby mode, TX mode and RX mode. An external MCU can set RF parameters, transmit data, receive data and wake up the RF chip via the I²C interface.



Note: 1. Deep Sleep mode: X'tal off.

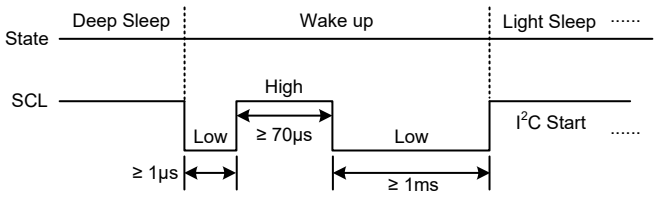
Light Sleep mode: X'tal on, RF frequency synthesizer off.

Standby mode: X'tal on, RF frequency synthesizer on, RF PA off.

TX mode: X'tal on, RF frequency synthesizer on, RF PA on.

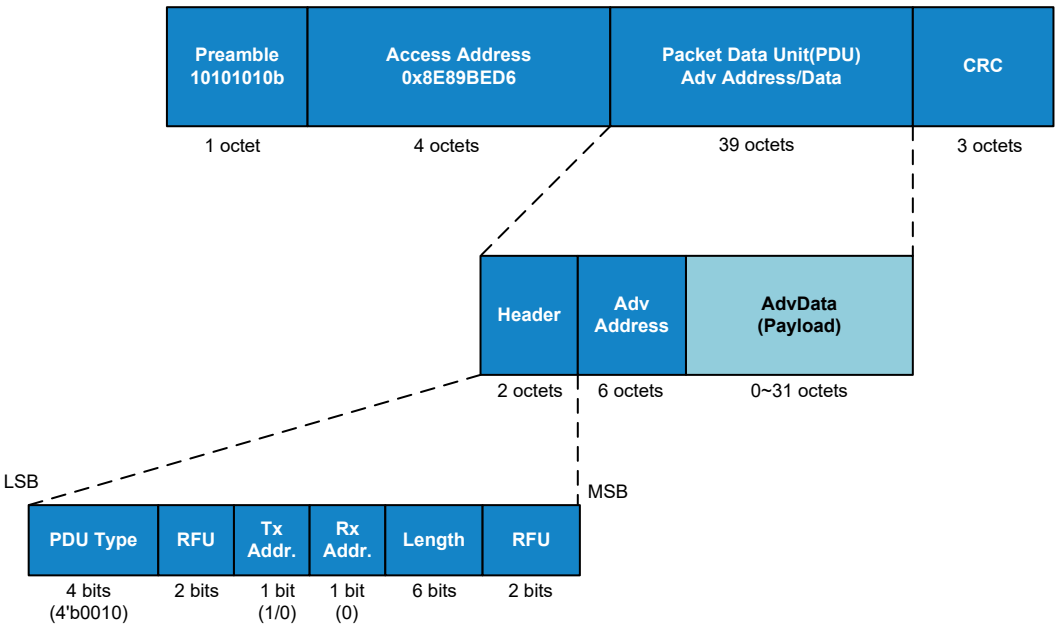
RX mode: X'tal on, RF frequency synthesizer on, RF LNA on.

2. In the Light Sleep mode, if the SDA and SCL pin states both keep unchanged for 10ms, the device state will change to the Deep Sleep mode. If the SDA or SCL pin state has been toggled and then keeps unchanged, the timer will reset and recount until the 10ms time is up and then enter the Deep Sleep mode.
3. The device will be woken up from the Deep Sleep mode if a falling edge is detected on the SCL pin and the low pulse width should be maintained at least 1ms to return to Light Sleep state. After this, the master MCU can control the device based on the I²C format.



4. Each frame will be sent consecutively until the frame counter (PKT_AUTORS) is finished then enter the Light Sleep mode.

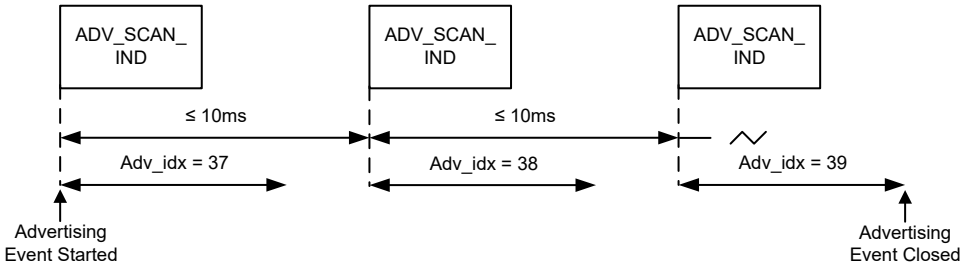
Packet Format



Packet Event Timing

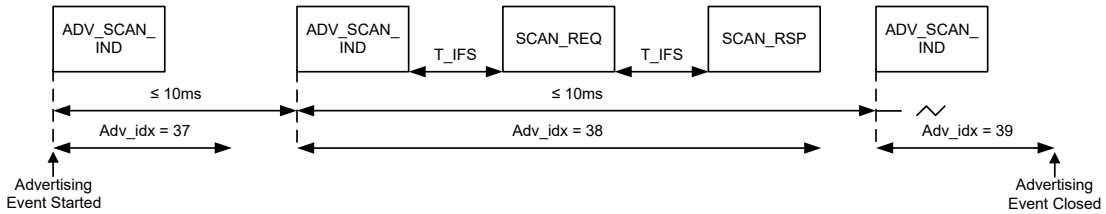
Scannable Undirected Event Type

The time between the beginning of two consecutive ADV_SCAN_IND PDUs within an advertising event should be less than or equal to 10ms. The advertising event shall be closed within the advertising interval. The structure of an advertising event in which no SCAN_REQ PDU is received as shown below.

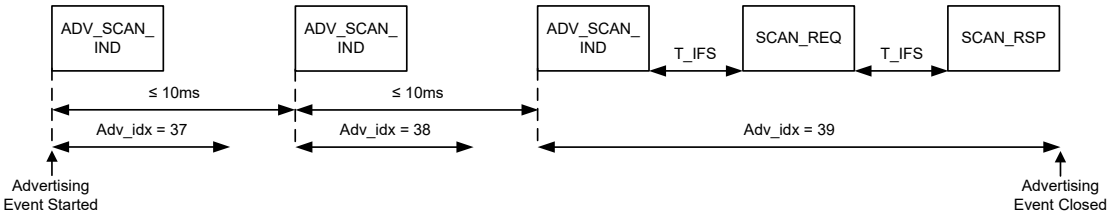


Scannable Event with only Advertising PDUs

The Inter Frame Space is known as "T_IFS" and the time should be 150μs. Two examples advertising events are as shown below, a SCAN_REQ PDU is received and a SCAN_RSP PDU is sent. For the case, all the advertising channels are used.



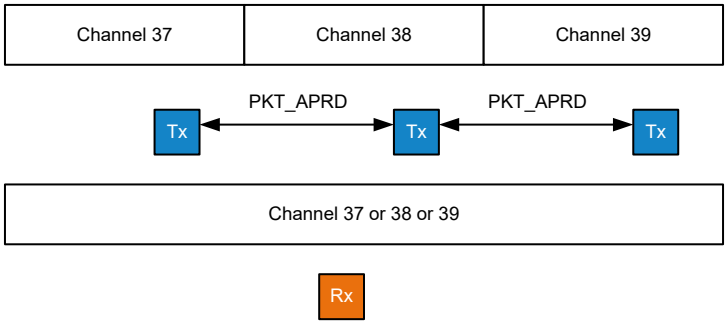
Scannable Event with SCAN_REQ and SCAN_RSP PDUs in the Middle of Event



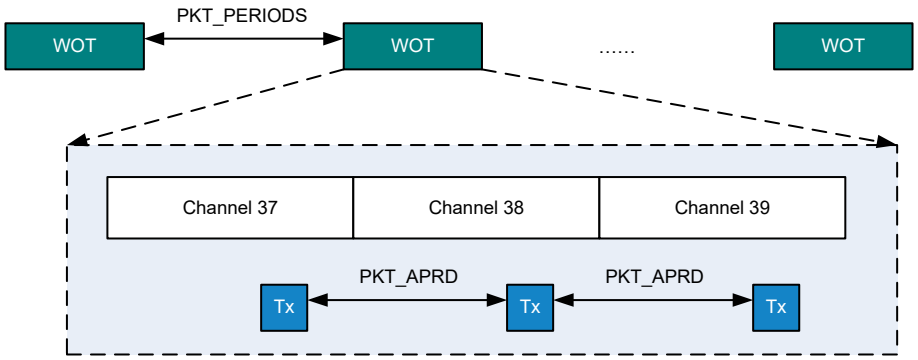
Scannable Event with SCAN_REQ and SCAN_RSP PDUs at the End of Event

Beacon Link Layer Protocol

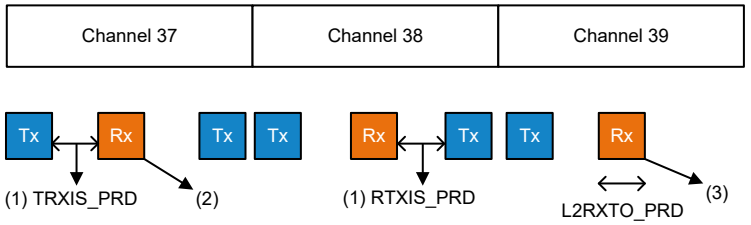
There are some cases about Beacon link layer protocol for Holtek RF design are introduced as shown in following figures.



L2RSP_EN=0, only TX or RX

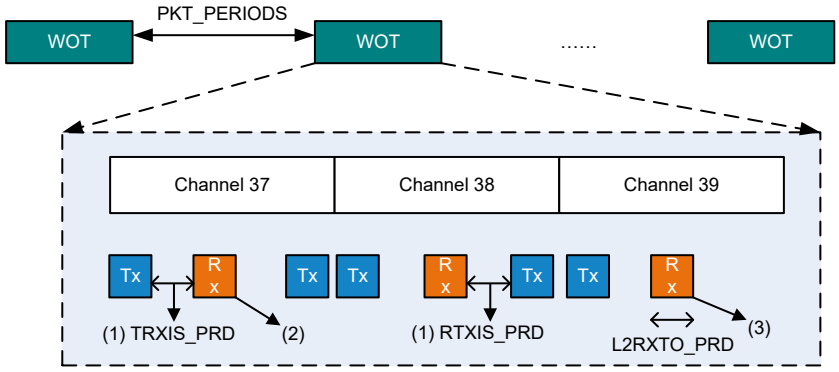


L2RSP_EN=0, Wake on TX (WOT)



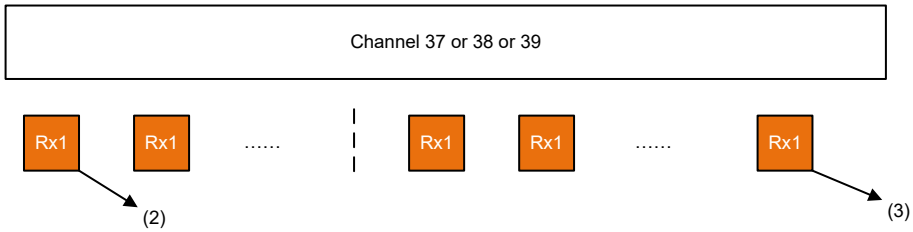
(1) TRXIS_PRD and RTXIS_PRD ≤ 150μs
(2) Next TX generation condition:
A. Received packet CRC pass
B. If WLA_FEN = 1, and check white list address match
(3) RX time-out or CRC fail or white list address match fail

L2RSP_EN=1, TRT Transmitter



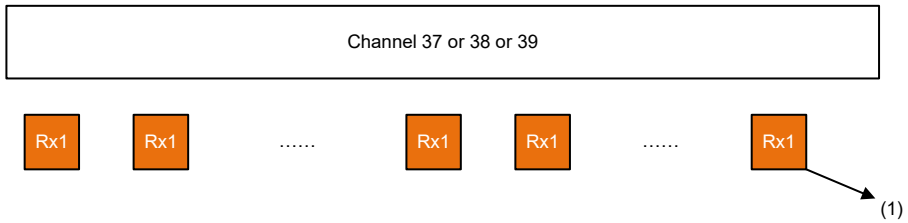
(1) Generate IRQ to MCU when the whole WOT sessions are completed

L2RSP_EN=1, TRT Transmitter (WOT)



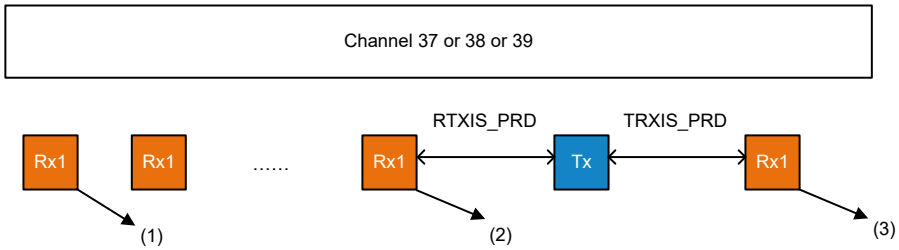
(1) No support wake on RX(WOR)
(2) RX continuous: PDU type check fail or CRC fail or white list address match fail
(3) RX complete:
A. Received packet CRC pass
B. If WLA_FEN = 1, and check white list address match
C. If RXPLHT_FEN = 1, PDU type ADV_DIRECT_IND or ADV_NONCONN_IND or ADV_SCAN_IND or ADV_IND check OK
D. Generate IRQ to MCU

L2RSP_EN=0, Continuous RX



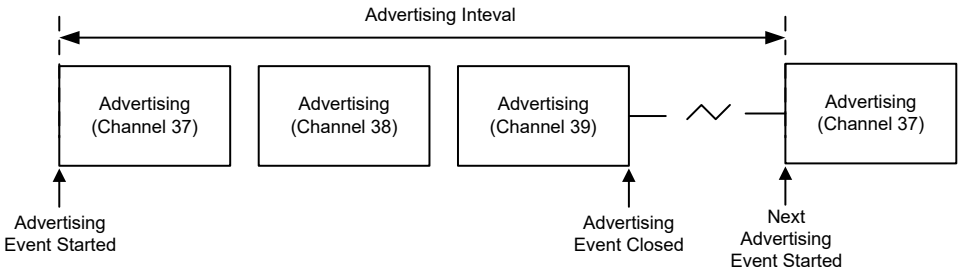
(1) RX complete:
A. Received packet CRC pass
B. If WLA_FEN = 1, and check white list address match
C. PDU type ADV_DIRECT_IND or ADV_NONCONN_IND check ok
D. Generate IRQ to MCU

L2RSP_EN=1, Continuous RX

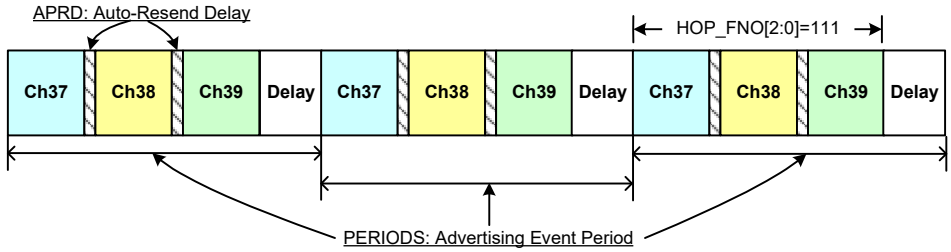


(1) RX continuous: PDU type check fail or CRC fail or white list address match fail
(2) Next TX generation condition:
A. Received packet CRC pass
B. If WLA_FEN = 1, and check white list address match
C. PDU type ADV_SCAN_IND or ADV_IND check OK
(3) RX complete:
A. Generate IRQ to MCU and no matter RX ok or fail or time-out

L2RSP_EN=1, RTR Receiver



Advertising Inteval = Advertising Event Period + Random



PKT_APRD[4:0]: Packet format auto-resend delay, 250μs (Min.) ~ 8ms (Max.)

PKT_AUTORS[7:0]: Packet event auto-resend times

0: No resend (auto-resend disabled)

1: Resend 1 time

2: Resend 2 times

:

254: Resend 254 times

255: Always resend periodicly until the MCU forcibly turns off the TX transmitter

PKT_PERIODS[9:0]: Advertising event period

Period=10ms×(1+PKT_PERIODS[9:0])

00-0000-0000: 10ms

00-0000-0001: 20ms

…

11-1111-1111: 10240ms (10.24s)

HOP_FNO[2:0]: Hopping frequency number

Bit0/Bit1/Bit2 indicates the enable bit for CH37/CH38/CH39 respectively.

It is not recommended to set these bits to "000". Ensure that there is at least one channel enabled.

For example:

001: CH37 enabled, CH38/CH39 disabled; each advertising event only includes CH37

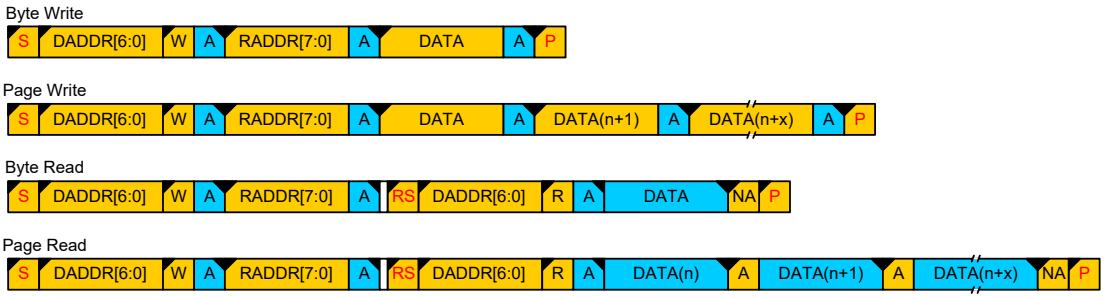
110: CH38/CH39 enabled, CH37 disabled; each advertising event only includes CH38 and CH39

101: CH37/CH39 enabled, CH38 disabled; each advertising event only includes CH37 and CH39

111: CH37/CH38/CH39 enabled; each advertising event includes CH37, CH38 and CH39

I²C Serial Programming

The device supports the I²C format for byte write, page write, byte read and page read formats. Regarding the page write/read, register address will not automatically increase for the FIFO port (address: 10h) when continuously writing/reading data to/from the FIFO.



Bus Direction: : Host to device; : Device to host

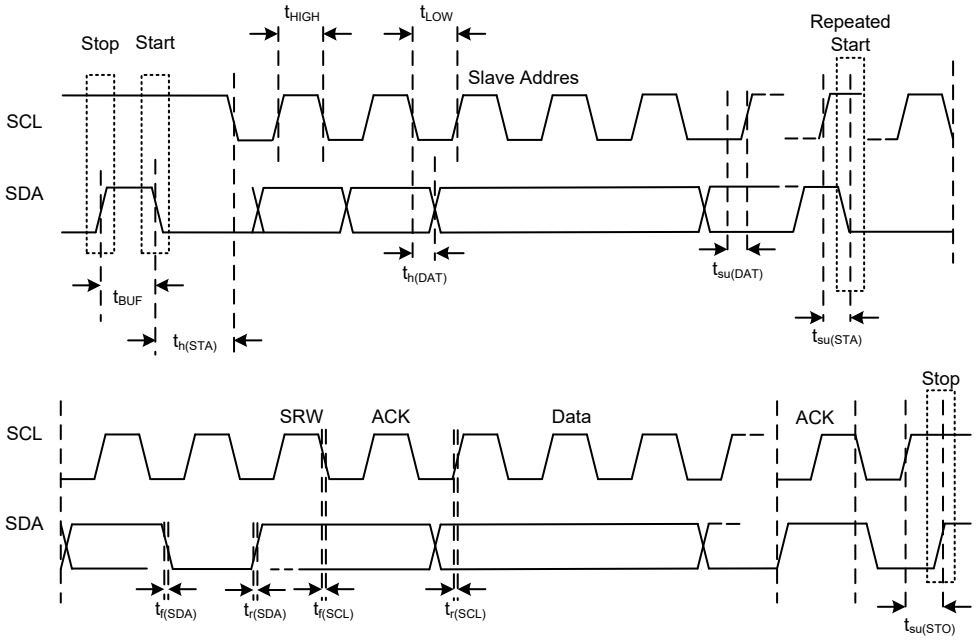
Symbol Definitions: S: Start; RS: Repeated Start; P: Stop;

DADDR[6:0]: Device Address, 71h;

R/W: Read/Write select; R: Read(1); W: Write(0);

RADDR[7:0]: register address;

A: ACK(0); NA: NAK(1)



Configuration Registers

Addr.	Bit							
	7	6	5	4	3	2	1	0
03h	PDUDATA[7:0]							
04h	RSTPDUFF	—						
05h	WHTSDS	WHTSD[6:0]						
06h	PKT_AUTORS[7:0]							
07h	APRD_PDTH[1:0]		RNDDLY_EN	PKT_APRD[4:0]				
08h	PKT_PERIODS[7:0]							
09h	—						PKT_PERIODS[9:8]	
0Bh	L2RSP_EN	—	L2RX_START	L2TX_START	—	HOP_FNO[2:0]		
15h	FSCALE[7:0]							
16h	FSCALE[15:8]							
17h	FD_HOLD[7:0]							
39h	ACCESS_ADDR[7:0]							
3Ah	ACCESS_ADDR[15:8]							
3Bh	ACCESS_ADDR[23:16]							
3Ch	ACCESS_ADDR[31:24]							
3Dh	—						L2RXTO_EN	—
3Eh	—				L2RXTO_PRD[3:0]			
3Fh	—		PMLEN	WHT_EN	PLTEN	PDUD_RS	FIFO_SEL	BKMODE
40h	PLH1_RXA	PLH1_TXA	—		PLH1_TYPE[3:0]			
41h	—		PLH1_LEN[5:0]					
42h	PLH2_RXA	PLH2_TXA	—		PLH2_TYPE[3:0]			
43h	—		PLH2_LEN[5:0]					
44h	DEVADDR[7:0]							
45h	DEVADDR[15:8]							
46h	DEVADDR[23:16]							

Addr.	Bit							
	7	6	5	4	3	2	1	0
47h	DEVADDR[31:24]							
48h	DEVADDR[39:32]							
49h	DEVADDR[47:40]							
4Ah	L2RXTO_F	L2RXREQ_F	—				IRQ_L2RX	IRQ_L2TX
4Bh	WLADDR[7:0]							
4Ch	WLADDR[15:8]							
4Dh	WLADDR[23:16]							
4Eh	WLADDR[31:24]							
4Fh	WLADDR[39:32]							
50h	WLADDR[47:40]							
51h	RXPLHT_FEN	RXADVSI_EN	WLA_FEN	—		RXADVNI_EN	RXADVDI_EN	RXADVI_EN
52h	TRXIS_PRD[7:0]							
53h	RTXIS_PRD[7:0]							
54h	—							WLTXA
61h	—	GIO2S[2:0]			—			
62h	—	SDAPU	SCLPU	—			GIO2PU	—

Note that for the addresses which are not listed in this table, it is suggested not to change their initial values.

The recommended values registers are listed below:

Addr.	Value	Addr.	Value
00h	27h @ TX; 25h @ RX	25h	F2h
02h	F0h	26h	4Bh
0Ch	15h	27h	7Fh
0Fh	00h @ TX; E4h @ RX	28h	C7h
10h	00	29h	B0h
11h	70h	2Ah	18h
14h	17h	2Bh	4Ch
18h	01h	2Ch	02h
19h	1Eh	35h	80h
1Ah	AAh	36h	36h
1Bh	6Eh	55h	61h
1Eh	84h	60h	8Fh
22h	2Fh	70h	03h
23h	03h	71h	03h @ TX; 01h @ RX
24h	10h	72h	01h

Output power setting:

Addr.	>5dBm	5dBm	2dBm	0dBm	-5dBm	-10dBm
31h	7Eh	7Dh	6Ch	F7h	CEh	CCh
32h	FAh	F9h	F8h	F3h	F8h	E8h

Addr.	Bit	7	6	5	4	3	2	1	0
03h	Name	PDUDATA[7:0]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **PDUDATA[7:0]**: PDU data FIFO read and write port

Addr.	Bit	7	6	5	4	3	2	1	0
04h	Name	RSTPDUFF	—						
	R/W	R/W	—						
	POR	0	0	0	0	0	0	0	0

Bit 7 **RSTPDUFF**: Reset PDU data FIFO, automatically cleared after completion

Bit 6~0 Reserved bits, cannot be changed

Addr.	Bit	7	6	5	4	3	2	1	0
05h	Name	WHTSDS	WHTSD[6:0]						
	R/W	R/W	R/W						
	POR	0	1	1	1	0	1	1	1

Bit 7 **WHTSDS**: Whitening seed selection

0: From channel number

1: From the WHTSD[6:0] bits

Whitening: polynomial $g(X)=X^7+X^4+1$

Bit 6~0 **WHTSD[6:0]**: Whitening seed

The WHTSD[4:0] bits are also acting as the random delay seed.

Addr.	Bit	7	6	5	4	3	2	1	0
06h	Name	PKT_AUTORS[7:0]							
	R/W	R/W							
	POR	1	1	1	1	1	1	1	1

Bit 7~0 **PKT_AUTORS[7:0]**: Packet event auto-resend times

00h: No resend, auto-resend disabled

01h: Resend 1 time

02h: Resend 2 times

...

FFh: Always resend until L2TX_START=0

Addr.	Bit	7	6	5	4	3	2	1	0
07h	Name	APRD_PDTH[1:0]		RNDDLY_EN	PKT_APRD[4:0]				
	R/W	R/W		R/W	R/W				
	POR	0	0	1	1	0	1	1	1

Bit 7~6 **APRD_PDTH[1:0]**: Auto power down threshold

00: 1ms

01: 1.5ms

10: 2ms

11: 3ms

These bits define the time threshold that the device should automatically power down, i.e. enter the Deep Sleep mode. The device will not enter the Deep Sleep mode if the automatic retransmission interval defined by PKT_APRD[4:0] is less than the automatic power down threshold defined by APRD_PDTH[1:0].

Bit 5 **RNDDLY_EN**: Enable random delay (250~8000μs) per advertising event period

0: Disable

1: Enable

Bit 4~0 **PKT_APRD[4:0]**: Packet format auto-resend delay

00000: 250μs

00001: 500μs

00010: 750μs

…

11111: 8000μs (8ms)

Addr.	Bit	7	6	5	4	3	2	1	0
08h	Name	PKT_PERIODS[7:0]							
	R/W	R/W							
	POR	0	1	1	0	0	0	1	1

Bit 7~0 **PKT_PERIODS[7:0]**: Advertising event transmit period low byte

Addr.	Bit	7	6	5	4	3	2	1	0
09h	Name	—	—	—	—	—	—	PKT_PERIODS[9:8]	
	R/W	—	—	—	—	—	—	R/W	
	POR	0	0	0	0	0	0	0	0

Bit 7~2 Reserved bits, cannot be changed

Bit 1~0 **PKT_PERIODS[9:8]**: Advertising event transmit period high byte

Period=10ms×(1+PKT_PERIODS[9:0]); range: 10ms (000h) ~ 10240ms (3FFh)

Addr.	Bit	7	6	5	4	3	2	1	0
0Bh	Name	L2RSP_EN	—	L2RX_START	L2TX_START	—	HOP_FNO[2:0]		
	R/W	R/W	—	R/W	R/W	—	R/W		
	POR	0	0	0	0	0	1	1	1

Bit 7 **L2RSP_EN**: RF layer 2 responds enable

0: Disable

1: Enable

Bit 6 Reserved bit, cannot be changed

Bit 5 **L2RX_START**: RF layer 2 reception start control

0: RF layer 2 reception stops

1: RF layer 2 reception starts

This bit will be cleared to zero by hardware when the reception is completed.

Bit 4 **L2TX_START**: RF layer 2 transmission start control

0: RF layer 2 transmission stops

1: RF layer 2 transmission starts

This bit will be cleared to zero by hardware when the transmission is completed.

Bit 3 Reserved bit, cannot be changed

Bit 2~0 **HOP_FNO[2:0]**: Hopping frequency number

HOP_FNO[0]: Enable channel 37 (2402MHz)

HOP_FNO[1]: Enable channel 38 (2426MHz)

HOP_FNO[2]: Enable channel 39 (2480MHz)

It is not recommended to set these bits to “000”. Ensure that there is at least one channel enabled. Do not set the L2TX_START/L2RX_START bit high when the HOP_FNO[2:0] bits are “000”. The L2TX_START bit and L2RX_START bit cannot be set high in the same time.

Addr.	Bit	7	6	5	4	3	2	1	0
15h	Name	FSCALE[7:0]							
	R/W	R/W							
	POR	1	1	1	1	1	1	1	1

Bit 7~0 **FSCALE[7:0]**: Frequency deviation scale parameter low byte

Addr.	Bit	7	6	5	4	3	2	1	0
16h	Name	FSCALE[15:8]							
	R/W	R/W							
	POR	0	0	0	0	0	1	1	1

Bit 7~0 **FSCALE[15:8]**: Frequency deviation scale parameter high byte

FSCALE[15:0]=(FD/f_{XTAL})×2^{19}-1

For example: DR (Data Rate)=1Mbps, FD=250kHz, FSCALE[15:0]=(250kHz/32MHz)×2^{19}-1=7FFh.

Addr.	Bit	7	6	5	4	3	2	1	0
17h	Name	FD_HOLD[7:0]							
	R/W	R/W							
	POR	0	0	1	1	0	0	0	0

Bit 7~0 **FD_HOLD[7:0]**: Frequency deviation threshold

Addr.	Bit	7	6	5	4	3	2	1	0
39h	Name	ACCESS_ADDR[7:0]							
	R/W	R/W							
	POR	1	1	0	1	0	1	1	0

Bit 7~0 **ACCESS_ADDR[7:0]**: BLE access address bit 7 ~ bit 0

Addr.	Bit	7	6	5	4	3	2	1	0
3Ah	Name	ACCESS_ADDR[15:8]							
	R/W	R/W							
	POR	1	0	1	1	1	1	1	0

Bit 7~0 **ACCESS_ADDR[15:8]**: BLE access address bit 15 ~ bit 8

Addr.	Bit	7	6	5	4	3	2	1	0
3Bh	Name	ACCESS_ADDR[23:16]							
	R/W	R/W							
	POR	1	0	0	0	1	0	0	1

Bit 7~0 **ACCESS_ADDR[23:16]**: BLE access address bit 23 ~ bit 16

Addr.	Bit	7	6	5	4	3	2	1	0
3Ch	Name	ACCESS_ADDR[31:24]							
	R/W	R/W							
	POR	1	0	0	0	1	1	1	0

Bit 7~0 **ACCESS_ADDR[31:24]**: BLE access address bit 31 ~ bit 24

Addr.	Bit	7	6	5	4	3	2	1	0
3Dh	Name	—	—	—	—	—	—	L2RXTO_EN	—
	R/W	—	—	—	—	—	—	R/W	—
	POR	0	0	0	0	0	0	1	0

Bit 7~2 Reserved bits, cannot be changed

Bit 1 **L2RXTO_EN**: Layer 2 RX time-out control

0: Disable

1: Enable

Bit 0 Reserved bit, cannot be changed

Addr.	Bit	7	6	5	4	3	2	1	0
3Eh	Name	—	—	—	—	L2RXTO_PRD[3:0]			
	R/W	—	—	—	—	R/W			
	POR	0	0	0	0	0	0	1	1

Bit 7~4 Reserved bits, cannot be changed

Bit 3~0 **L2RXTO_PRD[3:0]**: Layer 2 continuous RX time-out period

Period=250μs×(1+L2RXTO_PRD[3:0]).

Addr.	Bit	7	6	5	4	3	2	1	0
3Fh	Name	—	—	PMLEN	WHT_EN	PLTEN	PDUD_RS	FIFO_SEL	BKMODE
	R/W	—	—	R/W	R/W	R/W	R/W	R/W	R/W
	POR	0	0	0	1	0	0	0	0

Bit 7~6 Reserved bits, cannot be changed

Bit 5 **PMLEN**: Preamble length selection

0: 1 byte

1: 2 bytes

Bit 4 **WHT_EN**: Whitening enable control

0: Disable

1: Enable

Bit 3 **PLTEN**: Payload test enable

0: Disable

1: Enable

All data are from FIFO and bypass all the packet format setting. The PDU length is defined by the PLH1_LEN[5:0] bits.

Bit 2 **PDUD_RS**: PDU data read selection

0: Read register data

1: Read receiver data

Bit 1 **FIFO_SEL**: I^2C FIFO R/W selection

0: FIFO0

1: FIFO1

Bit 0 **BKMODE**: Beacon mode selection

0: Broadcaster mode

1: Scanner mode

Addr.	Bit	7	6	5	4	3	2	1	0
40h	Name	PLH1_RXA	PLH1_TXA	—	—	PLH1_TYPE[3:0]			
	R/W	R/W	R/W	—	—	R/W			
	POR	0	0	0	0	0	1	1	0

Bit 7 **PLH1_RXA**: Payload header RX address (RxADD)

Bit 6 **PLH1_TXA**: Payload header TX address (TxADD)

Bit 5~4 Reserved bits, cannot be changed

Bit 3~0 **PLH1_TYPE[3:0]**: Payload header type (PDU Type)

When the PDUD_RS=1, PDU read the data from the receiver.

PLH1_TYPE[3:0]=PLH1_RCV[3:0]

PLH1_TXA=PLH1_TXA_RCV

PLH1_RXA=PLH1_RXA_RCV

Note: Layer 2 TX (work in the PDU type)=ADV_NONCONN_IND (PLH1_TYPE=0x2), clear the L2RSP_EN to 0.

Addr.	Bit	7	6	5	4	3	2	1	0
41h	Name	—	—	PLH1_LEN[5:0]					
	R/W	—	—	R/W					
	POR	0	0	1	0	0	1	0	1

Bit 7~6 Reserved bits, cannot be changed

Bit 5~0 **PLH1_LEN**: Payload header length

When the PDUD_RS=1, PDU read the data from the receiver. PLH1_LEN[5:0]=PLH1_LEN_RCV[5:0].

Addr.	Bit	7	6	5	4	3	2	1	0
42h	Name	PLH2_RXA	PLH2_TXA	—	—	PLH2_TYPE[3:0]			
	R/W	R/W	R/W	—	—	R/W			
	POR	0	0	0	0	0	1	0	0

Bit 7 **PLH2_RXA**: Payload header RX address (RxADD) for phase

Bit 6 **PLH2_TXA**: Payload header TX address (TxADD) for phase

Bit 5~4 Reserved bits, cannot be changed

Bit 3~0 **PLH2_TYPE[3:0]**: Payload header type (PDU Type) for phase

When the PDUD_RS=1, PDU read the data from the receiver.

PLH2_TYPE[3:0]=PLH2_RCV[3:0]

PLH2_TXA=PLH2_TXA_RCV

PLH2_RXA=PLH2_RXA_RCV

Addr.	Bit	7	6	5	4	3	2	1	0
43h	Name	—	—	PLH2_LEN[5:0]					
	R/W	—	—	R/W					
	POR	0	0	1	0	0	1	0	1

Bit 7~6 Reserved bits, cannot be changed

Bit 5~0 **PLH2_LEN**: Payload header length for phase

When the PDUD_RS=1, PDU read the data from the receiver. PLH2_LEN[5:0]=PLH2_LEN_RCV[5:0].

Addr.	Bit	7	6	5	4	3	2	1	0
44h	Name	DEVADDR[7:0]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **DEVADDR[7:0]**: Device address bit 7 ~ bit 0

Addr.	Bit	7	6	5	4	3	2	1	0
45h	Name	DEVADDR[15:8]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **DEVADDR[15:8]**: Device address bit 15 ~ bit 8

Addr.	Bit	7	6	5	4	3	2	1	0
46h	Name	DEVADDR[23:16]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **DEVADDR[23:16]**: Device address bit 23 ~ bit 16

Addr.	Bit	7	6	5	4	3	2	1	0
47h	Name	DEVADDR[31:24]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **DEVADDR[31:24]**: Device address bit 31 ~ bit 24

Addr.	Bit	7	6	5	4	3	2	1	0
48h	Name	DEVADDR[39:32]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **DEVADDR[39:32]**: Device address bit 39 ~ bit 32

Addr.	Bit	7	6	5	4	3	2	1	0
49h	Name	DEVADDR[47:40]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **DEVADDR[47:40]**: Device address bit 47 ~ bit 40
When the PDUD_RS bit is high, DEVADDR[47:0]=DEVADDR_RCV[47:0].

Addr.	Bit	7	6	5	4	3	2	1	0
4Ah	Name	L2RXTO_F	L2RXREQ_F	—	—	—	—	IRQ_L2RX	IRQ_L2TX
	R/W	R/W	R/W	—	—	—	—	R/W	R/W
	POR	0	0	0	0	0	0	0	0

Bit 7 **L2RXTO_F**: The second RX time-out flag when layer 2 RX is completed. It will be cleared when the next Layer 2 RX starts

Bit 6 **L2RXREQ_F**: The recievied SCAN_REQ flag when layer 2 RX complete. It will be cleared when the next Layer 2 TX starts

Bit 5~2 Reserved bits, cannot be changed

Bit 1 **IRQ_L2RX**: Layer 2 RX complete IRQ. When user read the IRQ, wirte 1 to clear the IRQ

Bit 0 **IRQ_L2TX**: Layer 2 TX complete IRQ. When user read the IRQ, wirte 1 to clear the IRQ

Addr.	Bit	7	6	5	4	3	2	1	0
4Bh	Name	WLADDR[7:0]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **WLADDR[7:0]**: White list device address bit 7 ~ bit 0

Addr.	Bit	7	6	5	4	3	2	1	0
4Ch	Name	WLADDR[15:8]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **WLADDR[15:8]**: White list device address bit 15 ~ bit 8

Addr.	Bit	7	6	5	4	3	2	1	0
4Dh	Name	WLADDR[23:16]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **WLADDR[23:16]**: White list device address bit 23 ~ bit 16

Addr.	Bit	7	6	5	4	3	2	1	0
4Eh	Name	WLADDR[31:24]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **WLADDR[31:24]**: White list device address bit 31 ~ bit 24

Addr.	Bit	7	6	5	4	3	2	1	0
4Fh	Name	WLADDR[39:32]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **WLADDR[39:32]**: White list device address bit 39 ~ bit 32

Addr.	Bit	7	6	5	4	3	2	1	0
50h	Name	WLADDR[47:40]							
	R/W	R/W							
	POR	0	0	0	0	0	0	0	0

Bit 7~0 **WLADDR[47:40]**: White list device address bit 47 ~ bit 40

Addr.	Bit	7	6	5	4	3	2	1	0
51h	Name	RXPLHT_FEN	RXADVSI_EN	WLA_FEN	—	—	RXADVNI_EN	RXADVDI_EN	RXADVI_EN
	R/W	R/W	R/W	R/W	—	—	R/W	R/W	R/W
	POR	1	1	0	0	0	1	0	1

Bit 7 **RXPLHT_FEN**: Payload header type filtering
0: Receive all PDU type
1: Receive ADV_DIRECT_IND, ADV_NONCONN_IND, ADV_SCAN_IND and ADV_IND type only

Bit 6 **RXADVSI_EN**: Enable "ADV_SCAN_IND" PDU type only

Bit 5 **WLA_FEN**: Enable receiving white list device address filtering

Bit 4~3 Reserved bits, cannot be changed

Bit 2 **RXADVNI_EN**: Enable "ADV_NONCONN_IND" PDU type only

Bit 1 **RXADVDI_EN**: Enable "ADV_DIRECT_IND" PDU type only

Bit 0 **RXADVI_EN**: Enable "ADV_IND" PDU type only

Addr.	Bit	7	6	5	4	3	2	1	0
52h	Name	TRXIS_PRD[7:0]							
	R/W	R/W							
	POR	0	0	1	0	0	1	1	1

Bit 7~0 **TRXIS_PRD[7:0]**: TX to RX period delay time in layer 2
The time=(TRXIS_PRD[7:0]+1)×1μs.

Addr.	Bit	7	6	5	4	3	2	1	0
53h	Name	RTXIS_PRD[7:0]							
	R/W	R/W							
	POR	0	1	1	0	0	0	1	1

Bit 7~0 **RTXIS_PRD[7:0]**: RX to TX period delay time in layer 2
The time=(RTXIS_PRD[7:0]+1)×1μs.

Addr.	Bit	7	6	5	4	3	2	1	0
54h	Name	—	—	—	—	—	—	—	WLTXA
	R/W	—	—	—	—	—	—	—	R/W
	POR	0	0	0	0	0	0	0	0

Bit 7~1 Reserved bits, cannot be changed

Bit 0 **WLTXA**: White list address type
0: Public address
1: Random address

Addr.	Bit	7	6	5	4	3	2	1	0
61h	Name	—	GIO2S[2:0]			—	—	—	—
	R/W	—	R/W			—	—	—	—
	POR	0	0	0	0	0	0	0	0

Bit 7 Reserved bit, cannot be changed

Bit 6~4 **GIO2S[2:0]**: GIO2 pin function selection

000: No function, input

001: FSYCK output

110: IRQ_L2ACT output

111: L2TX_START output or L2RX_START output

Others: Reserved

Bit 3~0 Reserved bits, cannot be changed

Addr.	Bit	7	6	5	4	3	2	1	0
62h	Name	—	SDAPU	SCLPU	—	—	—	GIO2PU	—
	R/W	—	R/W	R/W	—	—	—	R/W	—
	POR	0	1	1	1	1	1	1	1

Bit 7 Reserved bit, cannot be changed

Bit 6 **SDAPU**: SDA pin function pull-high enable control

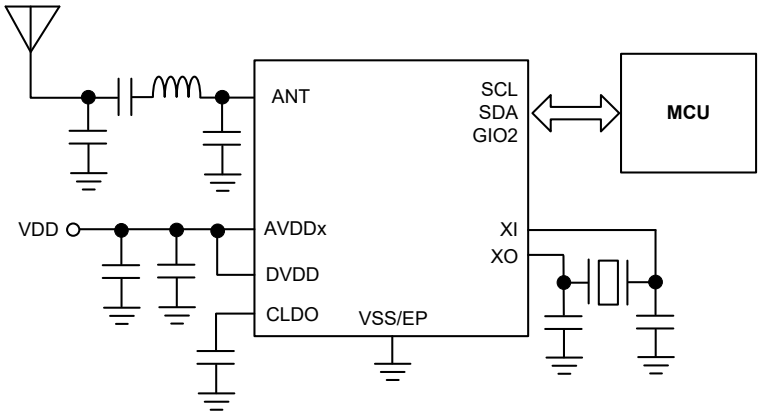
Bit 5 **SCLPU**: SCL pin function pull-high enable control

Bit 4~2 Reserved bits, cannot be changed

Bit 1 **GIO2PU**: GIO2 pin function pull-high enable control

Bit 0 Reserved bit, cannot be changed

Application Circuits



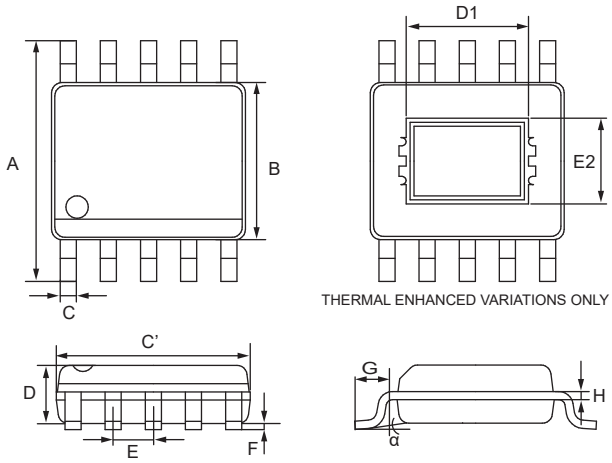
Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Meterials Information
- Carton information

10-pin SOP-EP (150mil) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	—	0.236 BSC	—
B	—	0.154 BSC	—
C	0.012	—	0.018
C′	—	0.193 BSC	—
D	—	—	0.069
D1	0.102	—	0.126
E	—	0.039 BSC	—
E2	0.071	—	0.090
F	0.000	—	0.006
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	—	6.00 BSC	—
B	—	3.90 BSC	—
C	0.30	—	0.45
C′	—	4.90 BSC	—
D	—	—	1.75
D1	2.59	—	3.20
E	—	1.00 BSC	—
E2	1.81	—	2.28
F	0.00	—	0.15
G	0.40	—	1.27
H	0.10	—	0.25
α	0°	—	8°