

**Enhanced Octal ARINC 429 Receiver
with Label Recognition and SPI Interface**

August, 2022

GENERAL DESCRIPTION

The HI-35981 from Holt Integrated Circuits interfaces up to eight ARINC 429 receive buses to a high-speed Serial Peripheral Interface (SPI) enabled microcontroller. The device is an enhanced version of Holt's well-established HI-35980 (HI-3598) family, with additional features and functionality. The user-programmable label filtering capability has been expanded from 16 labels to all 256 labels, and the 4-word deep receive FIFO has been increased to 32 words deep. Also, a 32-word deep transmit FIFO has been added, significantly increasing the transmit capability from the single-word buffer on the existing device. The digital transmit channel has a digital output pin to set the data rate on an external line driver, such as Holt's lightning-protected HI-8597 or galvanically isolated HI-8598.

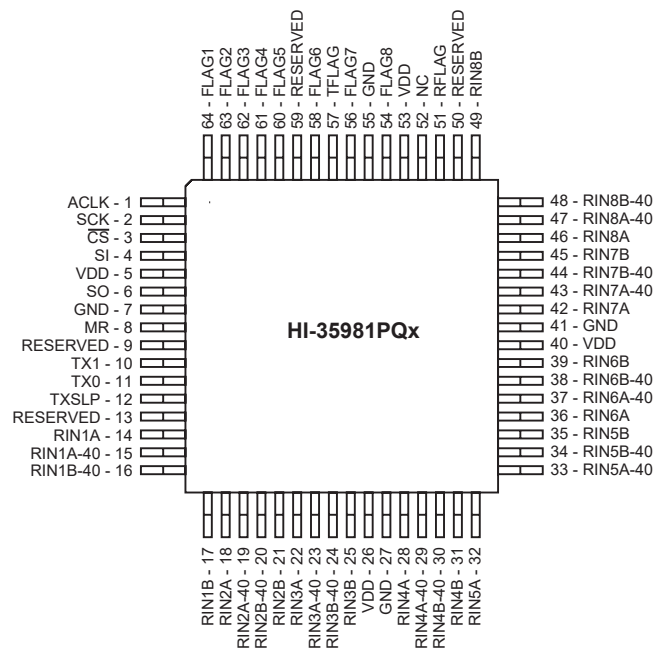
Each channel has an on-chip analog line receiver. Two choices of receiver input are available for each channel, each with different input resistance values to provide flexibility when using external lightning protection circuitry. Receive FIFO status can be monitored using the programmable external interrupt pins, or by polling the status register. Other features include the ability to switch the bit-significance of the ARINC 429 label and to recognize the 32nd received ARINC bit as either data or a parity flag. The SPI and all control signals are CMOS and TTL compatible and support 3.3V or 5V operation.

FEATURES

- ARINC 429 compliant
- Up to 8 independent receive channels
- 32-Word receive FIFO for each channel
- Op code readable receive FIFO message counts allows for more efficient FIFO unloading
- Digital transmit channel with slew rate control
- 32-Word transmit FIFO
- 3.3V or 5.0V logic supply operation
- On-chip analog line receivers connect directly to ARINC 429 bus
- Programmable label recognition for 256 labels per channel
- Independent data rate selection for each receiver

- Four-wire SPI interface
- Label bit-order control
- 32nd bit can be data or parity
- Low Power
- Industrial & extended temperature ranges

PIN CONFIGURATION (TOP VIEW)



BLOCK DIAGRAM

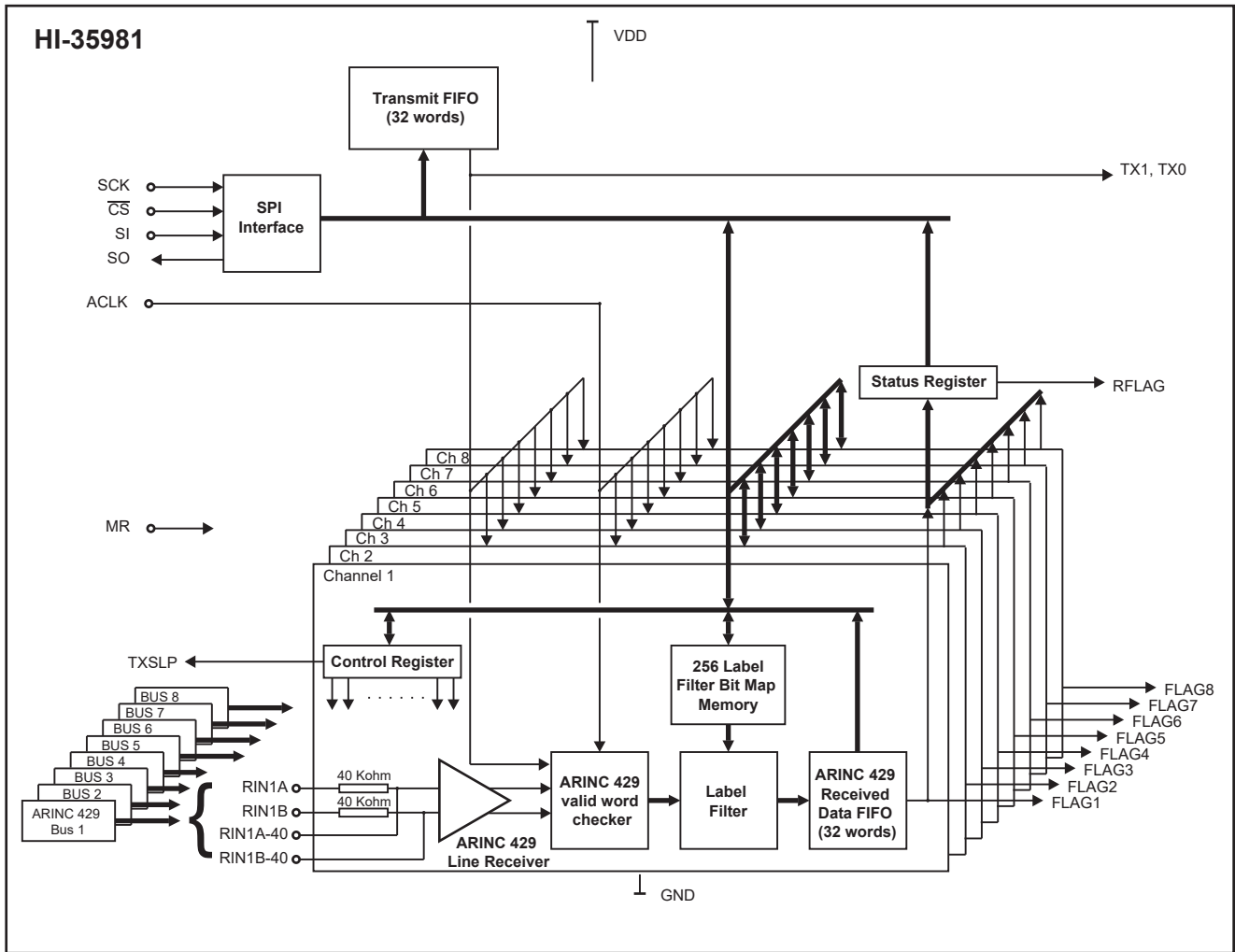


Figure 1. HI-35981 Block Diagram

PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin	Function	Description
VDD	POWER	3.3V or 5.0V power supply.
GND	POWER	Chip 0V supply.
\overline{CS}	INPUT	Chip select. Data is shifted into SI and out of SO when \overline{CS} is low.
SCK	INPUT	SPI Clock. Data is shifted into or out of the SPI interface using SCK.
SI	INPUT	SPI interface serial data input.
SO	OUTPUT	SPI interface serial data output.
ACLK	INPUT	Master 1 MHz timing reference for the ARINC 429 receiver and transmitter.
RIN1A – RIN8A	ARINC INPUT	ARINC 429 receiver positive input. Direct connection to ARINC 429 bus.
RIN1B – RIN8B	ARINC INPUT	ARINC 429 receiver negative input. Direct connection to ARINC 429 bus.
RIN1A-40 – RIN8A-40	ARINC INPUT	Alternate ARINC 429 receiver positive input. Requires external 40K Ω resistor.
RIN1B-40 – RIN8B-40	ARINC INPUT	Alternate ARINC 429 receiver negative input. Requires external 40K Ω resistor.
FLAG1 – FLAG8	OUTPUT	Goes high when specified ARINC 429 receiver FIFO is not empty (CR1=0), or full (CR1=1).
RFLAG	OUTPUT	Logical OR of FLAG1 through FLAG8.
TFLAG	OUTPUT	Goes high when ARINC 429 Transmit FIFO is empty (CR13=0), or full (CR13=1).
TX1	OUTPUT	ARINC 429 word ONE state digital output.
TX0	OUTPUT	ARINC 429 word ZERO state digital output.
TXSLP	OUTPUT	Set data rate on external line driver. Logic “1” = 100 kbps (High speed) Logic “0” = 12 – 14.5 kbps (Low speed).
MR	INPUT	Hardware active high Master Reset. Clears all receivers and FIFOs. Does not affect Control Register contents.

SPI INSTRUCTIONS

Instruction op codes are used to read, write and configure the HI-35981 via the SPI interface. The instruction format is illustrated in Figure 2. When \overline{CS} goes low, the next 8 clocks at the SCK pin shift an instruction op code into the decoder, starting with the first rising edge. The op code is fed into the SI pin, most significant bit first.

For write instructions, the most significant bit of the data word must immediately follow the instruction op code and is clocked into its register on the next rising SCK edge. Data word length varies depending on word type written, see Table 2.

For read instructions, the most significant bit of the requested data word appears at the SO pin after the last op code bit is clocked into the decoder, at the next falling SCK edge. As in write instructions, the data field bit-length varies with read instruction type.

Channel-specific instructions use the upper four bits to specify an ARINC 429 receiver channel, 1 – 8. The lower four bits specify the op code, described in Table 2. The four channel assignment bits are “don’t care” for instructions that are not channel-specific, such as Master Reset. In Table 2, we use the programming convention of designating hexadecimal values 0 – 9 and A – F using the “0x” prefix. Hexadecimal 0x0 – 0xF corresponds to decimal values 0 – 15.

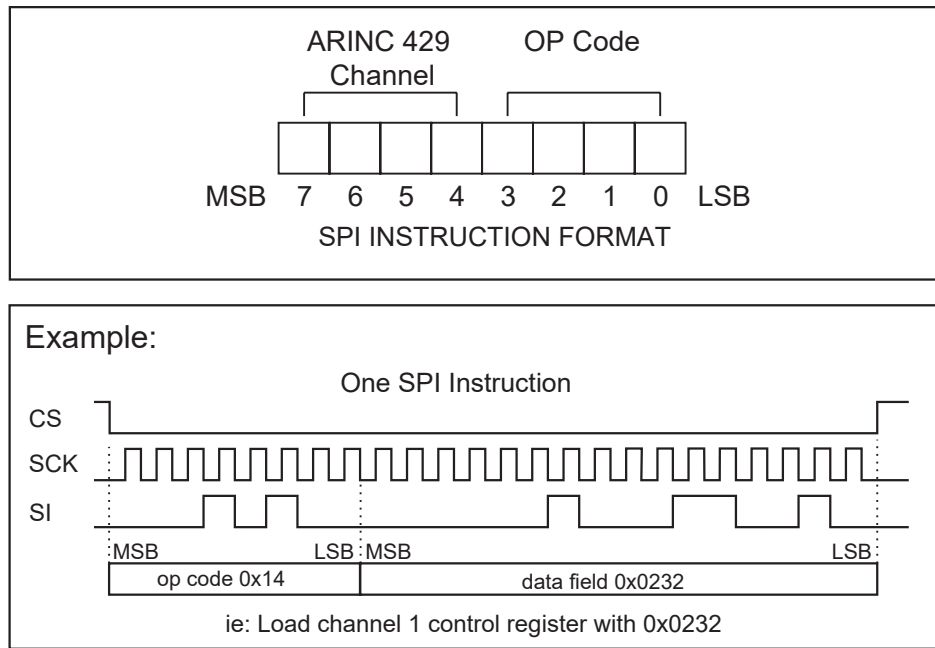


Figure 2. SPI Instruction Format

Table 2. Defined Instructions (Op Codes)

Upper Nibble (ARINC 429 Channel)	Lower Nibble (OP CODE)	DATA FIELD	Description
0x0	0x0	64 bits	Read all receive FIFO message counts. Each successive byte represents the message count in receiver 1 FIFO thru' receiver 8 FIFO respectively.
0x1 – 0x8	0x0	8 bits	Read receive FIFO message count for specified channel.
0x9	0x0	8 bits	Read transmit FIFO message count.
0x1 – 0x8	0x1	256 bits	<p>Write label acceptance filter for specified channel.</p> <p>The user loads a 256-bit label look-up table for each channel to specify which 8-bit incoming ARINC labels are captured by the receiver and stored in its FIFO, and which are discarded.</p> <p>Writing a “0” in the look-up table will filter the label in that bit position (255 to 0 Dec). This label will be ignored and received ARINC words containing the label will not be recorded in the Rx FIFO.</p> <p>Writing a “1” will turn off filtering for the label in that bit position (255 to 0 Dec) and received ARINC words containing the label will be stored in the Rx FIFO.</p> <p>The look-up table bits are loaded via the SPI data field, with the first bit following the SPI op code corresponding to label 255 Dec and so on down to the LSB corresponding to label 0 Dec.</p> <p>Label Recognition is enabled for each channel by setting bit CR2 = “1” in the channel’s Control Register.</p> <p>See Section “Label Recognition”.</p>
0x1 – 0x8	0x2	256 bits	Read label filter bit map memory for specified channel.
0x1 – 0x8	0x3	32 x N bits	Read the receive FIFO for specified channel. N is the number of 32-bit ARINC 429 words. If the FIFO is empty all zeros will be read.
0x1 – 0x8	0x4	16 bits	Load the specified channel’s Control Register and clear that channel’s FIFO.
0x1 – 0x8	0x5	16 bits	Read the specified channel’s Control Register.
X	0x6	32 bits	Read the Status Register.
X	0x7	None	Master Reset (All channels).
X	0x8	32 x N bits	<p>Write Tx FIFO (High-speed data rate). N is the number of 32-bit ARINC 429 words.</p> <p>This can also be used as a test word for each receiver (Loopback self-test).</p>

HI-35981

Upper Nibble (ARINC 429 Channel)	Lower Nibble (OP CODE)	DATA FIELD	Description
X	0x9	32 x N bits	Write Tx FIFO (Low-speed data rate). N is the number of 32-bit ARINC 429 words. This can also be used as a test word for each receiver (Loopback self-test).
X	0xA	None	Reset Tx FIFO.
X	0xB	None	Tx FIFO Transmit Start (Note: Control Register bit CR14 = "0". If CR14 = "1", the Tx FIFO will start transmitting when it has data).
0x0	0xC	None	Reset all bits in label look-up table for all Rx channels. This op code will write "zeros" to all locations of the 256-bit label look-up table for each of the 8 Rx channels. All 256 ARINC 429 labels for every channel will be rejected and not recorded in the Rx FIFOs. Label recognition must be enabled by setting CR2 = "1" in the Control Register.
0x1 – 0x8	0xC	None	Reset all bits in label look-up table for specified Rx channel. This op code will write "zeros" to all locations of the 256-bit label look-up table for the specified Rx channel. All 256 ARINC 429 labels for the specified channel will be rejected and not recorded in the Rx FIFO. Label recognition must be enabled by setting CR2 = "1" in the Control Register.
0x0	0xD	None	Set all bits in label look-up table for all Rx channels. This op code will write "ones" to all locations of the 256-bit label look-up table for each of the 8 Rx channels. All 256 ARINC 429 labels for every channel will be accepted and recorded in the Rx FIFOs. Label recognition must be enabled by setting CR2 = "1" in the Control Register.
0x1 – 0x8	0xD	None	Set all bits in label look-up table for specified Rx channel. This op code will write "ones" to all locations of the 256-bit label look-up table for the specified Rx channel. All 256 ARINC 429 labels for the specified channel will be accepted and recorded in the Rx FIFO. Label recognition must be enabled by setting CR2 = "1" in the Control Register.

HI-35981

Upper Nibble (ARINC 429 Channel)	Lower Nibble (OP CODE)	DATA FIELD	Description
0x1 – 0x8	0xE	8 bits	<p>Reset specific bit in label look-up table for specified Rx channel.</p> <p>This op code will write a “zero” to the location of the specified label in the label look-up table (for the specified Rx channel).</p> <p>The specific label is specified in binary in the 8-bit data field. This label will be rejected and not recorded in the Rx FIFO.</p> <p>Label recognition must be enabled by setting CR2 = “1” in the Control Register.</p>
0x1 – 0x8	0xF	8 bits	<p>Set specific bit in label look-up table for specified Rx channel.</p> <p>This op code will write a “one” to the location of the specified label in the label look-up table (for the specified Rx channel).</p> <p>The specific label is specified in binary in the 8-bit data field. When received, it will be accepted and recorded in the Rx FIFO.</p> <p>Label recognition must be enabled by setting CR2 = “1” in the Control Register.</p>

FUNCTIONAL DESCRIPTION

Control Word Register for Receiver 1 and Transmitter

Each HI-35981 receive channel is assigned a 16-bit Control Register which configures that receiver. Control Register bits CR15 - CR0 are loaded from a 16-bit data value appended to SPI instruction 0xN4, where “N” is the channel number 1 – 8. Writing to the Control Register also clears the data FIFO for that channel. The Control Register contents may be read using SPI instruction 0xN5. Table 3 summarizes the Control Register bit functions for the digital Transmitter and Receiver 1. The Control Register for Receivers 2 – 8 is described in Table 4.

Table 3. Control Register Bits for Transmitter and Receiver 1

CR Bit	Function	State	Description
CR0 (LSB)	Receiver Data Rate Select	0	Data rate = ACLK/10 (ARINC 429 High-Speed).
		1	Data rate = ACLK/80 (ARINC 429 Low-Speed).
CR1	RFLAG Definition	0	RFLAG output will be high when Rx FIFO is not empty (Contains at least one word).
		1	RFLAG output will be high when Rx FIFO is full (32 words).
CR2	Enable Label Recognition	0	Label recognition disabled.
		1	Label recognition enabled.
CR3	Reset Receiver	0	Normal Operation.
		1	Reset this receiver (Clear receiver logic and FIFO). The receive channel is disabled if CR3 is left high.
CR4	Receiver Parity Check Enable	0	Receiver parity check disabled.
		1	Receiver odd parity check enabled.
CR5	Self-Test (Loopback)	0	Receiver’s inputs are connected to the Transmit FIFO serial data output.
		1	Normal operation.
CR6	Receiver Decoder	0	Receiver Decoder Disabled.
		1	Receiver Decoder Enabled. ARINC bits 10 and 9 must match CR7 and CR8.
CR7	-	-	If receiver decoder is enabled, the ARINC bit 10 must match this bit.
CR8	-	-	If receiver decoder is enabled, the ARINC bit 9 must match this bit.
CR9	ARINC Label Bit Order	0	Label bit order reversed (See Table 6).
		1	Label bit order same as received (See Table 6)
CR10	Transmitter Parity Bit Enable	0	Disabled. Bit 32 is data.
		1	Enabled. Bit 32 is parity.
CR11	Transmitter Parity Select	0	Odd parity.
		1	Even parity.
CR12	Transmitter Disable	0	Enable.
		1	Disable (forces outputs to null state).

HI-35981

CR Bit	Function	State	Description
CR13	TFLAG Definition	0	TFLAG output will be high when Tx FIFO is empty.
		1	TFLAG output will be high when Tx FIFO is full.
CR14	Tranmitter Start Mode	0	Start transmission by SPI opcode 0x0B.
		1	Start transmission when Tx FIFO has data.
CR15 (MSB)	RESERVED	1	Always reads logic "1".

Table 4. Control Register Bits for Receivers 2 – 8.

CR Bit	Function	State	Description
CR0 (LSB)	Receiver Data Rate Select	0	Data rate = ACLK/10 (ARINC 429 High-Speed).
		1	Data rate = ACLK/80 (ARINC 429 Low-Speed).
CR1	RFLAG Definition	0	RFLAG output will be high when Rx FIFO is not empty (Contains at least one word).
		1	RFLAG output will be high when Rx FIFO is full (32 words).
CR2	Enable Label Recognition	0	Label recognition disabled.
		1	Label recognition enabled.
CR3	Reset Receiver	0	Normal Operation .
		1	Reset this receiver (Clear receiver logic and FIFO). The receive channel is disabled if CR3 is left high.
CR4	Receiver Parity Check Enable	0	Receiver parity check disabled.
		1	Receiver odd parity check enabled.
CR5	Self-Test (Loopback)	0	Receiver's inputs are connected to the Transmit FIFO serial data output.
		1	Normal operation.
CR6	Receiver Decoder	0	Receiver Decoder Disabled.
		1	Receiver Decoder Enabled. ARINC bits 10 and 9 must match CR7 and CR8.
CR7	-	-	If receiver decoder is enabled, the ARINC bit 10 must match this bit.
CR8	-	-	If receiver decoder is enabled, the ARINC bit 9 must match this bit.
CR9	ARINC Label Bit Order	0	Label bit order reversed (See Table 6).
		1	Label bit order same as received (SeeTable 6).

Status Register

The HI-35981 device has a single 16-bit Status Register which is read to determine status for the eight received data FIFOs. The Status Register is read using SPI instruction 0x6. Table 5 summarizes the Status Register bits functions.

Table 5. Status Register Bits Functions

CR Bit	Function	State	Description
SR0 (LSB)	Receiver 1 FIFO Empty	0	Receiver 1 FIFO contains valid data. FLAG1 output will be high if CR1 = "0".
		1	Receiver 1 FIFO is empty (all data read). FLAG1 output will be low if CR1 = "0".
SR1	Receiver 2 FIFO Empty	0	Receiver 2 FIFO contains valid data. FLAG2 output will be high if CR1 = "0".
		1	Receiver 2 FIFO is empty (all data read). FLAG2 output will be low if CR1 = "0".
SR2 to SR06	Receiver 3 to Receiver 7 FIFO Empty	:	:
SR7	Receiver 8 FIFO Empty	0	Receiver 8 FIFO contains valid data FLAG8 output will be high if CR1 = "0".
		1	Receiver 8 FIFO is empty (all data read). FLAG8 output will be low if CR1 = "0".
SR8	Receiver 1 FIFO Full	0	Receiver 1 FIFO not full. FLAG1 output will be low if CR1 = "1".
		1	Receiver 1 FIFO full. FLAG1 output will be high if CR1 = "1". To avoid data loss, the FIFO must be read within one ARINC word period.
SR9	Receiver 2 FIFO Full	0	Receiver 2 FIFO not full. FLAG2 output will be low if CR1 = "1".
		1	Receiver 2 FIFO full. FLAG2 output will be high if CR1 = "1". To avoid data loss, the FIFO must be read within one ARINC word period.
SR10 to SR14	Receiver 3 to Receiver 7 FIFO Full	:	:

HI-35981

CR Bit	Function	State	Description
SR15 (MSB)	Receiver 8 FIFO Full	0	Receiver 8 FIFO not full. FLAG8 output will be low if CR1 = "1".
		1	Receiver 8 FIFO full. FLAG8 output will be high if CR1 = "1". To avoid data loss, the FIFO must be read within one ARINC word period.
SR16	Receiver 1 FIFO Half Full	0	Less than Half Full.
		1	At least Half Full.
SR17	Receiver 2 FIFO Half Full	0	Less than Half Full.
		1	At least Half Full.
SR18 to SR22	Receiver 3 to Receiver 7 FIFO Half Full	:	:
SR23	Receiver 8 FIFO Half Full	0	Less than Half Full.
		1	At least Half Full.
SR24	Tx FIFO Empty	0	Not empty. (Contains at least one word).
		1	Empty.
SR25	Tx FIFO Half Full	0	Less than Half Full.
		1	At least Half Full.
SR26	Tx FIFO Full	0	Not Full.
		1	Full.
SR27 to SR31	Not Used	0	Returns 0 when read.

ARINC 429 Data Format

Control Register bit CR9 controls how individual bits in the received ARINC word are mapped to the SPI data word during data read operations. Table 6 describes this mapping.

Table 6. SPI / ARINC bit-mapping

SPI / ARINC bit-mapping												
SPI Order	1	2 – 22	23	24	25	26	27	28	29	30	31	32
ARINC bit	32	31 – 11	10	9	1	2	3	4	5	6	7	8
CR9 = 0	Parity	Data	SDI	SDI	Label (MSB)	Label	Label	Label	Label	Label	Label	Label (LSB)
ARINC bit	32	31 – 11	10	9	8	7	6	5	4	3	2	1
CR9 = 1	Parity	Data	SDI	SDI	Label (LSB)	Label	Label	Label	Label	Label	Label	Label (MSB)

ARINC 429 Receiver

ARINC Bus Interface

Figure 3 shows the input circuit for each on-chip ARINC 429 line receiver. The ARINC 429 specification requires detection levels summarized in Table 7.

Table 7. ARINC 429 Detection Levels

STATE	DIFFERENTIAL VOLTAGE
ONE	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
ZERO	-6.5 Volts to -13 Volts

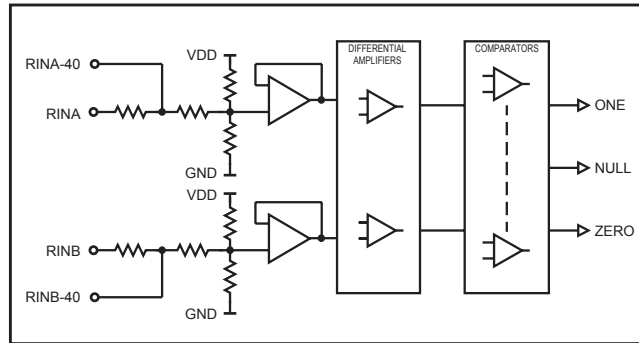


Figure 3. ARINC Receiver Input

The HI-35981 family guarantees recognition of these levels with a common mode Voltage with respect to GND less than $\pm 30V$ for the worst case condition (3.15V supply and 13V signal level).

The tolerances in the design guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the ARINC signal is out of the actual acceptance ranges, including the nulls, the chip rejects the data.

Bit Timing

The ARINC 429 specification defines timing tolerances for received data according to Table 8.

Table 8. ARINC 429 Receiver Timing Tolerances

	HIGH SPEED	LOW SPEED
Bit Rate	100 kbps \pm 1%	12K – 14.5 kbps
Pulse Rise Time	1.5 \pm 0.5 μ s	10 \pm 5 μ s
Pulse Fall Time	1.5 \pm 0.5 μ s	10 \pm 5 μ s
Pulse Width	5 μ s \pm 5%	34.5 to 41.7 μ s

Receiver Logic Operation

Figure 4 is a block diagram showing the logic for each receiver.

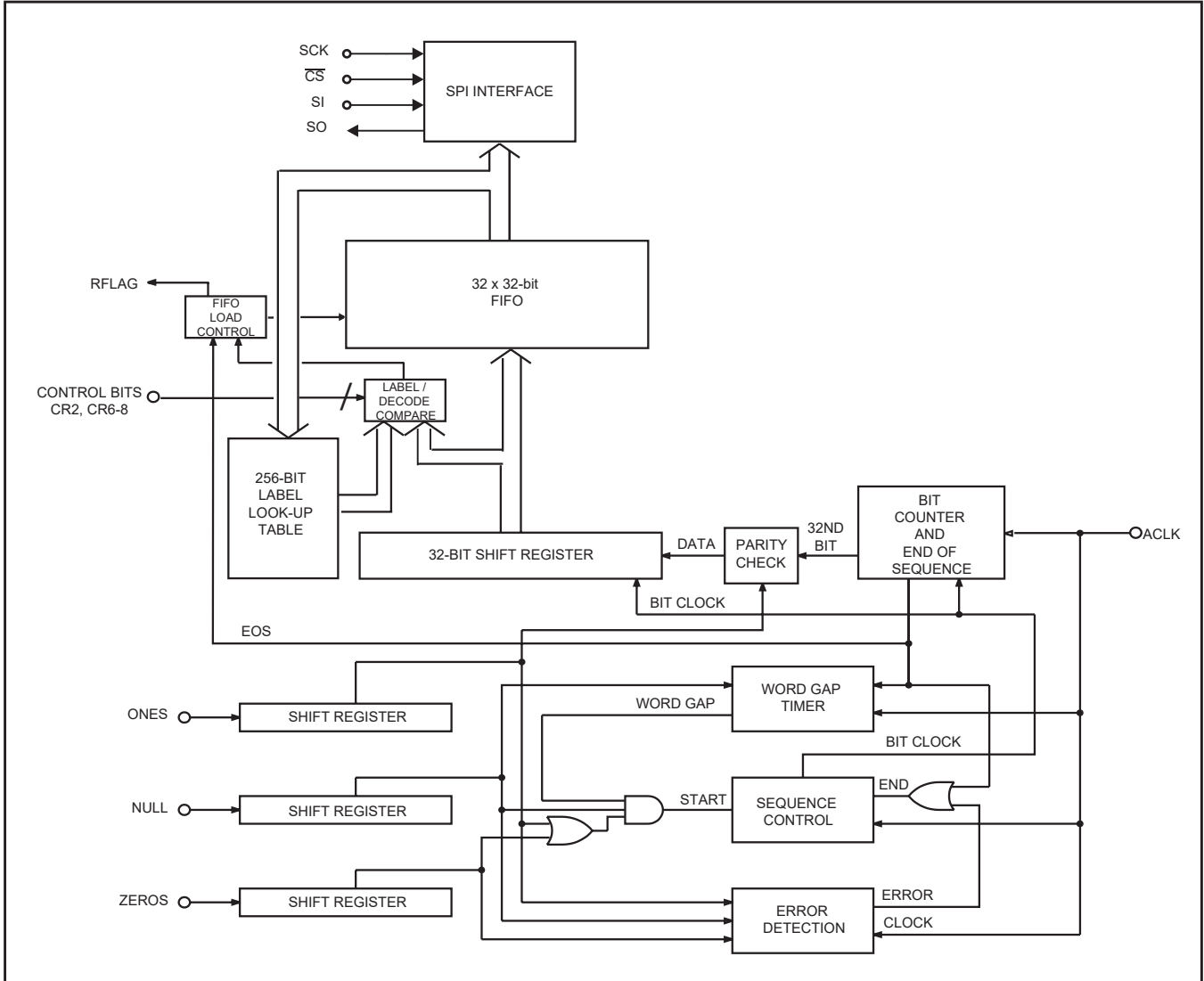


Figure 4. Receiver Block Diagram

The HI-35981 family accept signals within these tolerances and rejects signals outside these tolerances. Receiver logic achieves this as described below:

1. An accurate 1MHz clock source is required to validate the receive signal timing. Less than 0.1% error is recommended.
2. The receiver uses three separate 10-bit sampling shift registers for Ones detection, Zeros detection and Null detection. When the input signal is within the differential voltage range for any shift register's state (One, Zero or Null) sampling clocks a high bit into that register. When the receive signal is outside the differential voltage range defined for any shift register, a low bit is clocked. Only one shift register can clock a high bit for any given sample. All three registers clock low bits if the differential input voltage is between defined state voltage bands.

Valid data bits require at least three consecutive One or Zero samples (three high bits) in the upper half of the Ones or Zeros sampling shift register, and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register within the data bit interval.

A word gap Null requires at least three consecutive Null samples (three high bits) in the upper half of the Null sampling shift register and at least three consecutive Null samples (three high bits) in the lower half of the Null sampling shift register. This guarantees the minimum pulse width.

3. To validate the receive data bit rate, each bit must follow its preceding bit by not less than 8 samples and not more than 12 samples. With exactly 1MHz input clock frequency, the acceptable data bit rates are shown in Table 9.

Table 9. Acceptable Data Bit Rates at 1MHz Input Clock Frequency

	HIGH SPEED	LOW SPEED
Data Bit Rate Min	83Kbps	10.4Kbps
Data Bit Rate Max	125Kbps	15.6Kbps

4. Following the last data bit of a valid reception, the Word Gap timer samples the Null shift register every 10 input clocks (every 80 clocks for low speed). If a Null is present, the Word Gap counter is incremented. A Word Gap count of 3 enables the next reception.

Receiver Parity

The 32nd bit of received ARINC words stored in the receive FIFO is used as a Parity Flag indicating whether good Odd parity is received from the incoming ARINC word.

Odd Parity Received

The parity bit is reset to indicate correct parity was received and the resulting word is then written to the receive FIFO.

Even Parity Received

The receiver sets the 32nd bit to a "1", indicating a parity error and the resulting word is then written to the receive FIFO.

Therefore, the 32nd bit retrieved from the receiver FIFO will always be "0" when valid (odd parity) ARINC 429 words are received.

Retrieving Data

Once 32 valid bits are recognized, the receiver logic generates an End of Sequence (EOS). Depending on the state of Control Register bits CR2, CR6, CR7 and CR8, the received 32-bit ARINC word is then checked for correct decoding and label match before it is loaded into the 32 x 32 Receive FIFO. ARINC words that do not match required 9th and 10th ARINC bit and do not have a label match are ignored and are not loaded into the Receive FIFO. Table 10 describes this operation.

Table 10. FIFO Loading Control

CR2	ARINC word matches Enabled label	CR6	ARINC word bits 10, 9 match CR7, CR8	FIFO
0	X	0	X	Load FIFO
1	No	0	X	Ignore Data
1	Yes	0	X	Load FIFO
0	X	1	No	Ignore Data
0	X	1	Yes	Load FIFO
1	Yes	1	No	Ignore Data
1	No	1	Yes	Ignore Data
1	No	1	No	Ignore Data
1	Yes	1	Yes	Load FIFO

Once a valid ARINC word is loaded into the FIFO, the EOS signal clocks the Data Ready flip-flop to a “1”, and the corresponding channel’s Status Register FIFO Empty bit (SR0- SR7) goes to a “0”. The channel’s Empty bit remains low until the corresponding Receive FIFO is empty. Each received ARINC word is retrieved via the SPI interface using SPI instruction 0xN3, where “N” is the channel number 1 – 8.

Up to 32 ARINC words may be held in each channel’s Receive FIFO. The Status Register FIFO Full bit (SR8 - SR15) goes high when the corresponding channel’s Receive FIFO is full. Failure to offload a full Receive FIFO causes additional received valid ARINC words to overwrite the last received word.

Label Recognition

Each receive channel has the capability to filter (accept or reject) all 256 ARINC labels. The user loads a 256-bit label look-up table for each receive channel to specify which 8-bit incoming ARINC labels are captured by the receiver, and which are discarded. Setting a “1” in the look-up table enables processing of received ARINC words containing the corresponding label (255 to 0 Dec). A “0” in the look-up table causes rejection of received ARINC words containing the label. The 256-bit look-up table is loaded using SPI op code 0xN1 as described in Table 2, where “N” is the receiver channel number 1 – 8. The SPI data is written in reverse order, such that the first bit following the op code corresponds to label 255 Dec, and so on down to the LSB corresponding to label 0 Dec. After the look-up tables are initialized, set each receiver Control Register bit CR2 to enable label recognition for each channel. SPI op codes 0xNC, 0xND, 0xNE and 0xNF may also be used to set or reset individual or all bits in each receiver’s look-up table (see Table 2).

Reading the Label Memory

The contents of each channel’s Label Memory may be read via the SPI interface using instruction 0xN2, where “N” is the channel number 1 – 8, as described in Table 2.

Transmitter

Transmit FIFO

The Transmit FIFO is loaded with ARINC 429 words awaiting transmission. SPI op code 0x08 (for ARINC 429 high speed data rate) or 0x09 (for ARINC 429 low speed) writes up to 32 ARINC words into the Transmit FIFO, starting at the next available FIFO location. If Status Register bit SR24 equals “1” (Tx FIFO empty), then up to 32 words (32 bits each) may be loaded. If Status Register bit SR24 equals “0” then only the available positions may be loaded. The Tx FIFO count may be read prior to writing the FIFO using SPI op code 0x90 to determine exactly how many messages may be loaded. If all 32 positions are full, Status Register bit SR26 is asserted. Further attempts to load the Transmit FIFO are ignored until at least one ARINC word is transmitted.

The Tx FIFO half-full flag (Status Register bit SR25) equals “0” when the Tx FIFO contains less than 16 words. When SR25 equals “0”, the system microprocessor can safely initiate a 16-word ARINC block-write sequence.

In normal operation (Control Register bit CR3 = “0” and CR10 = “1”), the 32nd bit transmitted is a word parity bit. Odd or even parity is selected by programming Control Register bit CR11 to a “0” or “1” respectively. If Control Register bit CR10 equals “0”, all 32 bits loaded into the Transmit FIFO are treated as data and are transmitted.

SPI op code 0xA asynchronously clears all data in the Tx FIFO. The Tx FIFO should be cleared after a self-test before starting normal operation to avoid inadvertent transmission of test data.

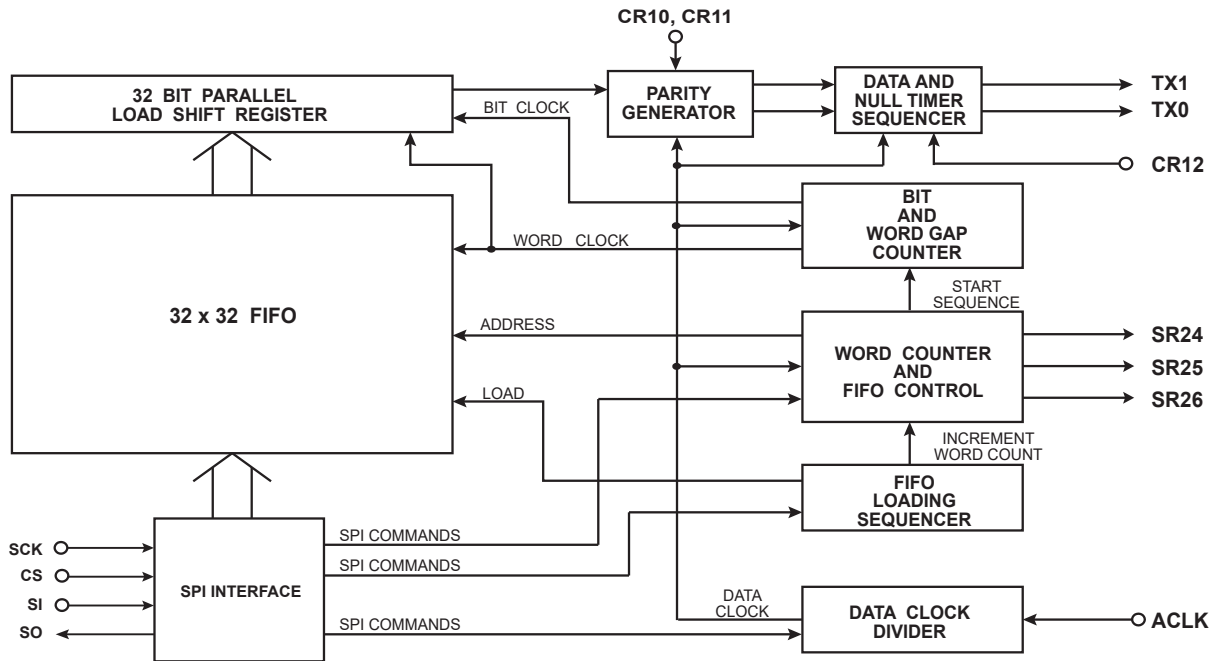


Figure 5. Transmitter Block Diagram

Data Transmission

If Control Register bit CR14 equals “1”, ARINC 429 data is transmitted immediately following the CS rising edge of the SPI instruction that loaded data into the Transmit FIFO. Loading Control Register bit CR14 to “0” allows the software to control transmission timing; each time an SPI op code 0x0B is executed, all loaded Transmit FIFO words are transmitted. If new words are loaded into the Transmit FIFO before transmission stops, the new words will also be output. Once the Transmit FIFO is empty and transmission of the last word is complete, the FIFO can be loaded with new data which is held until the next SPI 0x0B instruction is executed. Once transmission is enabled, the FIFO positions are incremented with the top register loading into the data transmission shift register. The 31 or 32 bits in the data transmission shift register are presented sequentially to the outputs in the ARINC 429 format with the following timing:

	High Speed	Low Speed
ARINC Data Bit Time	10 clocks	80 clocks
Data Bit Time	5 clocks	40 clocks
Null Bit Time	5 clocks	40 clocks
Word Gap Bit Time	40 clocks	320 clocks

The word counter detects when all loaded positions have been transmitted and sets the transmitter ready flag, SR24, high.

Transmitter parity

The parity generator counts the Ones in the 31-bit word. If control register bit CR11 is set to a “0”, the 32nd bit transmitted will make parity odd. If the control bit CR11 is a “1”, the parity is even. Setting CR10 to “0” bypasses the parity generator, and allows 32 bits of data to be transmitted.

Loopback Self-Test

The HI-35981 may use the Transmit FIFO to execute user-defined self-test sequences (loopback test) for each receiver. This feature may be individually enabled for each receiver by resetting Control Register CR5 bit to “0”. 32-bit test words are loaded to the Transmit FIFO using SPI instructions 0x08 (for ARINC 429 high-speed data rate) or 0x09 (for ARINC 429 low speed). Upon completion of the instruction, the words are shifted out of the FIFO and routed to all receivers. If self-test mode is enabled and the receive channel is set to the correct speed, each channel will receive the test words as if they came from an external ARINC 429 bus. If loopback is not enabled, the channel ignores the self-test words and continues to respond to the external ARINC 429 bus. In all cases, the serial test words may be observed at the TX1 and TX0 pins, as shown in Table 11.

NOTE: The first bit shifted into the FIFO will be the first bit sent to the receivers and the TX1 and TX0 pins. In ARINC 429 protocol, this bit is the LSB.

Table 11. Test Outputs

TX1	TX0	ARINC 429 State
0	0	NULL
1	0	ONE
0	1	ZERO

Line Receiver Input Pins

Each channel has two sets of Line Receiver input pins, RINA/B and RINA/B-40. Only one pair may be used to connect to the ARINC 429 bus. THE RINA/B pins may be connected directly to the ARINC 429 bus. The RINA/B-40 pins require an external 40K Ω resistor to be added in series with each ARINC input without affecting the ARINC input thresholds. This option is especially useful in applications where lightning protection circuitry is also required.

When using the RINA/B-40 pins, each side of the ARINC bus must be connected through a 40K Ω series resistor in order for the chip to detect the correct ARINC levels. The typical 10V differential signal is translated and input to a window comparator and latch. The comparator levels are set so that with the external 40K Ω resistors, they are just below the standard 6.5V minimum ARINC data threshold and just above the standard 2.5V maximum ARINC null threshold.

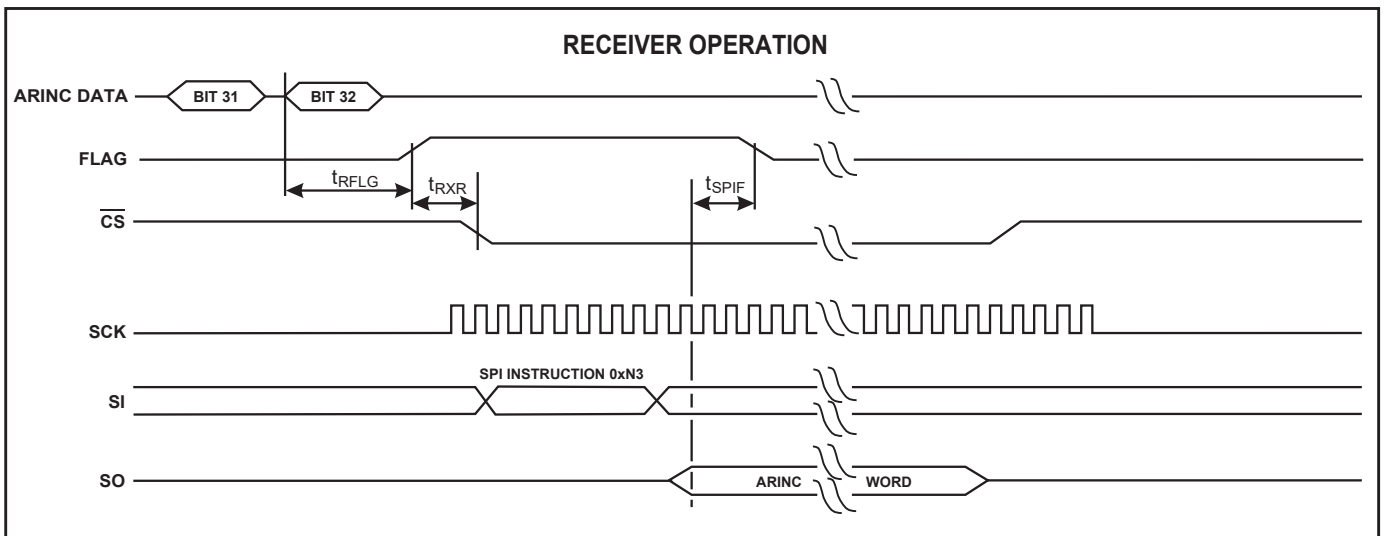
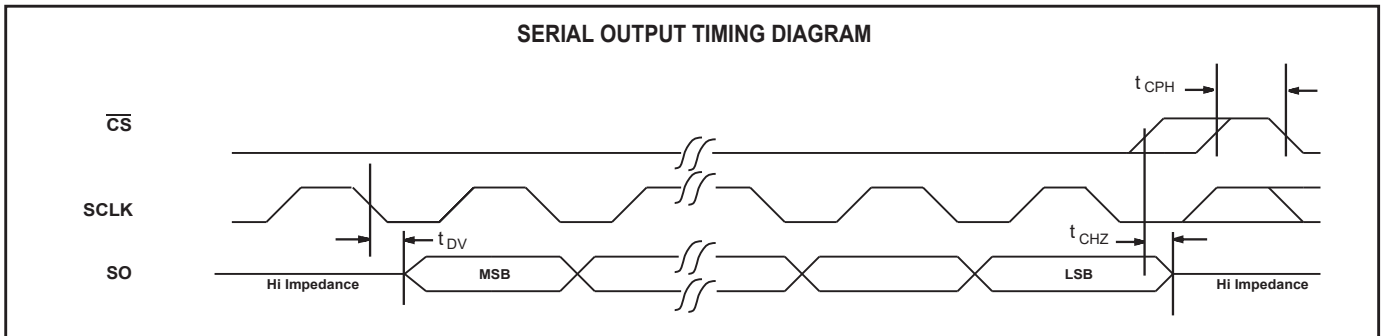
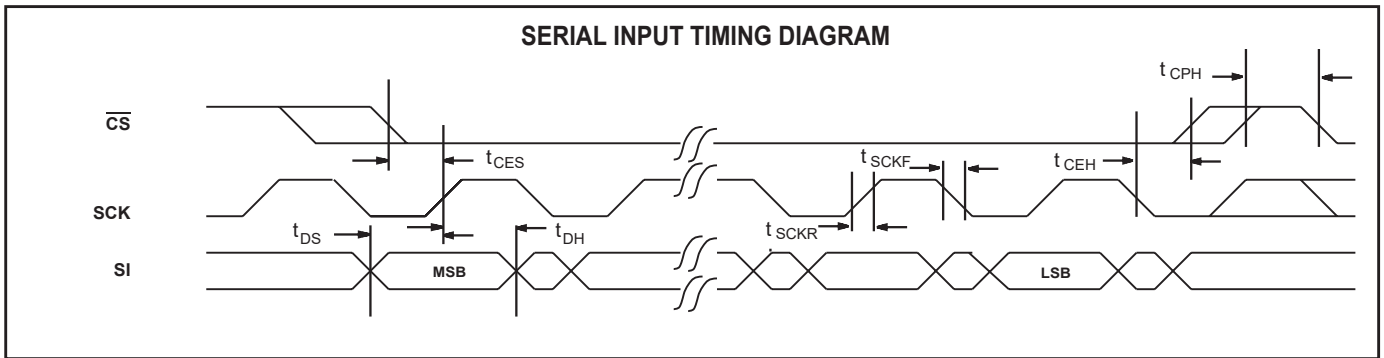
Please refer to the Holt AN-300 Application Note for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

Master Reset (MR)

Assertion of Master Reset (MR) causes immediate termination of data reception. The eight Receive FIFOs are cleared. Status Register FIFO flags and FIFO status output signals are also cleared. Attempting to read FIFO data when FIFOs are empty will result in indeterminate data. Writing the Control Register clears the label memory. **Note that Master Reset does not affect the eight channel Control Registers, does not clear the label memory and Control Registers do not initialize or power up with a default setting.** Master Reset may be asserted using the MR input pin or by executing SPI instruction 0x07.

An individual receive channel can be reset by setting its corresponding Control Register CR3 bit to "1". This clears the channel's receiver logic and Receive FIFO and disables the receiver until CR3 is reset to "0". For applications requiring less than eight channels, unused receivers should be held in reset by setting the corresponding Control Register CR3 bits.

TIMING DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Supply Voltages V_{DD}	-0.3 to +7.0V	Power dissipation at 25°C Plastic Quad Flat Pack	1.5 W, derate 10mW/°C
ARINC Input Voltage (Pins RIN1A, RIN1B, RIN2A, RIN2B)	DC -120V to +120V	DC Current Drain per pin	±10mA
	AC 120Vrms@ 400Hz		
Voltage at any other pin	-0.3V to $V_{DD}+0.3V$	Storage Temperature Range	-65°C to +150°C
Solder temperature (Reflow)	260°C	Operating Temperature Range (Industrial)	-40°C to +85°C
		(Extended Temp)	-55°C to +125°C

NOTE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Table 12. DC Electrical Characteristics

V_{DD} = 3.3V or 5.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Test Conditions	Limits			Unit	
			Min	Typ	Max		
ARINC INPUTS - Pins RINA, RINB, RINA-40 (with external 40KΩ), RINB-40 (with external 40KΩ)							
Differential Input Voltage (RIN1A to RIN1B, RIN2A to RIN2B, etc.)	ONE	V_{IH}	Common mode voltages less than ±30V with respect to GND	6.5	10.0	13.0	V
	ZERO	V_{IL}		-13.0	-10.0	-6.5	V
	NULL	V_{NUL}		-2.5	0	2.5	V
Input Resistance	Differential	R_I		-	160	-	kΩ
	To GND	R_G		-	80	-	kΩ
	To V_{DD}	R_H		-	80	-	kΩ
Input Current	Input Sink	I_{IH}		-	-	200	μA
	Input Source	I_{IL}		-450	-	-	μA
Input Capacitance (Guaranteed but not tested)	Differential	C_I	(RINA to RINB)	-	-	20	pF
	To GND	C_G		-	-	20	pF
	To V_{DD}	C_H		-	-	20	pF
LOGIC INPUTS							
Input Voltage	Input Voltage HI	V_{IH}		70% V_{DD}	-	-	V
	Input Voltage LO	V_{IL}		-	-	30% V_{DD}	V
Input Current	Input Sink	I_{IH}		-	-	1.5	μA
	Input Source	I_{IL}		-1.5	-	-	μA
	Pull-down Current (MR, SI, SCK, ACLK pins)	I_{PD}		-	-	100	μA
	Pull-up Current (CS)	I_{PU}		-100	-	-	μA
LOGIC OUTPUTS							
Output Voltage	Logic “1” Output Voltage	V_{OH}	$I_{OH} = -100\mu A$	90% V_{DD}	-	-	V
	Logic “0” Output Voltage	V_{OL}	$I_{OL} = 1.0mA$	-	-	10% V_{DD}	V

HI-35981

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Output Current (All outputs and Bi-directional pins)	Output Sink I_{OH}	$V_{OUT} = 0.4V$ $V_{OUT} = V_{DD} - 0.4V$	1.6	-	-	mA
	Output Source I_{OL}		-	-	-1.0	mA
Output Capacitance	C_O		-	15	-	pF
OPERATING VOLTAGE RANGE						
	V_{DD}		3.15	-	5.25	V
OPERATING SUPPLY CURRENT						
	I_{DD}		-	10	15	mA

Table 13. AC Electrical Characteristics

$V_{DD} = 3.3V$ or $5.0V$, $GND = 0V$, T_A = Operating Temperature Range and $f_{clk} = 1MHz \pm 0.1\%$ with 60/40 duty cycle

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
SPI INTERFACE TIMING					
SCK clock Period	t_{CYC}	80	-	-	ns
\overline{CS} setup time to first SCK rising edge	t_{CES}	10	-	-	ns
\overline{CS} hold time after last SCK falling edge	t_{CEH}	20	-	-	ns
\overline{CS} inactive between SPI instructions	t_{CPH}	20	-	-	ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	10	-	-	ns
SPI SI Data hold time after SCK rising edge	t_{DH}	10	-	-	ns
SCK rise time	t_{SCKR}	-	-	5	ns
SCK fall time	t_{SCKF}	-	-	5	ns
SO valid after SCK falling edge	t_{DV}	-	-	40	ns
SO high-impedance after \overline{CS} inactive	t_{CHZ}	-	-	50	ns
Master Reset pulse width	t_{MR}	100	-	-	ns
RECEIVER TIMING					
Delay - Last bit of received ARINC word to RFLAG (Full or Empty) – Hi Speed	t_{RFLG}	-	-	16	μs
Delay - Last bit of received ARINC word to RFLAG (Full or Empty) – Lo Speed	t_{RFLG}	-	-	126	μs
Received data available to SPI interface. RFLAG to \overline{CS} active	t_{RXR}	0	-	-	ns
SPI receiver read	t_{SPIF}	-	-	155	ns
TRANSMITTER TIMING					
SPI transmit data write or FIFO clear instruction to TFLAG (Empty or Full)	t_{TFLG}			120	ns
SPI instruction to ARINC 429 data output – Hi Speed	t_{SDAT}	-	-	17	μs
SPI instruction to ARINC 429 data output – Lo Speed	t_{SDAT}	-	-	118	μs

HI-35981

Parameters	Symbol	Limits			Units	
		Min	Typ	Max		
Delay TFLAG high after enable transmit - Hi Speed	t_{DATT}	-	-	14	μs	
Delay TFLAG high after enable transmit - Lo Speed	t_{DATT}	-	-	114	μs	
Line driver transition differential times:						
(High Speed, control register CR10 = Logic 0)	high to low	t_{rx}	1.0	1.5	2.0	μs
	low to high	t_{rx}	1.0	1.5	2.0	μs
(Low Speed, control register CR10 = Logic 1)	high to low	t_{rx}	5.0	10	15	μs
	low to high	t_{rx}	5.0	10	15	μs

ORDERING INFORMATION

HI - 35981 PQ x x

PART NUMBER	LEAD FINISH
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PQ	64 PIN PLASTIC QUAD FLAT PACK, PQFP (64PQTS)

REVISION HISTORY

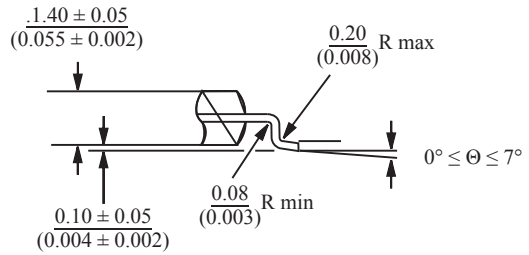
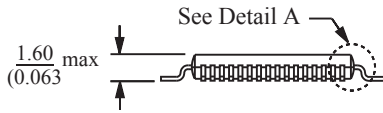
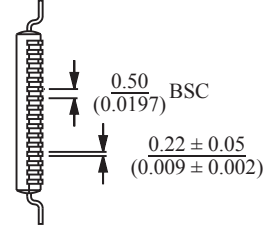
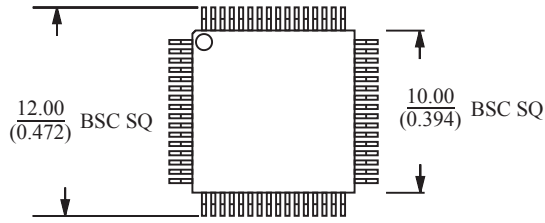
Revision	Date	Description of Change
DS35981, Rev. New	08/25/2022	Initial Release.

PACKAGE DIMENSIONS

64-PIN PLASTIC QUAD FLAT PACK (PQFP)

millimeters (inches)

Package Type: 64PQTS



Detail A

BSC = "Basic Spacing between Centers"
is theoretical true position dimension and
has no tolerance. (JEDEC Standard 95)