HT32F67233
Datasheet

32-Bit Arm® Cortex®-M0+ Microcontroller,
up to 32 KB Flash and 4 KB SRAM with 1 Msps ADC,
USART, UART, SPI, I²C, GPTM, SCTM, BFTM, WDT and
Sub-1GHz GFSK RF Transceiver

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1 General Description

The Holtek HT32F67233 is high performance, low power consumption 32-bit microcontrollers based around an Arm® Cortex®-M0+ processor core. The Cortex®-M0+ is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The device operates at a frequency of up to 40 MHz for HT32F67233 with a Flash accelerator to obtain maximum efficiency. It provides up to 32 KB of embedded Flash memory for code/data storage and 4 KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I²C, USART, UART, SPI, GPTM, SCTM, BFTM, WDT, SW-DP (Serial Wire Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The RF module is a high performance and low cost OOK/GFSK transceiver for wireless applications in the 315 MHz, 433 MHz, 470 MHz, 868 MHz and 915 MHz frequency bands. It incorporates a highly integrated sub-1GHz transceiver and a baseband modem with programmable GFSK data rates from 2 Kbps to 250 Kbps and OOK data rates from 0.5 Kbps to 20 Kbps. Data handling features include 64-byte TX/RX FIFO and packet handling such as CRC generation, Forward Error Correction and data whitening, Manchester encoding.

The RF module is optimized for the very low power consumption applications. At 433 MHz band, its RX mode is operated at 5.8 mA and it delivers +19 dBm TX output power at 71 mA current consumption. A low-noise low-IF receiver can achieve -117 dBm sensitivity of 2 Kbps data rate at 433 MHz bands. A Class-E Power Amplifier can deliver up to +20 dBm output power at 433/868 MHz bands. A fully integrated Fractional-N synthesizer can support a wide frequency range with a fine resolution. Both loop filter and XO load capacitors are integrated to on-chip to minimize the requirement for external components.

External MCU can access the RF module through a 3-wire or 4-wire SPI interface. The device supports short strobe commands to reduce the loading of the MCU while maintaining wireless communication link.

Additional link layer features like RSSI for channel assessment, auto-acknowledgement and auto-resend, WOT and WOR, etc., facilitate microcontroller based ISM bands wireless link applications.

The above features ensure that the device is suitable for use in a wide range of applications, especially in areas such as industrial control (meter and data logging), smart home appliances (security products, sensor and alarm system), remote control (keyless entry), industrial/agricultural automation, data acquisition and recording and so on.

2 Features

Core

- 32-bit Arm® Cortex®-M0+ processor core
- Up to 40 MHz operating frequency
- Single-cycle multiplication
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex®-M0+ processor is a very low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications that require an area optimized, low-power processor. The processor is based on the ARMv6-M architecture and supports Thumb® instruction sets; single-cycle I/O port; hardware multiplier and low latency interrupt respond time.

On-chip Memory

- Up to 32 KB on-chip Flash memory for instruction/data and options storage
- 4 KB on-chip SRAM
- Supports multiple boot modes

The Arm® Cortex®-M0+ processor accesses and debug accesses share the single external interface to external AHB peripherals. The processor accesses take priority over debug accesses. The maximum address range of the Cortex®-M0+ is 4 GB since it has a 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex®-M0+ processor to reduce the software complexity of repeated implementation by different device vendors. However, some regions are used by the Arm® Cortex®-M0+ system peripherals. Refer to the Arm® Cortex®-M0+ Technical Reference Manual for more information. Figure 2 shows the memory map of the device, including code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller – FMC

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer and cache are provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit – RSTCU

- Supply supervisor:
  - Power On Reset / Power Down Reset – POR/PDR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit, RSTCU, has three kinds of reset, a power on reset, a system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SW-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit – CKCU

- External 4 to 16 MHz crystal oscillator
- Internal 8 MHz RC oscillator trimmed to ±2 % accuracy at 3.3 V operating voltage and 25 °C operating temperature
- Internal 32 kHz RC oscillator
- Integrated system clock PLL
- Independent clock divider and gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers, APB clock divider and gating circuitry. The AHB, APB and Cortex®-M0+ clocks are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer uses the LSI as its clock source.

Power Management – PWRCU

- Single V_{DD} power supply: 2.0 V to 3.6 V
- Integrated 1.5 V LDO regulator for MCU core, peripherals and memories power supply
- Two power domains: V_{DD}, V_{CORE}
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in the device provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

External Interrupt/Event Controller – EXTI

- Up to 16 EXTI lines with configurable trigger source and type
- All GPIO pins can be selected as EXTI trigger source
- Source trigger type includes high level, low level, negative edge, positive edge, or both edge
- Individual interrupt enable, wakeup enable and status bits for each EXTI line
- Software interrupt trigger mode for each EXTI line
- Integrated deglitch filter for short pulse blocking

The External Interrupt/Event Controller, EXTI, comprises 16 edge detectors which can generate a wake-up event or interrupt requests independently. Each EXTI line can also be masked independently.

Analog to Digital Converter – ADC

- 12-bit SAR ADC engine
- Up to 1 Msps conversion rate
- Up to 8 external analog input channels

A 12-bit multi-channel ADC is integrated in the device. There are multiplexed channels, which include 8 external analog signal channels and 2 internal channels which can be measured. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

I/O Ports – GPIO

- Up to 21 GPIOs
- Port A, B are mapped as 16 external interrupts – EXTI
- Almost all I/O pins have a configurable output driving current

There are up to 21 General Purpose I/O pins, GPIO, named Port A and Port B for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximize flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins. The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

General-Purpose Timer – GPTM

- 16-bit up, down, up/down auto-reload counter
- Up to 4 independent channels
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned and Center-aligned Counting Modes
- Single Pulse Mode Output
- Encoder interface controller with two inputs using quadrature decoder

The General-Purpose Timer Module consists of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Single Channel Timer – SCTM

- 16-bit up and auto-reload counter
- One channel for each timer
- 16-bit programmable prescaler that allows division of the prescaler clock source by any factor between 1 and 65536 to generate the counter clock frequency
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge-aligned

The Single-Channel Timer consists of one 16-bit up-counter, one 16-bit Capture/Compare Register (CCR), one 16-bit Counter-Reload Register (CRR) and several control/status registers. It can be used for a variety of purposes including general timer, input signal pulse width measurement or output waveform generation such as single pulse generation or PWM output.

Basic Function Timer – BFTM

- 32-bit compare/match count-up counter – no I/O control
- One shot mode – counter stops counting when compare match occurs
- Repetitive mode – counter restarts when compare match occurs

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer – WDT

- 12-bit down counter with 3-bit prescaler
- Provide reset to the system
- Programmable watchdog timer window function
- Register write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT delta value register, WDT operation control circuitry and a WDT protection mechanism. If the software does not reload the counter value before a Watchdog Timer underflow occurs, a reset will be generated when the counter underflows. In addition, a reset is also generated if the software reloads the counter when the counter value is greater than the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Inter-integrated Circuit – I²C

- Supports both master and slave modes with a frequency of up to 1 MHz
- Provides an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing modes and general call addressing
- Supports slave multi-addressing mode with maskable address

The I^2C is an internal circuit allowing communication with an external I^2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I^2C module provides three data transfer rates: 100 kHz in the Standard mode, 400 kHz in the Fast mode and 1 MHz in the Fast plus mode. The SCL period generation register is used to setup different kinds of duty cycle implementations for the SCL pulse.

The SDA line which is connected directly to the I^2C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I^2C also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I^2C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave modes
- Frequency of up to (f_{PCLK}/2) MHz for the master mode and (f_{PCLK}/3) MHz for the slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried out in a similar way but in a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Supports both asynchronous and clocked synchronous serial communication modes
- Programmable baud rate clock frequency up to (f_{PCLK}/16) MHz for Asynchronous mode and (f_{PCLK}/8) MHz for synchronous mode
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error
- Auto hardware flow control mode – RTS, CTS
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- FIFO Depth: 8-level for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous data transfer. The USART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The USART peripheral function supports four types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt and Time Out Interrupt. The USART module includes a transmitter FIFO, (TX_FIFO) and receiver

FIFO (RX_FIFO). The software can detect a USART error status by reading the USART Status & Interrupt Flag Register, USRSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

Universal Asynchronous Receiver Transmitter – UART

- Asynchronous serial communication operating baud-rate clock frequency up to (f_{PCLK}/16) MHz
- Full duplex communication
- Fully programmable serial communication characteristics including:
  - Word length: 7, 8, or 9-bit character
  - Parity: Even, odd, or no-parity bit generation and detection
  - Stop bit: 1 or 2 stop bit generation
  - Bit order: LSB-first or MSB-first transfer
- Error detection: Parity, overrun and frame error

The Universal Asynchronous Receiver Transceiver, UART, provides a flexible full duplex data exchange using asynchronous transfer. The UART is used to translate data between parallel and serial interfaces, and is commonly used for RS232 standard communication. The UART peripheral function supports Line Status Interrupt. The software can detect a UART error status by reading the UART Status & Interrupt Flag Register, URSIFR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

RF Module

- Frequency band: 315/433/470/868/915 MHz
- OOK/FSK/GFSK modulation
- Supports 3-wire or 4-wire SPI interface
- Programmable data rate:
  - OOK: 0.5 Kbps ~ 20 Kbps
  - GFSK: 2 Kbps ~ 250 Kbps
- Programmable TX output power: up to 20 dBm
- Low current consumption
  - 0.4μA deep sleep mode current with data retention
  - RX current consumption (AGC on & low data rate) @ 433.92 MHz: 5.4 mA
  - RX current consumption (AGC on & low data rate) @ 868.3 MHz: 6.8 mA
  - TX current consumption @ 433.92 MHz: 33 mA @ 10 dBm P_{OUT}
  - TX current consumption @ 868.3 MHz: 35 mA @ 10 dBm P_{OUT}
- High RX sensitivity (433.92 MHz)
  - -120 dBm at 2 Kbps on-air data rate
  - -103 dBm at 250 Kbps on-air data rate
- High RX sensitivity (868.3 MHz)
  - -119 dBm at 2 Kbps on-air data rate
  - -102 dBm at 250 Kbps on-air data rate
- On-chip VCO and Fractional-N synthesizer with integrated loop filter
- Supports low cost 16 MHz crystal with integrated load capacitor
- AGC (Auto Gain Control) to achieve wide input range, up to +10 dBm
- AFC (Auto Frequency Compensation) for frequency drift due to X'tal aging

- On-chip low power RC oscillator for WOR (Wake-on-RX) and WOT (Wake-on-TX) functions
- Physical TX/RX FIFO buffers: TX 64 bytes, RX 64 bytes
- Simple FIFO/Block FIFO/Extend FIFO (up to 255 bytes)/Infinite FIFO modes
- Programmable threshold for carrier detection
- Frame synchronization recognition for both FIFO mode and Direct mode
- Packet handling
  - FEC (Forward Error Correction)
  - Data whitening
  - Manchester encoding
  - CRC-16 checking
- ATR (Auto-Transmit-Receive)
  - Auto-resend
  - Auto-acknowledgment
  - WOT + Auto-resend
  - WOR + Auto-acknowledgment
- Packet filtering
  - CRC filtering
  - Address filtering

Debug Support

- Serial Wire Debug Port – SW-DP
- 4 comparators for hardware breakpoint or code / literal patch
- 2 comparators for hardware watchpoints

Package and Operation Temperature

- 46-pin QFN package
- Operation temperature range: -40 °C to 85 °C

3 Overview

Device Information

Table 1. Features and Peripheral List

Peripherals		HT32F67233
Main Flash (KB)		31
Option Bytes Flash (KB)		1
SRAM (KB)		4
Timers	GPTM	1
	SCTM	2
	BFTM	1
	WDT	1
Communication	SPI	1
	USART	1
	UART	1
	I^2C	1
EXTI		16
12-bit ADC		1
Number of channels		8 Channels
GPIO		Up to 21
RF frequency bands		315/433/470/868/915 MHz
Modulation type		OOK/GFSK
Programmable data rate		0.5 ~ 50 Kbps (OOK mode)
		2 ~ 250 Kbps (GFSK mode)
Max. output power		20 dBm
RF RX current consumption		5.8 mA @ 433 MHz
		6.8 mA @ 868 MHz
RX sensitivity		-117 dBm @ 433 MHz
		-116 dBm @ 868 MHz
CPU frequency		Up to 40 MHz
Operating voltage		2.0 V ~ 3.6 V
Operating temperature		-40 °C ~ 85 °C
Package		46-pin QFN

Note: The functions listed here, except the Sub-1 GHz GFSK RF transceiver, are compatible with the HT32F52230 device. Refer to the HT32F52230 user manual for detailed function description.

Block Diagram

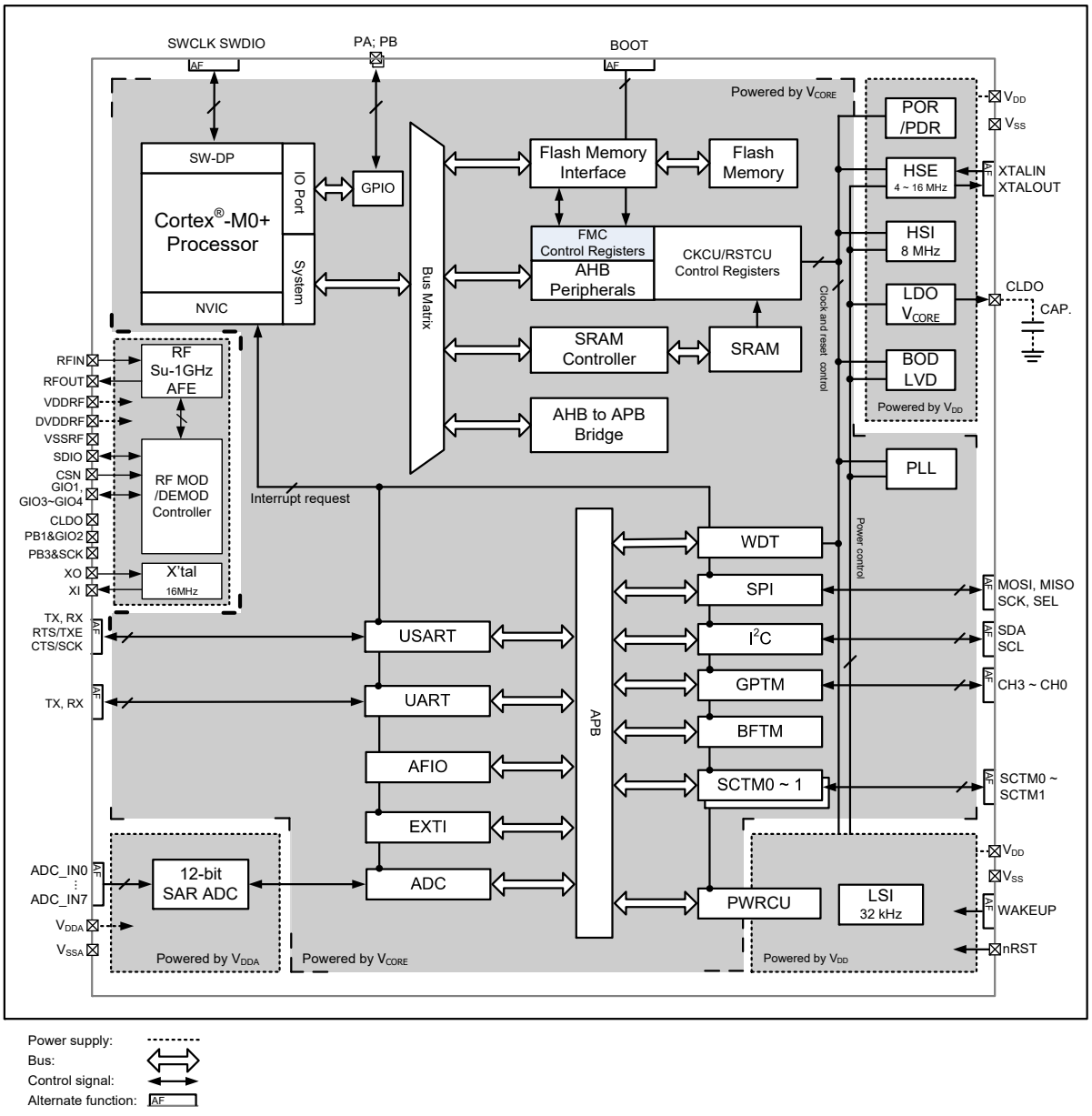


Figure 1. Block Diagram

Memory Map

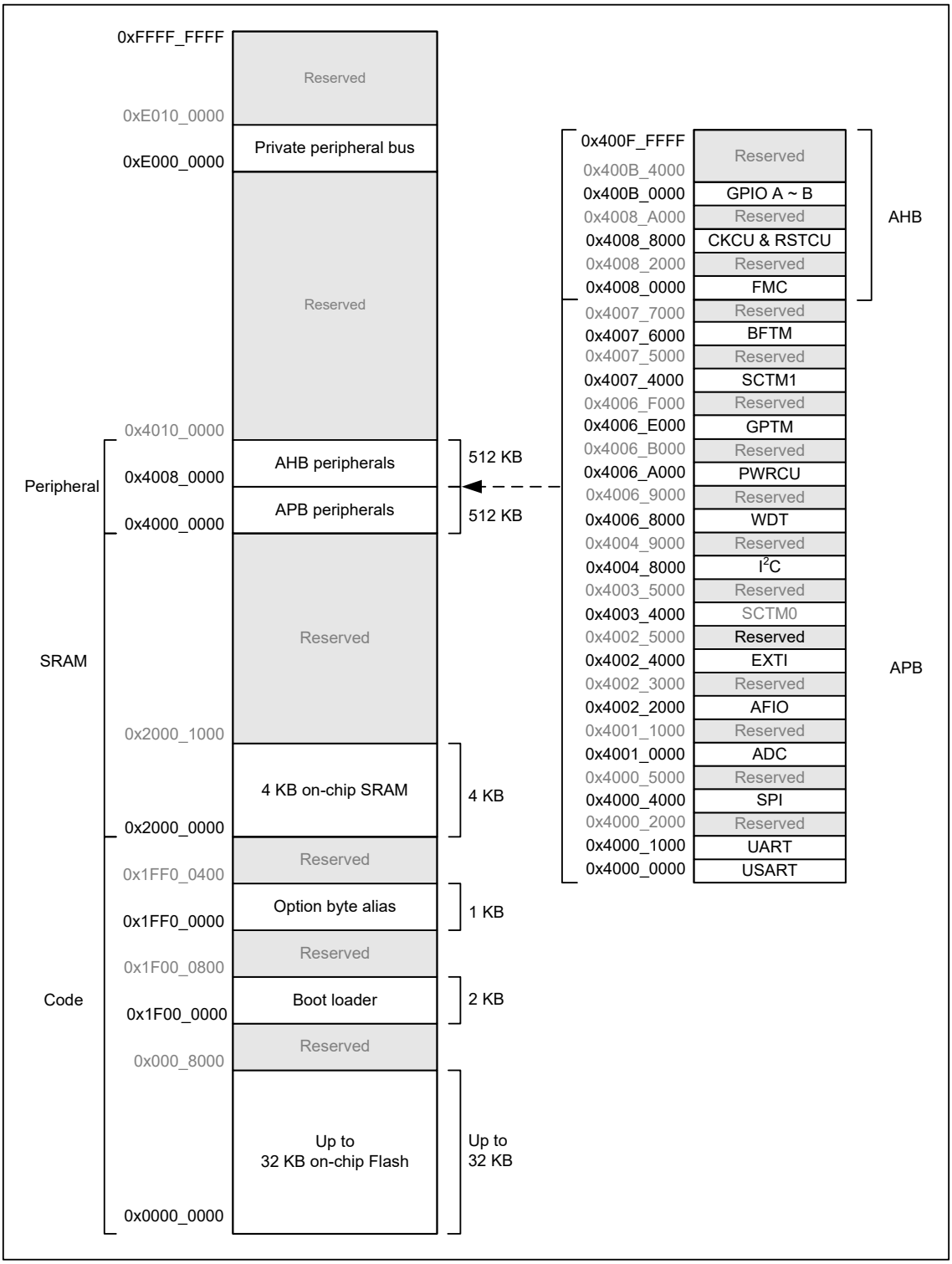


Figure 2. Memory Map

Table 2. Register Map

Start Address	End Address	Peripheral	Bus
0x4000_0000	0x4000_0FFF	USART	APB
0x4000_1000	0x4000_1FFF	UART	
0x4000_2000	0x4000_3FFF	Reserved	
0x4000_4000	0x4000_4FFF	SPI	
0x4000_5000	0x4000_FFFF	Reserved	
0x4001_0000	0x4001_0FFF	ADC	
0x4001_1000	0x4002_1FFF	Reserved	
0x4002_2000	0x4002_2FFF	AFIO	
0x4002_3000	0x4002_3FFF	Reserved	
0x4002_4000	0x4002_4FFF	EXTI	
0x4002_5000	0x4003_3FFF	Reserved	
0x4003_4000	0x4003_4FFF	SCTM0	
0x4003_5000	0x4004_7FFF	Reserved	
0x4004_8000	0x4004_8FFF	I^2C	
0x4004_9000	0x4006_7FFF	Reserved	
0x4006_8000	0x4006_8FFF	WDT	
0x4006_9000	0x4006_9FFF	Reserved	
0x4006_A000	0x4006_AFFF	PWRCU	
0x4006_B000	0x4006_DFFF	Reserved	
0x4006_E000	0x4006_EFFF	GPTM	
0x4006_F000	0x4007_3FFF	Reserved	
0x4007_4000	0x4007_4FFF	SCTM1	
0x4007_5000	0x4007_5FFF	Reserved	
0x4007_6000	0x4007_6FFF	BFTM	
0x4007_7000	0x4007_FFFF	Reserved	
0x4008_0000	0x4008_1FFF	FMC	AHB
0x4008_2000	0x4008_7FFF	Reserved	
0x4008_8000	0x4008_9FFF	CKCU & RSTCU	
0x4008_A000	0x400A_FFFF	Reserved	
0x400B_0000	0x400B_1FFF	GPIOA	
0x400B_2000	0x400B_3FFF	GPIOB	
0x400B_4000	0x400F_FFFF	Reserved	

Clock Structure

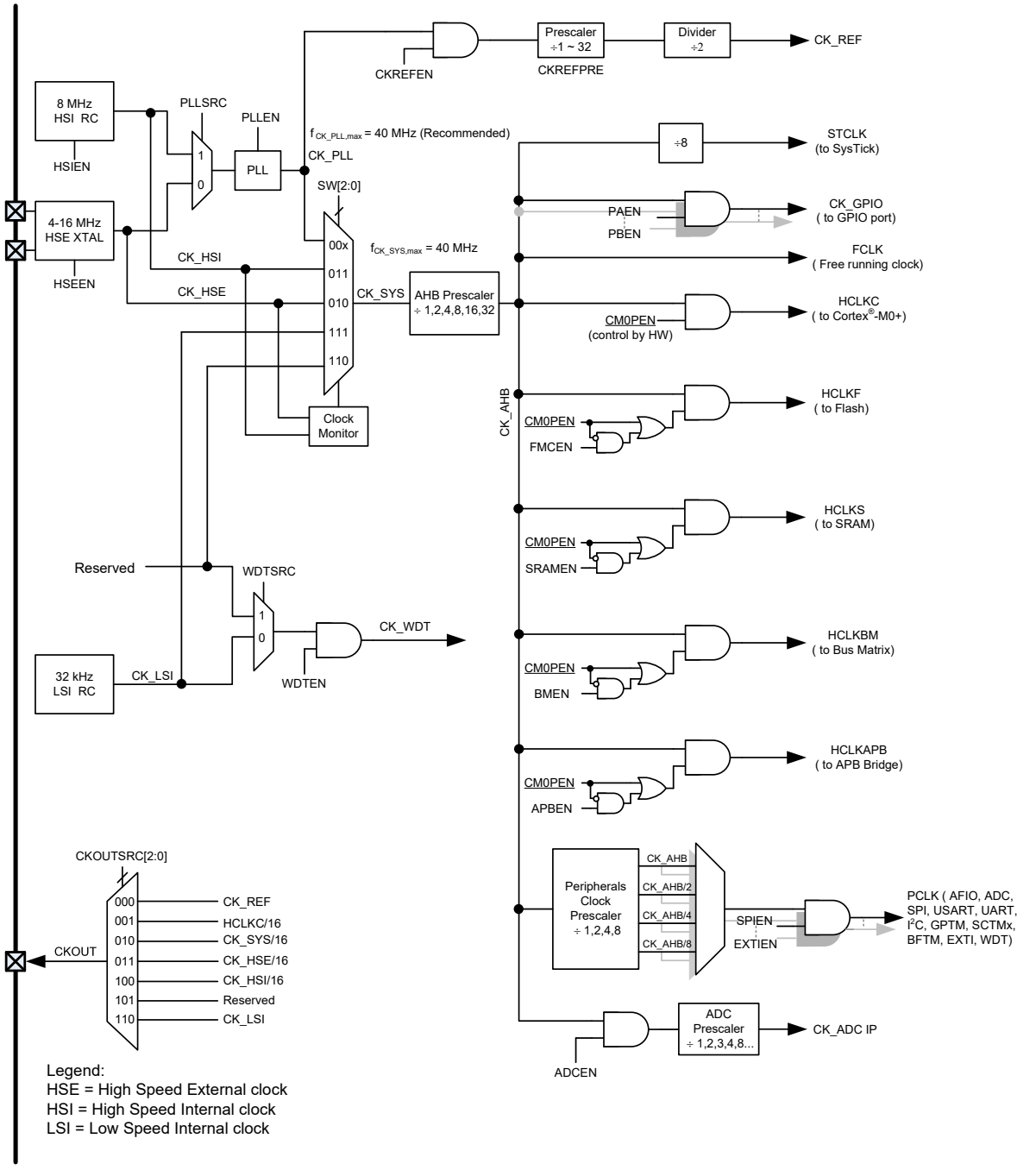
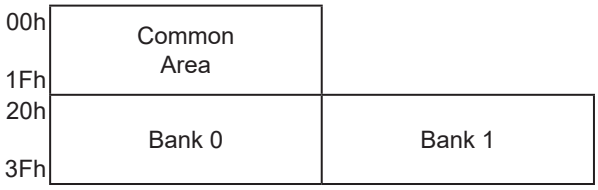


Figure 3. Clock Structure

4 RF Module

Memory Mapping



Common Area: It contains 32 bytes space. Accessing addresses 00h ~ 1Fh always means to access the Common Area regardless of Bank Pointer configuration.

Bank 0 ~ 1: Each bank contains 32 bytes space. They are selected by the Bank Pointer.

The Bank Pointer, BANK[1:0], which is defined in the Common Area, can be set directly by the Set Register Bank command and read/written by the Control Register command.

Control Register Access

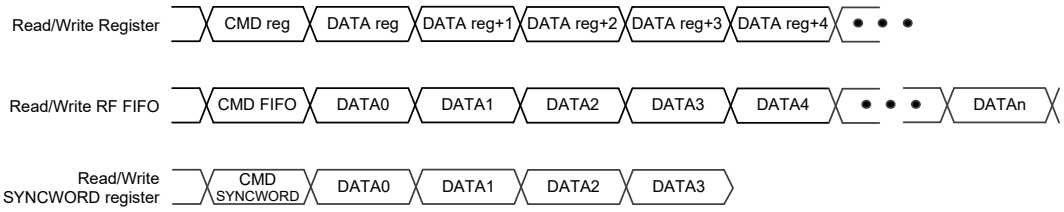


Figure 4. Strobe Command Followed by n-byte Data (CmdD)

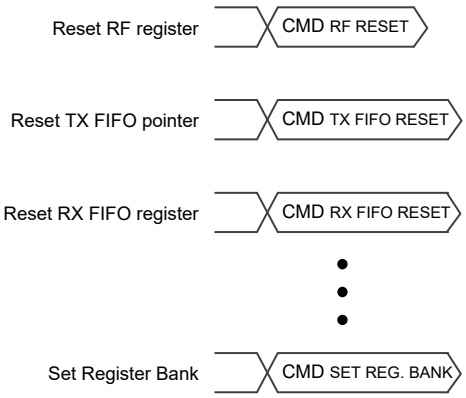


Figure 5. Strobe Command Only (CmdO)

SFR Mapping and Bit Definition

Common Area Control Register

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value except the FSYCK_EN, FSYCK_DIV[1:0], PWRON, GIO1S[2:0], GIO2S[2:0], PADDS[1:0], GIO3S[3:0], GIOPU[3:1], SPIPU, SDO_TEN bits in the RC1, IO1, IO2 and IO3 registers. These bits keep unchanged after software reset.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
00h	CFG1	OOK_EN	AGC_EN	RXCON_EN	DIR_EN	—	—	BANK[1:0]	
01h	RC1	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RST_LL
02h	IRQ1	RXTO	RXFFOW	—	RXCRCF	RXDETS[1:0]		IRQCPOR	IRQPOR
03h	IRQ2	ARKTFIE	ATRCTIE	FIFOLTIE	RXERRIE	RXDETIE	CALCMPIE	RXCMPIE	TXCMPIE
04h	IRQ3	ARKTFIF	ATRCTIF	FIFOLTIF	RXERRIF	RXDETIF	CALCMPIF	RXCMPIF	TXCMPIF
06h	IO1	PADDS[1:0]		GIO2S[2:0]			GIO1S[2:0]		
07h	IO2	—				GIO3S[3:0]			
08h	IO3	SDO_TEN	SPIPU	—	—	GIOPU[3:1]			—
09h	FIFO1	—	—	TXFFSA[5:0]					
0Ah	FIFO2	—	—	—	RXPL2F_EN	FFINF_EN	FFMG_EN	FFMG[1:0]	
0Bh	PKT1	TXPMLEN[7:0]							
0Ch	PKT2	PID[1:0]		TRAILER_EN	WHTFMT[0]	SYNCLEN[1:0]		—	
0Dh	PKT3	MCH_EN	FEC_EN	CRC_EN	CRCFMT	PLLEN_EN	PLHAC_EN	PLHLEN	PLH_EN
0Eh	PKT4	WHT_EN	WHTSD[6:0]						
0Fh	PKT5	TXDLEN[7:0]							
10h	PKT6	RXDLEN[7:0]							
11h	PKT7	RXPID[1:0]		DLY_RXS[2:0]			DLY_TXS[2:0]		
12h	PKT8	—		PLHA[5:0]					
13h	PKT9	PLHEA[7:0]							
14h	MOD1	DTR[7:0]							
15h	MOD2	RXFDOS[11:8]				DITHER[1:0]		—	DTR[8]
16h	MOD3	RXFDOS[7:0]							
17h	DM1	—	—	MDIV[5:0]					
18h	DM2	—	—	SDR[5:0]					
19h	DM3	CSF_SW_EN	FD_MOD[6:0]						
1Ah	DM4	—				CFO_DSEL	—	PH_DIFF_MOD	—
1Bh	DM5	FD_HOLD[7:0]							
1Eh	DM8	M_RATIO[7:0]							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The reset value shown in the following register description tables means the software reset results of strobe command.

- **CFG1: Configuration Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	OOK_EN	AGC_EN	RXCON_EN	DIR_EN	—	—	BANK[1:0]	
R/W	R/W	R/W	R/W	R/W	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

Bit 7 **OOK_EN**: OOK mode enable
0: GFSK mode
1: OOK mode, support Direct mode (DIR_EN = 1) only

Bit 6 **AGC_EN**: AGC enable
0: Disable
1: Enable

Bit 5 **RXCON_EN**: RX continue mode enable
0: Disable
1: Enable
Note that this bit only affects normal RX mode and ATR RX mode without ARK function.

Bit 4 **DIR_EN**: Direct mode enable
0: TX/RX data from packet handling hardware
1: TX/RX data from/to external MCU directly

Bit 3~2 Reserved, must be "00"

Bit 1~0 **BANK[1:0]**: Control register bank selection
00: Bank 0
01: Bank 1
10: Bank 2
11: Reserved
This selection can be set by both the Set Register Bank command and Control Register command.

- **RC1: Reset/Clock Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PWRON	FSYCK_RDY	XCLK_RDY	XCLK_EN	FSYCK_DIV[1:0]		FSYCK_EN	RST_LL
R/W	R/W	R	R	R/W	R/W		R/W	R/W
POR	1	—	—	—	0	0	0	—
Reset	—	0	0	1	—	—	—	0

Bit 7 **PWRON**: 3.3 V power on flag
This bit is only set to 1 by power on reset and not affected by software reset of strobe command. After being set high, this bit should be cleared by application program. The firmware can check this flag status and determine whether to execute auto calibration in the Light Sleep mode.

Bit 6 **FSYCK_RDY**: FSYCK clock ready flag (ready only)
0: Not ready
1: Ready
This bit is used to indicate that whether the FSYCK clock is ready for operation. This bit will be automatically cleared when FSYCK_EN = 0, when power on reset occurs or when a Deep Sleep command or an Idle command is received.

Bit 5 **XCLK_RDY**: XCLK clock ready flag (ready only)
0: Not ready
1: Ready
This bit is used to indicate whether the XCLK debounce counter is full and XCLK is ready for operation. Note that when exiting the Deep Sleep state, this flag may need a certain period before being set high. This bit will be automatically cleared to zero when XCLK_EN = 0, when RST_LL = 1, when power on reset occurs or when a software reset command, a Deep Sleep command or an Idle command is received.

Bit 4 **XCLK_EN**: XCLK clock enable
0: Disable
1: Enable
Setting this bit high will enable the XCLK path to the baseband block while clearing this bit to zero can save power if required. The XCLK clock should be enabled when writing data to the FIFO.

Bit 3~2 **FSYCK_DIV[1**:0]: FSYCK clock (XCLK division) selection
00: 1/1 XCLK
01: 1/2 XCLK
10: 1/4 XCLK
11: 1/8 XCLK

Bit 1 **FSYCK_EN**: FSYCK clock enable
0: Disable
1: Enable

Bit 0 **RST_LL**: Low voltage (1.2 V) logic reset control
0: Release reset
1: Reset

- **IRQ1: Interrupt Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	RXTO	RXFFOW	—	RXCRCF	RXDETS[1:0]		IRQCPOR	IRQPOR
R/W	R	R	—	R/W	R/W		R/W	R/W
Reset	0	0	0	0	1	0	0	1

Bit 7 **RXTO**: RX time-out flag
0: RX time-out does not occur
1: RX time-out occurs
This flag will be set high by hardware when the RX time-out condition occurs and automatically cleared when a Light Sleep strobe command is received, when the device enters the RX continuous mode, when WOR/WOT wake up occurs or when the device enters the ARK TX/RX mode.

Bit 6 **RXFFOW**: RX FIFO overwrite flag
0: RX FIFO overwrite does not occur
1: RX FIFO overwrite occurs
This flag will be set high by hardware when the RX FIFO overwrite condition occurs and automatically cleared when an RX FIFO reset strobe command or an RX strobe command is received.

Bit 5 Reserved, must be "0"

Bit 4 **RXCRCF**: RX CRC failure flag

Bit 3~2 **RXDETS[1:0]**: RX detect selection
00: Detect carry
01: Reserved
10/11: Detect SYNCWORD

Bit 1 **IRQCPOR**: IRQ flags clearing polarity selection
0: IRQ flags are cleared by writing 0 to the corresponding bits
1: IRQ flags are cleared by writing 1 to the corresponding bits

Bit 0 **IRQPOR**: IRQ signal polarity selection
0: Active low
1: Active high
When an IRQ flag in the IRQ3 register is set high and the corresponding IRQ function is enabled, the active level of the IRQ signal is determined by this configuration.

- **IRQ2: Interrupt Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	ARKTFIE	ATRCTIE	FIFOLTIE	RXERRIE	RXDETIE	CALCMPIE	RXCMPIE	TXCMPIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 7 **ARKTFIE**: ARK TX Failure IRQ Enable
0: Disable
1: Enable

Bit 6 **ATRCTIE**: ATR Cycle Timer IRQ Enable
0: Disable
1: Enable

Bit 5 **FIFOLTIE**: FIFO Low Threshold IRQ Enable
0: Disable
1: Enable

Bit 4 **RXERRIE**: RX Error IRQ Enable
0: Disable
1: Enable

Bit 3 **RXDETIE**: RX Event Detected IRQ Enable
0: Disable
1: Enable

Bit 2 **CALCMPIE**: Calibration Complete IRQ Enable
0: Disable
1: Enable

Bit 1 **RXCMPIE**: RX Complete IRQ Enable
0: Disable
1: Enable

Bit 0 **TXCMPIE**: TX Complete IRQ Enable
0: Disable
1: Enable

- **IRQ3: Interrupt Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	ARKTFIF	ATRCTIF	FIFOLTIF	RXERRIF	RXDETIF	CALCMPIF	RXCMPIF	TXCMPIF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

When the individual flag within this register is set high by the hardware, the corresponding IRQ will be generated. These flags can be cleared by writing 0 or 1 to the corresponding flag which is determined by the IRQCPOR bit configuration.

Bit 7 **ARKTFIF**: ARK TX Failure IRQ Flag
0: No request
1: Interrupt request

Bit 6 **ATRCTIF**: ATR Cycle Timer IRQ Flag
0: No request
1: Interrupt request
This flag will be set high when the ATRCT timer is full.

Bit 5 **FIFOLTIF**: FIFO Low Threshold IRQ Flag
0: No request
1: Interrupt request
When in the Burst TX mode, if this flag is set high, it means that TX FIFO data length is less than FFMG setting threshold and there are TX data to be written into the FIFO. When in the Burst RX mode, if this flag is set high, it means that RX FIFO remaining space is less than FFMG setting threshold and the remaining RX data length is longer than FFMG setting threshold.

Bit 4 **RXERRIF**: RX Error IRQ Flag
0: No request
1: Interrupt request
The RX error conditions include RX failure, CRC failure (CRC_EN = 1) or RX FIFO overwrite.

Bit 3 **RXDETIF**: RX Event Detected IRQ Flag
0: No request
1: Interrupt request
The RX events include carry and syncword, and the actual trigger source is determined by the RXDETS[1:0] configuration.

Bit 2 **CALCMPIF**: Calibration Complete IRQ Flag
0: No request
1: Interrupt request
If ACAL_EN = 0, the LIRC calibration is enabled by its individual calibration enable bit and the calibration completion will trigger IRQ. If ACAL_EN = 1, VCO and RC calibrations are enabled and both completion will trigger IRQ.

Bit 1 **RXCMPIF**: RX Complete IRQ Flag
0: No request
1: Interrupt request
When the RX operation is completed without any error, this flag will be set high by hardware.

Bit 0 **TXCMPIF**: TX Complete IRQ Flag
0: No request
1: Interrupt request

- **IO1: I/O Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	PADDS[1:0]		GIO2S[2:0]			GIO1S[2:0]		
R/W	R/W		R/W			R/W		
POR	0	1	0	0	0	0	0	0

Bit 7~6 **PADDS[1:0]**: PAD driving strength selection (only reset by POR)
00: 0.5 mA
01: 1 mA
10: 5 mA
11: 10 mA

Bit 5~3 **GIO2S[2:0]**: GIO2 pin function selection (only reset by POR)
000/111: No function, input
001: SDO, 4-wire SPI data, output
010: TRXD, direct mode TXD/RXD, input/output
011: TXD, direct mode TXD, input
100: RXD, direct mode RXD, output
101: IRQ, interrupt request, output
110: ROSCi, ATR clock external input

Bit 2~0 **GIO1S[2:0]**: GIO1 pin function selection (only reset by POR)
000/111: No function, input
001: SDO, 4-wire SPI data, output
010: TRXD, direct mode TXD/RXD, input/output
011: TXD, direct mode TXD, intput
100: RXD, direct mode RXD, output
101: IRQ, interrupt request, output
110: ROSCi, ATR clock external input

- **IO2: I/O Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	GIO3S[3:0]			
R/W	—	—	—	—	R/W			
POR	0	0	0	0	0	0	0	0

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **GIO3S[3:0]**: GIO3 pin function selection (only reset by POR)
0000/0111: No function, input
0001: SDO, 4-wire SPI data, output
0010: TRXD, direct mode TXD/RXD, input/output
0011: TXD, direct mode TXD, input
0100: RXD, direct mode RXD, output
0101: IRQ, interrupt request, output
0110: ROSCi, ATR clock external input

1000: TBCLK, TX bit (data) clock, output
1001: RBCLK, RX bit (recovery) clock, output
1010: FSYCK, i.e. XCLK 1/1, 1/2, 1/4, 1/8 output
1011: LIRCCLK, internal LIRC clock with debounce, output
1100: EPA_EN, external PA enable, output
1101: ELAN_EN, external LNA enable, output
1110: TRBCLK, TBCLK in TX mode or RBCLK in RX mode, output
1111: PDB, Power down bar and XO enable, output

- **IO3: I/O Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	SDO_TEN	SPIPU	—	—	GIOPU[3:1]			—
R/W	R/W	R/W	—	—	R/W			—
POR	0	1	1	1	1	1	1	1

Bit 7 **SDO_TEN**: SDO tri-state enable (only reset by POR)
0: Disable
1: Enable

Bit 6 **SPIPU**: 3-wire SPI pull-up enable (only reset by POR)
0: Disable
1: Enable
When this bit is set high, it only controls the pull-up function for the CSN, SCK and SDIO pins. Note that the pull-up function of the SDO pin for the 4-wire SPI is configured using the GIOPU[3:1] bits.

Bit 5~4 Reserved, must be "11"

Bit 3~1 **GIOPU[3:1]**: GIO pin function pull-up enable control (only reset by POR)
These bits control the pull-high function of the GIO3 ~ GIO1 pins respectively.

Bit 0 Reserved, must be "1"

- **FIFO1: FIFO Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TXFFSA[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be "00"

Bit 5~0 **TXFFSA[5:0]**: TX FIFO start address, used for Block FIFO mode

- **FIFO2: FIFO Control Regsiter 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	RXPL2F_EN	FFINF_EN	FFMG_EN	FFMG[1:0]	
R/W	—	—	—	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	1

Bit 7~5 Reserved, must be "000"

Bit 4 **RXPL2F_EN**: RX payload length byte to FIFO enable
0: Disable
1: Enable

Setting this bit high will place the payload length byte in the packet to RX FIFO. In the RX continue mode (RXCON_EN = 1), this bit should be set to 1 to support multiple payload in single RX FIFO.

Bit 3 **FFINF_EN**: FIFO infinite length mode enable
0: Disable
1: Enable

Bit 2 **FFMG_EN**: FIFO length margin detect enable
0: Disable
1: Enable

Bit 1~0 **FFMG[1:0]**: FIFO length margin selection

Threshold of remaining data in TX FIFO:
00: 4 bytes
01: 8 bytes
10: 16 bytes
11: 32 bytes

Threshold of remaining space in RX FIFO:
00: 4 bytes
01: 8 bytes
10: 16 bytes
11: 32 bytes

After the FIFO length margin detect function has been enabled by setting the FFMG_EN bit high and the required FIFO length margin has been selected by setting these bits, when the selected condition occurs the FIFOLTIF flag will be set high. In this case, an interrupt signal will also be generated if the corresponding interrrpt function has been enabled.

- **PKT1: Packet Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	TXPMLEN[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **TXPMLEN[7:0]**: TX preamble length

Transmit preamble length = (TXPMLEN[7:0] + 1) words; the word length, 1 byte or 2 bytes, is further determined by the PMLP_EN and PMLPLEN settings.

- **PKT2: Packet Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	PID[1:0]		TRAILER_EN	WHTFMT[0]	SYNCLEN[1:0]		—	—
R/W	R/W		R/W	R/W	R/W		—	—
Reset	0	0	1	0	0	1	0	0

Bit 7~6 **PID[1:0]**: TX Packet ID

This ID will be placed in the highest two bits of the payload header field when the header option is enabled using the PLH_EN bit.

Bit 5 **TRAILER_EN**: Trailer field enable
0: Disable
1: Enable

Bit 4 **WHTFMT[0]**: Whitening format selection bit 0
WHTFMT[1:0] =
00: RF transceiver, $G(X) = X^7 + X^6 + X^5 + X^4 + 1$
01: PN7, $G(X) = X^7 + X^4 + 1$
10: PN9-CCITT, $G(X) = X^9 + X^5 + 1$
11: PN9-IBM, $G(X) = X^9 + X^5 + 1$
The WHTFMT[1] bit is located in the PKT10 register.

Bit 3~2 **SYNCLEN[1:0]**: TX/RX mode SYNCWORD length setting bit 1 ~ 0
Final SYNCWORD length = ({SYNCLEN[1:0], SYNCLENLB}) + 1; SYNCLENLB is located in the PKT10 register.

Bit 1~0 Reserved, must be "00"

- **PKT3: Packet Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	MCH_EN	FEC_EN	CRC_EN	CRCFMT	PLLEN_EN	PLHAC_EN	PLHLEN	PLH_EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 7 **MCH_EN**: Manchester code enable
0: Disable
1: Enable

Bit 6 **FEC_EN**: FEC enable
0: Disable
1: Enable

Bit 5 **CRC_EN**: CRC field enable
0: Disable
1: Enable

Bit 4 **CRCFMT**: CRC format selection
0: CCITT-16-CRC, $G(X) = X^{16} + X^{12} + X^5 + 1$
1: IBC-16-CRC, $G(X) = X^{16} + X^{15} + X^2 + 1$

Bit 3 **PLLEN_EN**: Payload length field enable
0: Disable
1: Enable

Bit 2 **PLHAC_EN**: Payload header address correction enable control
0: Disable, PLHA[5:0] and PLHEA[7:0] can be used as software flags defined by users.
1: Enable, PLHA[5:0] and PLHEA[7:0] of TX/RX devices must include the same address, otherwise the packet will be regarded as a failed packet.
Note: Whether the PLHEA[7:0] is included or not is determined by the PLHLEN bit setting.

Bit 1 **PLHLEN**: Payload header length
0: 1 byte
1: 2 bytes

Bit 0 **PLH_EN**: Payload header field enable
0: Disable
1: Enable

- **PKT4: Packet Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	WHT_EN	WHTSD[6:0]						
R/W	R/W	R/W						
Reset	0	0	1	1	0	1	1	0

Bit 7 **WHT_EN**: Data whitening enable
0: Disable
1: Enable

Bit 6~0 **WHTSD[6:0]**: Data whitening seed bit 6 ~ 0
WHTSD[8:7] is located in the PKT15 register.

- **PKT5: Packet Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	TXDLEN[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

Bit 7~0 **TXDLEN[7:0]**: TX data length (unit: byte, used in burst mode only)

- **PKT6: Packet Control Register 6**

Bit	7	6	5	4	3	2	1	0
Name	RXDLEN[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

Bit 7~0 **RXDLEN[7:0]**: RX data length (unit: byte; used in burst mode only)
When the PLLEN_EN bit is cleared to 0, the received data length is determined by this field.
When this register is read, the read value indicates the RX data length in FIFO. The default read value is 00h.

- **PKT7: Packet Control Register 7**

Bit	7	6	5	4	3	2	1	0
Name	RXPID[1:0]		DLY_RXS[2:0]			DLY_TXS[2:0]		
R/W	R		R/W			R/W		
Reset	0	0	1	0	0	0	0	0

Bit 7~6 **RXPID[1:0]**: Received packet PID (read only)

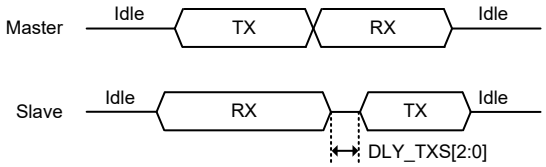
Bit 5~3 **DLY_RXS[2:0]**: RX block stable time after RX is enabled
000: 4 μs
001: 8 μs
010: 12 μs
011: 16 μs
100: 20 μs
101: 32 μs

110: 64 μs
111: 100 μs

These bits are used to select the waiting time between RX enable and RX stable. This time should be configured to a value greater than the default RX DCOC turbo mode delay time of 6 μs.

Bit 2~0 **DLY_TXS[2:0]**: TX start (delay) time before entering the TX mode
000: 0 μs
001: 10 μs
010: 20 μs
011: 40 μs
100: 60 μs
101: 80 μs
110: 100 μs
111: 120 μs

It is used to align the timing between transmitter and receiver in ARK mode.



- **PKT8: Packet Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	—	—	PLHA[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be “00”

Bit 5~0 **PLHA[5:0]**: Payload header address to support broadcast
Address = 0 in RX mode means not doing address correction check.
Write: write data to TX PLHA[5:0]. Read: read data from RX PLHA[5:0].

- **PKT9: Packet Control Register 9**

Bit	7	6	5	4	3	2	1	0
Name	PLHEA[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **PLHEA[7:0]**: Payload header extended address to support broadcast
Address = 0 in RX mode means not doing address correction check.

• MOD1: Modulator Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	DTR[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **DTR[7:0]**

DTR[8:0]: Data rate divider, DTR[8] is loaced in the MOD2 register.

Data Rate = f_{XTAL} / [32 × (DTR[8:0] + 1)], here data rate indicates TBCLK. Note that DTR[8:0] can only be an odd number.

• MOD2: Modulator Control Register 2

Bit	7	6	5	4	3	2	1	0
Name	RXFDOS[11:8]				DITHER[1:0]		—	DTR[8]
R/W	R/W				R/W		—	R/W
Reset	1	0	0	1	0	0	0	0

Bit 7~4 **RXFDOS[11:8]**

RXFDOS[11:0]: RX frequency diavation offset, RXFDOS[7:0] is located in the MOD3 register.

Write to RXFDOS[11:8] first and then write to RXFDOS[7:0] to fully update RXFDOS[11:0].

RXFDOS[11:0] = Floor{(f_{IF} / f_{XTAL}) × 2^{17}}

Bit 3~2 **DITHER[1:0]**: Dither value

Bit 1 Reserved, must be “0”

Bit 0 **DTR[8]**:

DTR[8:0]: Data rate divider, DTR[7:0] is loaced in the MOD1 register.

Data Rate = f_{XTAL} / [32 × (DTR[8:0] + 1)], here data rate indicates TBCLK. Note that DTR[8:0] can only be an odd number.

• MOD3: Modulator Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	RXFDOS[7:0]							
R/W	R/W							
Reset	1	0	0	1	1	0	1	0

Bit 7~0 **RXFDOS[7:0]**

RXFDOS[11:0]: RX frequency diavation offset, RXFDOS[11:8] is loaced in the MOD2 register.

Write to RXFDOS[11:8] first and then write to RXFDOS[7:0] to fully update RXFDOS[11:0].

RXFDOS[11:0] = Floor{(f_{IF} / f_{XTAL}) × 2^{17}}

- **DM1: Demodulator Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	—	MDIV[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	1	1

Bit 7~6 Reserved, must be "00"

Bit 5~0 **MDIV[5:0]**: Demodulator operation clock divider

DMCLK = ADCLK / (MDIV[5:0] + 1)

- **DM2: Demodulator Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	SDR[5:0]					
R/W	—	—	R/W					
Reset	0	0	0	0	0	0	0	0

Bit 7~6 Reserved, must be "00"

Bit 5~0 **SDR[5:0]**: Decimator operation clock after phase extract

SDR[5:0] + 1 = DMCLK / (8 × DATA_RATE), here DATA_RATE indicates RBCLK.

- **DM3: Demodulator Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	CSF_SW_EN	FD_MOD[6:0]						
R/W	R/W	R/W						
Reset	1	1	1	0	0	0	0	0

Bit 7 **CSF_SW_EN**: Channel selection filter auto bandwidth switch enable

0: Disable

1: Enable

Bit 6~0 **FD_MOD[6:0]**: Frequency deviation modifier

FD_MOD = Round((h / (SDR[5:0] + 1)) × 128); h = modulation index

SDR[5:0] + 1 = DMCLK / (8 × DATA_RATE)

- **DM4: Demodulator Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	CFO_DSEL	—	PH_DIFF_MOD	—
R/W	—	—	—	—	R/W	—	R/W	—
Reset	0	0	0	0	1	0	0	0

Bit 7~4 Reserved, must be "0000"

Bit 3 **CFO_DSEL**: CFO correction domain selection

0: Analog domain

1: Digital domain

Bit 2 Reserved, must be "0"

Bit 1 **PH_DIFF_MOD**: Phase difference extract mode setting
0: Phase extract range [-pi/2, pi/2]
1: Phase extract range [-pi, pi]

Bit 0 Reserved, must be "0"

- **DM5: Demodulator Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	FD_HOLD[7:0]							
R/W	R/W							
Reset	0	0	1	1	0	0	0	0

Bit 7~0 **FD_HOLD[7:0]**: Frequency deviation threshold for "preamble + SYNCWORD" detection

- **DM8: Demodulator Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	M_RATIO[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

Bit 7~0 **M_RATIO[7:0]**: For CFO calulation
M_RATIO = round(1 / (MDIV[5:0] + 1) × 2^8)

Bank 0 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value except the LIRC_EN and LIRC_OW bits in the XO3 register. These bits keep unchanged after software reset.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
20h	OM	PWR_SOFT	BAND_SEL[1:0]		—	ACAL_EN	RTX_EN	RTX_SEL	SX_EN
22h	SX1	—	D_N[6:0]						
23h	SX2	D_K[7:0]							
24h	SX3	D_K[15:8]							
25h	SX4	—	—	—	—	D_K[19:16]			
26h	STA1	—	—	—	CD_FLAG	—	OMST[2:0]		
28h	RSSI2	—				RSSI_CTHD[3:0]			
29h	RSSI3	RSSI_NEGDB[7:0]							
2Ah	RSSI4	RSSI_SYNC_OK[7:0]							
2Bh	ATR1	ATRCLK_DIV[1:0]		ATRCLKS	ATRTU	ATRCTM	ATRM[1:0]		ATR_EN
2Ch	ATR2	ATRCYC[7:0]							
2Dh	ATR3	ATRCYC[15:8]							
2Eh	ATR4	ATRRXAP[7:0]							
2Fh	ATR5	ATRRXEP[7:0]							
30h	ATR6	ATRRXEP[15:8]							
31h	ATR7	ARKNM[3:0]				—	ATR_WDLY[1:0]		ARK_EN
32h	ATR8	ARKRXAP[7:0]							
33h	ATR9	ATRCT[7:0]							

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
34h	ATR10	ATRCT[15:8]							
35h	ATR11	ATRCYCM	—				ATRRXAP[10:8]		
36h	PTK10	—	WHTFMT[1]	CRCBYTEO	CRCBITO	CRCINV	SYNCLENLB	PMLPLEN	PMLP_EN
37h	PTK11	PMLPAT[7:0]							
38h	PTK12	PMLPAT[15:8]							
39h	PTK13	CRCSD[7:0]							
3Ah	PTK14	CRCSD[15:8]							
3Bh	PTK15	WHTSD[8:7]		OOKDT_TS[3:0]				OOKDT_POR	OOKDT_EN
3Ch	XO1	XSHIFT[1:0]		—	XO_TRIM[4:0]				
3Dh	XO2	—			XO_SW	—			
3Eh	XO3	LIRCCAL_EN	LIRC_OW	LIRC_OP[4:0]					LIRC_EN
3Fh	TX2	—		CT_PAD[5:0]					

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The reset value shown in the following register description tables means the software reset results of strobe command.

- **OM: Operation Mode Control Register**

Bit	7	6	5	4	3	2	1	0
Name	PWR_SOFT	BAND_SEL[1:0]		—	ACAL_EN	RTX_EN	RTX_SEL	SX_EN
R/W	R/W	R/W		—	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

Bit 7 **PWR_SOFT**: RF operation mode selection
0: RF normal operation mode
1: RF engineering mode

Bit 6~5 **BAND_SEL[1:0]**: Band selection (when PWR_SOFT = 0)
00: 315 MHz band, ODDIV = 4
01: 433 MHz band, ODDIV = 2
10: 470 ~ 510 MHz band, ODDIV = 2
11: 868/915 MHz band, ODDIV = 1

Bit 4 Reserved, must be "0"

Bit 3 **ACAL_EN**: Auto calibration enable
0: Disable
1: Enable
When this bit is set high, both the VCO and RC calibrations will be enabled. When the VCO and RC calibrations are completed, this bit will be cleared to zero by hardware.

Bit 2 **RTX_EN**: RX or TX mode enable
0: Disable
1: Enable
After the RX or TX mode has been selected by the RTX_SEL bit, setting this bit high will enable the selected mode.

Bit 1 **RTX_SEL**: RX or TX mode selection
0: RX mode
1: TX mode

Bit 0 **SX_EN**: Synthesizer enable (standby mode enable control)
0: Disable
1: Enable
Setting this bit high will enable the PFD, CP and VCO functions.

- **SX1: Fractional-N Synthesizer Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	—	D_N[6:0]						
R/W	—	R/W						
Reset	0	0	1	1	0	1	1	0

Bit 7 Reserved, must be "0"

Bit 6~0 **D_N[6:0]**: RF channel integer number code
D_N[6:0] = floor(f_{RF} × ODDIV / f_{XTAL})
For example, XO = 16 MHz and RF band = 433.92 MHz which are initial setup:
→ (433.92 MHz × 2) / 16 MHz = 54.24
→ D_N = 54
→ Dec2Hex(54) = 36
→ Dec2Bin(54) = 011_0110

- **SX2: Fractional-N Synthesizer Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	D_K[7:0]							
R/W	R/W							
Reset	0	0	0	0	1	0	1	0

Bit 7~0 **D_K[7:0]**: RF channel fractional number code lowest byte

- **SX3: Fractional-N Synthesizer Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	D_K[15:8]							
R/W	R/W							
Reset	1	1	0	1	0	1	1	1

Bit 7~0 **D_K[15:8]**: RF channel fractional number code medium byte

• SX4: Fractional-N Synthesizer Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	D_K[19:16]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	0	0	1	1

Bit 7~4 Reserved, must be "0000"

Bit 3~0 **D_K[19:16]**: RF channel fractional number code highest byte

$D\_K[19:0] = floor\{(f_{RF} \times ODDIV / f_{XTAL} - D\_N[6:0]) \times 2^{20}\}$

For example, XO = 16 MHz and RF band = 433.92 MHz which are initial setup:

→ (433.92 MHz × 2) / 16 MHz = 54.24

→ D_K = 0.24 × 220 = 251658

→ Dec2Hex(251658) = 3D70A

→ Dec2Bin(251658) = 0011_1101 + 0111_0000_1010

• STA1: Status Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	CD_FLAG	—	OMST[2:0]		
R/W	—	—	—	R	—	R		
Reset	0	0	0	0	0	0	0	0

Bit 7~5 Reserved, must be "000"

Bit 4 **CD_FLAG**: Carrier detection flag (read only)

This flag will be set high by hardware when carrier detection is okey after pulling DEMOD_EN high. Here DEMOD_EN high level is an internal signal which is generated by the internal state machine when in the Direct mode (DIR_EN = 1) or after the RX strobe command is received when in the Burst mode (DIR_EN = 0). The flag will be automatically cleared when RX_EN rising edge occurs. Here RX_EN rising edge is generated after setting RTX_SEL = 0 and RTX_EN = 1 when in the Direct mode or by the internal state machine after the RX strobe command is received when in the Burst mode.

Bit 3 Reserved, must be "0"

Bit 2~0 **OMST[2:0]**: Operation mode state indication (read only)

000: Deep Sleep mode
001: Idle mode
010: Light Sleep mode
011: Standby mode
100: TX mode
101: RX mode
110: VCO calibration mode
111: Undefined

- **RSSI2: RSSI Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	RSSI_CTHD[3:0]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	1	0	1	0

Bit 7~4 Reserved, must be "0000"

Bit 3~0 **RSSI_CTHD[3:0]**: RSSI threshold for carrier detection
(RSSI_CTHD[3:0] × 2 + 1) + 74 = RSSI threshold for carrier detection

- **RSSI3: RSSI Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	RSSI_NEGDB[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RSSI_NEGDB[7:0]**: RSSI value (unit: -dB)
It is a real time measurement value.

- **RSSI4: RSSI Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	RSSI_SYNC_OK[7:0]							
R/W	R							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **RSSI_SYNC_OK[7:0]**: RSSI snapshot when SYNCWORD is detected correct

- **ATR1: Auto TX/RX Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	ATRCLK_DIV[1:0]		ATRCLKS	ATRTU	ATRCTM	ATRM[1:0]		ATR_EN
R/W	R/W		R/W	R/W	R/W	R/W		R/W
Reset	1	1	0	0	1	0	0	0

Bit 7~6 **ATRCLK_DIV[1:0]**: ATR clock frequency division selection
00: 1/1, ATRCLK = 32768 Hz
01: 1/4, ATRCLK = 8192 Hz
10: 1/8, ATRCLK = 4096 Hz
11: 1/16, ATRCLK = 2048 Hz

Bit 5 **ATRCLKS**: ATRCLK clock source selection
0: From the internal LIRC clock
1: From the exteral ROSCi clock input on the GIOx pin

Bit 4 **ATRTU**: Auto TRX unit time selection
0: 250 μs
1: 1 ms, used to support low data rate applications
This bit is used to select the unit time for the ATR RX active period (ATRRXAP[10:0]), ATR RX extended period (ATRRXEP[15:0]) and ARK RX active period (ARKRXAP[7:0]).

Bit 3 **ATRCTM**: Auto TRX timer mode selection
0: Single mode, restart ATRCT timer when every ATR transaction occurs.
1: Continuous mode, start ATRCT timer upon receiving Idle command; stop ATRCT timer when ATR_EN = 0 or ATRCTM = 0 and exit the ATR active period.

Bit 2~1 **ATRM[1:0]**: Auto TRX mode selection
00: ATR WOT mode
01: ATR WOR mode
10/11: ATR WTM mode

Bit 0 **ATR_EN**: Auto TRX enable
0: Disable
1: Enable

Note that the ATR functions are activated by operation state transition from Deep Sleep/Light Sleep mode to Idle mode.

- **ATR2: Auto TX/RX Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	ATRCYC[7:0]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **ATRCYC[7:0]**: ATRCT timer expire value low byte

- **ATR3: Auto TX/RX Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	ATRCYC[15:8]							
R/W	R/W							
Reset	0	0	0	0	1	1	1	1

Bit 7~0 **ATRCYC[15:8]**: ATRCT timer expire value high byte
ATRCYCM = 0 – BC3601/BC3602 compatible mode (default):
Wake-up period = ATRCLK period × ATRCYC[15:0] + LIRCCLK period, ATRCYC[15:0] ≠ 0. Default wake-up period is 2 seconds.
ATRCYCM = 1 – RF module mode:
Wake-up period = ATRCLK period × (ATRCYC[15:0] + 1), ATRCYC[15:0] ≠ 0. Default wake-up period is 2 seconds.

- **ATR4: Auto TX/RX Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	ATRRXAP[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	1	1	1

Bit 7~0 **ATRRXAP[7:0]**: ATR RX active period low byte
ATR RX active period high byte ATRRXAP[10:8] is located in the ATR11 register.
Active period = unit time × (ATRRXAP[10:0] + 1); the unit time can be 250 μs or 1 ms which is determined by the ATRTU bit. The default ATR RX active period is 10 ms with a default time unit of 250 μs.

- **ATR5: Auto TX/RX Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	ATRRXEP[7:0]							
R/W	R/W							
Reset	1	0	0	0	1	1	1	1

Bit 7~0 **ATRRXEP[7:0]**: ATR RX extend period low byte

- **ATR6: Auto TX/RX Control Register 6**

Bit	7	6	5	4	3	2	1	0
Name	ATRRXEP[15:8]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	1

Bit 7~0 **ATRRXEP[15:8]**: ATR RX extended period high byte
Extended period = unit time × (ATRRXEP[15:0] + 1); the unit time can be 250 μs or 1 ms which is determined by the ATRTU bit. The default ATR RX extended period is 100 ms with a default time unit of 250 μs.

- **ATR7: Auto TX/RX Control Register 7**

Bit	7	6	5	4	3	2	1	0
Name	ARKNM[3:0]				—	ATR_WDLY[1:0]		ARK_EN
R/W	R/W				—	R/W		R/W
Reset	0	1	1	1	0	0	1	0

Bit 7~4 **ARKNM[3:0]**: ARK repeat cycle number
Maximum repeat cycle number = ARKNM[3:0] + 1

Bit 3 Reserved, must be "0"

Bit 2~1 **ATR_WDLY[1:0]**: Auto wake-up delay time
00: 244 μs
01: 488 μs
10: 732 μs
11: 976 μs

Bit 0 **ARK_EN**: Auto-Resend/ACK enable
0: Disable
1: Enable

- **ATR8: Auto TX/RX Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	ARKRXAP[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	1	1	1

Bit 7~0 **ARKRXAP[7:0]**: ARK RX active period
Active period = unit time × (ARKRXAP[7:0] + 1); the unit time can be 250 μs or 1 ms which is determined by the ATRTU bit. The default ARK RX active period is 10 ms with a default time unit of 250 μs.

• ATR9: Auto TX/RX Control Register 9

Bit	7	6	5	4	3	2	1	0
Name	ATRCT[7:0]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATRCT[7:0]**: ATR cycle timer low byte

• ATR10: Auto TX/RX Control Register 10

Bit	7	6	5	4	3	2	1	0
Name	ATRCT[15:8]							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

Bit 7~0 **ATRCT[15:8]**: ATR cycle timer high byte

Reading ATRCT[15:0] will get the current counting value. Due to the limitation of SPI 8-bit data length, reading the ATR9 register will take a snapshot of the whole 16-bit data into the read register buffer. Users should read ATR9 and ATR10 continuously (non-interrupted) to get correct data.

Writing to ATRCT[15:0] will update the counting value. Write to ATR9 first and then write to ATR10 to trigger the ATRCT write function. This timer update mechanism is used to align the time slot for the master and slave in a two-way RF system.

• ATR11: Auto TX/RX Control Register 11

Bit	7	6	5	4	3	2	1	0
Name	ATRCYCM	—	—	—	—	ATRRXAP[10:8]		
R/W	R/W	—	—	—	—	R/W		
Reset	0	0	0	0	0	0	0	0

Bit 7 **ATRCYCM**: ATR cycle calculation mode
0: BC3601/BC3602/BC66F36x2 compatible mode
1: HT32F67233 mode

Refer to the ATR2 and ATR3 registers for more cycle calculation details.

Bit 6~3 Reserved, must be “0000”

Bit 2~0 **ATRRXAP[10:8]**: ATR RX active period high byte

ATR RX active period low byte ATRRXAP[7:0] is located in the ATR4 register.

Active period = unit time × (ATRRXAP[10:0] + 1); the unit time can be 250 μs or 1 ms which is determined by the ATRTU bit. The default ATR RX active period is 10 ms with a default time unit of 250 μs.

- **PKT10: Packet Control Register 10**

Bit	7	6	5	4	3	2	1	0
Name	—	WHTFMT[1]	CRCBYTEO	CRCBITO	CRCINV	SYNCLENLB	PMLPLEN	PMLP_EN
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	1	0	0

Bit 7 Reserved, must be "0"

Bit 6 **WHTFMT[1]**: Whitening format selection bit 1

WHTFMT[1:0] =

00: RF transceiver, $G(X) = X^7 + X^6 + X^5 + X^4 + 1$

01: PN7, $G(X) = X^7 + X^4 + 1$

10: PN9-CCITT, $G(X) = X^9 + X^5 + 1$

11: PN9-IBM, $G(X) = X^9 + X^5 + 1$

The WHTFMT[0] bit is located in the PKT2 register.

Bit 5 **CRCBYTEO**: CRC byte order

0: CRC high byte first

1: CRC low byte first

Bit 4 **CRCBITO**: CRC bit order

0: CRC high bit first

1: CRC low bit first

Bit 3 **CRCINV**: CRC bit inverse function control

0: Non-inverse

1: Inverse

Bit 2 **SYNCLENLB**: TX/RX mode SYNCWORD length setting lowest bit

Final SYNCWORD length = ({SYNCLEN[1:0], SYNCLENLB) + 1; SYNCLEN[1:0] is located in the PKT2 register.

Bit 1 **PMLPLEN**: Preamble pattern length selection (when PMLP_EN = 1)

0: 1 byte – PMLPAT[7:0]

1: 2 bytes – PMLPAT[15:0], low byte first

Bit 0 **PMLP_EN**: Preamble pattern selection

0: Preamble pattern is derived from "SYNCWORD MSB + 1/0 toggle"

Ex: SYNCWORD MSB = 0, preamble = 01010101(b)

SYNCWORD MSB = 1, preamble = 10101010(b)

1: Preamble pattern is derived from PMLPAT[15:0]

- **PKT11: Packet Control Register 11**

Bit	7	6	5	4	3	2	1	0
Name	PMLPAT[7:0]							
R/W	R/W							
Reset	0	1	0	1	0	1	0	1

Bit 7~0 **PMLPAT[7:0]**: Preamble pattern low byte

- **PKT12: Packet Control Register 12**

Bit	7	6	5	4	3	2	1	0
Name	PMLPAT[15:8]							
R/W	R/W							
Reset	0	1	0	1	0	1	0	1

Bit 7~0 **PMLPAT[15:8]**: Preamble pattern high byte

- **PKT13: Packet Control Register 13**

Bit	7	6	5	4	3	2	1	0
Name	CRCSD[7:0]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **CRCSD[7:0]**: CRC seed low byte

- **PKT14: Packet Control Register 14**

Bit	7	6	5	4	3	2	1	0
Name	CRCSD[15:8]							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

Bit 7~0 **CRCSD[15:8]**: CRC seed high byte

- **PKT15: Packet Control Register 15**

Bit	7	6	5	4	3	2	1	0
Name	WHTSD[8:7]		OOKDT_TS[3:0]				OOKDT_POR	OOKDT_EN
R/W	R/W		R/W				R/W	R/W
Reset	0	0	0	1	0	1	0	1

Bit 7~6 **WHTSD[8:7]**: Data whitening seed bit 8 ~ 7
WHTSD[6:0] is located in the PKT4 register. Note that only PN9-CCIT and PN9-IBM data whitening polynomials use the entire WHTSD[8:0] 9 bits.

Bit 5~2 **OOKDT_TS[3:0]**: OOK duty cycle tuning time selection
0000: 2 μs
0001: 4 μs
0010: 6 μs
0011: 8 μs
....(step: 2 μs)
1100: 26 μs
1101: 28 μs
1110: 30 μs
1111: 32 μs

Bit 1 **OOKDT_POR**: OOK duty cycle tuning polarity
0: Extend 0 duty cycle
1: Extend 1 duty cycle

Bit 0 **OOKDT_EN**: OOK duty cycle tuning enable
0: Disable
1: Enable

- **XO1: XO Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	XSHIFT[1:0]		—	XO_TRIM[4:0]				
R/W	R/W		—	R/W				
Reset	0	0	0	1	0	0	0	0

Bit 7~6 **XSHIFT[1:0]**: Coarse tune of XO load capacitor for different crystal C_{LOAD}
Bit 5 Reserved, must be set to "1"
Bit 4~0 **XO_TRIM[4:0]**: Fine tune of XO load capacitor

- **XO2: XO Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	XO_SW	—	—	—	—
R/W	—	—	—	R/W	—	—	—	—
Reset	0	0	0	0	0	0	1	1

Bit 7~5 Reserved, must be "000"
Bit 4 **XO_SW**: Crystal oscillator load capacitance switch
0: About 12 ~ 16 pF
1: About 8 ~ 12 pF
Bit 3~0 Reserved, must be "0011"

- **XO3: XO Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	LIRCCAL_EN	LIRC_OW	LIRC_OP[4:0]					LIRC_EN
R/W	R/W	R/W	R/W					R/W
POR	—	0	—	—	—	—	—	0
Reset	0	—	0	1	1	0	1	—

Bit 7 **LIRCCAL_EN**: LIRC calibration enable
0: Disable
1: Enable
Bit 6 **LIRC_OW**: LIRC overwrite control (only reset by POR)
0: LIRC_OP[4:0] from calibration engine
1: LIRC_OP[4:0] from control register
Bit 5~1 **LIRC_OP[4:0]**: LIRC trim
After writing data to LIRC_OP[4:0], this trim will become active when the LIRC_OW bit is set high. When reading data from LIRC_OP[4:0], the actual data source is determined by the LIRC_OW bit setting.
Bit 0 **LIRC_EN**: LIRC enable (only reset by POR)
0: Disable
1: Enable

- **TX2: TX Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	CT_PAD[5:0]					
R/W	—	—	R/W					
Reset	0	0	1	1	0	0	0	0

Bit 7~6 Reserved, must be "00"

Bit 5~0 **CT_PAD[5:0]**: TX PAD linear power control

Bank 1 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
20h	AGC1	MPT_0DB_EN	—	OFFSET_HBSEL[2:0]			OFFSET_LBSEL[2:0]		
21h	AGC2	—			DBFS_OFFSET[2:0]			AGC_CMP_THD[1:0]	
22h	AGC3	—					IF_DETOK_THD[2:0]		
23h	AGC4	GAIN_SEL[3:0]				—	AGC_ST[2:0]		
26h	AGC7	GAIN_STB[7:0]							
2Ch	FCF1	—	—	SFRATIO[1:0]		GFD_COMP[3:0]			
2Dh	FCF2	FSCALE[7:0]							
2Eh	FCF3	—				FSCALE[11:8]			
2Fh	FCF4	CF_B12[7:0]							
30h	FCF5	—						CF_B12[9:8]	
31h	FCF6	CF_B13[7:0]							
32h	FCF7	—						CF_B13[9:8]	
33h	FCF8	CF_A12[7:0]							
34h	FCF9	—						CF_A12[9:8]	
35h	FCF10	CF_A13[7:0]							
36h	FCF11	—						CF_A13[9:8]	
37h	FCF12	CF_B22[7:0]							
38h	FCF13	—						CF_B22[9:8]	
39h	FCF14	CF_B23[7:0]							
3Ah	FCF15	—						CF_B23[9:8]	
3Bh	FCF16	CF_A22[7:0]							
3Ch	FCF17	—						CF_A22[9:8]	
3Dh	FCF18	CF_A23[7:0]							
3Eh	FCF19	—						CF_A23[9:8]	

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The reset value shown in the following register description tables means the software reset results of strobe command.

- **AGC1: AGC Control Register 1**

Bit	7	6	5	4	3	2	1	0
Name	MPT_0DB_EN	—	OFFSET_HBSEL[2:0]			OFFSET_LBSEL[2:0]		
R/W	R/W	—	R/W			R/W		
Reset	0	0	0	1	1	0	0	0

Bit 7 **MPT_0DB_EN**: Force Curve1 max point = 0dB
0: Disable
1: Enable

Bit 6 Reserved, must be "0"

Bit 5~3 **OFFSET_HBSEL[2:0]**: AGC max point selection
max point = -6 + 2 × offset_HB

Bit 2~0 **OFFSET_LBSEL[2:0]**: AGC min point select
min point = max point - 22 + 2 × offset_LB

OFFSET_HBSEL[2:0]	offset_HB
000	0
001	1
010	2
011	3
100	-4
101	-3
110	-2
111	-1

OFFSET_LBSEL[2:0]	offset_LB
000	0
001	1
010	2
011	3
100	-4
101	-3
110	-2
111	-1

Ex: OFFSET_HBSEL[2:0] = 011, offset_HB = +3; OFFSET_LBSEL[2:0] = 000, offset_LB = +0;
AGC max point = -6 + 2 × 3 = 0dBFs; AGC min point = 0 - 22 + 2 × 0 = -22dBFs

- **AGC2: AGC Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	DBFS_OFFSET[2:0]			AGC_CMP_THD[1:0]	
R/W	—	—	—	R/W			R/W	
Reset	0	0	0	1	0	1	0	0

Bit 7~5 Reserved, must be "000"

Bit 4~2 **DBFS_OFFSET[2:0]**: Log offset for GFSK

Bit 1~0 **AGC_CMP_THD[1:0]**: AGC comparison number threshold
00: Continuous AGC comparison until SYNCWORD is detected
01 ~ 11: Comparison number threshold

• AGC3: AGC Control Register 3

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	IF_DETOK_THD[2:0]		
R/W	—	—	—	—	—	R/W		
Reset	0	0	0	0	0	1	0	0

Bit 7~3 Reserved, must be "00000"

Bit 2~0 **IF_DETOK_THD[2:0]**: IF detection OK threshold

After the gain stable time which determined by the AGC7 register, the AGC circuit will wait for (IF_DETOK_THD[2:0] × 8) ADCLK cycles before starting to detect the IF signal strength.

• AGC4: AGC Control Register 4

Bit	7	6	5	4	3	2	1	0
Name	GAIN_SEL[3:0]				—	AGC_ST[2:0]		
R/W	R				—	R		
Reset	0	0	0	1	0	0	0	1

Bit 7~4 **GAIN_SEL[3:0]**: Gain curve selection

Bit 3 Reserved, must be "0"

Bit 2~0 **AGC_ST[2:0]**: AGC state machine state

100: AGC is completed

• AGC7: AGC Control Register 7

Bit	7	6	5	4	3	2	1	0
Name	GAIN_STB[7:0]							
R/W	R/W							
Reset	0	0	1	1	0	0	0	0

Bit 7~0 **GAIN_STB[7:0]**: Gain stable count

Gain stable count delay in ADCLK period = GAIN_STB[7:0] × 2

• FCF1: Filter Coefficient Control Register 1

Bit	7	6	5	4	3	2	1	0
Name	—	—	SFRATIO[1:0]		GFD_COMP[3:0]			
R/W	—	—	R/W		R/W			
Reset	0	0	0	0	0	1	1	0

Bit 7~6 Reserved, must be "00"

Bit 5~4 **SFRATIO[1:0]**: Smooth filter ratio selection

00: 1/1

01: 1/16

10: 1/64

11: 1/128

Bit 3~0 **GFD_COMP[3:0]**: Compensate gaussian filter for 101/010 pattern
[3]: 1/8; [2]: 1/16; [1]: 1/32; [0]: 1/64
For example:
0000: no eompensation
….
1111: value after compensation = (1 + 0.234375)x = [1 + (1/8 + 1/16 + 1/32 + 1/64)]x

- **FCF2: Filter Coefficient Control Register 2**

Bit	7	6	5	4	3	2	1	0
Name	FSCALE[7:0]							
R/W	R/W							
Reset	0	1	0	0	0	1	0	0

Bit 7~0 **FSCALE[7:0]**: Frequency deviation scale parameter low byte

- **FCF3: Filter Coefficient Control Register 3**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	FSCALE[11:8]			
R/W	—	—	—	—	R/W			
Reset	0	0	0	0	0	1	0	0

Bit 7~4 Reserved, must be “0000”

Bit 3~0 **FSCALE[11:8]**: Frequency deviation scale parameter high byte
If the data rate is in the range of 250 Kbps ~ 100 Kbps, the pre-filter is required.
$FSCALE[11:0] = round\{(h \times f_S / f_{XTAL}) \times 2^{15}\}$
where h = (2 × frequency deviation) / (data rate).
Here “h” is the modulation index calculated from frequency deviation and data rate.

- **FCF4: Filter Coefficient Control Register 4**

Bit	7	6	5	4	3	2	1	0
Name	CF_B12[7:0]							
R/W	R/W							
Reset	1	0	0	0	0	1	0	1

- **FCF5: Filter Coefficient Control Register 5**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B12[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	0

- **FCF6: Filter Coefficient Control Register 6**

Bit	7	6	5	4	3	2	1	0
Name	CF_B13[7:0]							
R/W	R/W							
Reset	1	0	0	0	1	0	1	0

- **FCF7: Filter Coefficient Control Register 7**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B13[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

- **FCF8: Filter Coefficient Control Register 8**

Bit	7	6	5	4	3	2	1	0
Name	CF_A12[7:0]							
R/W	R/W							
Reset	0	0	0	1	0	0	1	0

- **FCF9: Filter Coefficient Control Register 9**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A12[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

When the data rate is in the range of 49 Kbps ~ 2 Kbps, the following smooth filter is needed.

$CF\_A12[9:0] = mod(2^{10} + [(SFRATIO[1:0] - 1) \times 2^{8}], 2^{10})$

- **FCF10: Filter Coefficient Control Register 10**

Bit	7	6	5	4	3	2	1	0
Name	CF_A13[7:0]							
R/W	R/W							
Reset	0	0	1	0	1	0	1	1

- **FCF11: Filter Coefficient Control Register 11**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A13[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	1	1

- **FCF12: Filter Coefficient Control Register 12**

Bit	7	6	5	4	3	2	1	0
Name	CF_B22[7:0]							
R/W	R/W							
Reset	0	0	0	1	0	1	0	0

- **FCF13: Filter Coefficient Control Register 13**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B22[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	1

- **FCF14: Filter Coefficient Control Register 14**

Bit	7	6	5	4	3	2	1	0
Name	CF_B23[7:0]							
R/W	R/W							
Reset	0	0	1	0	0	0	0	1

- **FCF15: Filter Coefficient Control Register 15**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_B23[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

- **FCF16: Filter Coefficient Control Register 16**

Bit	7	6	5	4	3	2	1	0
Name	CF_A22[7:0]							
R/W	R/W							
Reset	0	1	1	1	1	0	0	0

- **FCF17: Filter Coefficient Control Register 17**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A22[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

- **FCF18: Filter Coefficient Control Register 18**

Bit	7	6	5	4	3	2	1	0
Name	CF_A23[7:0]							
R/W	R/W							
Reset	0	0	1	0	1	0	0	0

- **FCF19: Filter Coefficient Control Register 19**

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	CF_A23[9:8]	
R/W	—	—	—	—	—	—	R/W	
Reset	0	0	0	0	0	0	0	0

The FCF4 ~ FCF19 regsiters define eight groups of IIR coefficients, their recommended settings for different XTAL clock conditions are listed below.

f_{XTAL}	16 MHz	16 MHz	16 MHz	16 MHz	16 MHz
f_S	250 Kbps	125 Kbps	50 Kbps	10 Kbps	2 Kbps
f_D	93.75 kHz	46.875 kHz	18.75 kHz	40 kHz	8 kHz
D_K[19:0] (H)	f_{RF} × ODDIV / f_{XTAL}, take decimal number				
D_N[6:0] (H)	f_{RF} × ODDIV / f_{XTAL}, take integer number				
SFRATIO[1:0] (D)	0	0	0	1	3
FSCALE[11:0] (H)	294	119	4C	A4	20
CF_B12[9:0] (H)	2CA	01D	0	0	0
CF_B13[9:0] (H)	62	346	0	0	0
CF_A12[9:0] (H)	358	22	0	310	302
CF_A13[9:0] (H)	3E9	331	0	0	0
CF_B22[9:0] (H)	3B3	386	0	0	0
CF_B23[9:0] (H)	3E	12	0	0	0
CF_A22[9:0] (H)	3E9	8	0	0	0
CF_A23[9:0] (H)	39	8	0	0	0

Bank 2 Control Registers

All control registers will be set to their initial value by power-on reset (POR). The software reset will set the control registers to their initial value.

Addr.	Name	Bit							
		7	6	5	4	3	2	1	0
21h	CFG0	Reserved							
2Eh	CFG1	Reserved							
2Fh	CFG2	Reserved							
33h	CFG3	Reserved							
34h	CFG4	Reserved							
39h	CFG5	Reserved							

Note: The addresses which are not listed in this table are reserved for future use, it is suggested not to change their initial values by any methods.

The recommended values for the Bank 2 registers are listed below:

Addr.	Name	Frequency Band	
		433 MHz	868 MHz
21h	CFG0	97h	
2Eh	CFG1	68h	
2Fh	CFG2	16h (≤ 50 Kbps: 06h)	96h (≤ 50 Kbps: 86h)
33h	CFG3	01h(OOK mode) / 41h(FSK mode)	
34h	CFG4	90h	
39h	CFG5	9Ch	

Special Function Description

Sub-1GHz RF Transceiver

The RF module adopts a fully-integrated, low-IF receiver architrecture. The received RF signal is first amplified by a low noise amplifier (LNA), after which the frequency is down-converted to an intermediate frequency (IF) by a quadrature mixer. The mixer output is filtered by a channel-selected filter which rejects the unwanted out-of-band (OOB) interference and image signals. After filtering, the IF signal is amplified by a analog programmable gain amplifier (PGA). Then the IF signal is digitized by a 10-bit ΣΔ ADC.

The RF module features an Automatic Gain Control (AGC) unit to adjust the receiver gain according to the RSSI, generated at the digital modem. The AGC enables the RF module to operate from sensitivity level to +10 dBm input power.

The RF module adopts a fully integrated fractional-N synthesizer which includes RF VCO, loop filter, digital controlled XO (DCXO) and integrated load capacitors for XO. Placing VCO load inductor on the PCB is to lower VCO resonant frequency to achieve an RX mode current consumption low to 5.4 mA. The fractional-N synthesizer architecture allows the users to extend their potential usage to a wider frequency range.

The transmit session is a VCO direct modulation architecture. Different from the conventional direct up-conversion transmitters, the GFSK modulation signal is fed into the VCO directly to take advantange of fractional-N synthesizer. As a result, both layout area and current consumption are much smaller compared with direct up-conversion transmitters. The fine resolution can generate a low FSK error GFSK signal. The modulated signal is fed into a Class-E Power Amplifier (PA) and the maximum output power can be up to +20 dBm.

Serial Interface

The RF module communicates with a MCU via a 3-wire SPI interface (CSN, SCK, SDIO) or a 4-wire SPI interface (SDO from GIO1 or GIO2) with a data rate up to 4Mbps. An SPI transmission is an (8 + 8 × n) bits sequence which consists of an 8-bit command and n × 8 bits of data, where n can be 0 or any natural number. If the number n is greater than the address boundary, the address will return to zero. The MCU should pull the CSN (SPI chip select) pin low in order to access the RF module. Using the SPI interface, user can access the control registers and issue Strobe commands. When writing data to the RF chip, the SPI data will be latched into the registers at the rising edge of the SCK signal. When reading data from the RF chip registers, the bit data will be transferred at the falling edge of the SCK signal after the target register address has been input.

Table 3. SPI Command Format

Command (8 bits)								Data (8 bits)							
C7	C6	C5	C4	C3	C2	C1	C0	D7	D6	D5	D4	D3	D2	D1	D0

Two kinds of command are defined. One is 1-byte command only, named CmdO, and the other is 1-byte command followed by n-byte data, named CmdD.

C7	C6	C5	C4	C3	C2	C1	C0	Description	CmdO	CmdD
0	1	A5	A4	A3	A2	A1	A0	Write to control registers		√
1	1	A5	A4	A3	A2	A1	A0	Read from control registers		√
0	0	1	x	x	x	B1	B0	Set register bank	√	
0	0	0	1	x	x	x	0	Write SYNCWORD command		√
1	0	0	1	x	x	x	0	Read SYNCWORD command		√
0	0	0	1	x	x	x	1	TX FIFO write command		√
1	0	0	1	x	x	x	1	RX FIFO read command		√
1	0	0	1	1	1	1	1	Read Chip ID command		√
0	0	0	0	1	0	0	0	Software reset command	√	
0	0	0	0	1	0	0	1	TX FIFO address pointer reset command	√	
1	0	0	0	1	0	0	1	RX FIFO address pointer reset command	√	
0	0	0	0	1	0	1	0	Deep Sleep mode	√	
0	0	0	0	1	0	1	1	Idle mode	√	
0	0	0	0	1	1	0	0	Light Sleep mode	√	
0	0	0	0	1	1	0	1	Standby mode	√	
0	0	0	0	1	1	1	0	TX mode	√	
1	0	0	0	1	1	1	0	RX mode	√	

A5 ~ A0: The address of control registers;

x: Hardware doesn't care but it is recommended to set to 0 by software;

B1 ~ B0: Bank number.

Note: 1. The chip supports multi-byte read/write operations and the address is increased automatically after each read or write operation.
2. Using software to read/write multiple bytes is allowed after one read/write command in a single CSN enabled cycle.
3. In the sleep mode, GIOs will keep the same level of the last operation mode.

SPI Timing

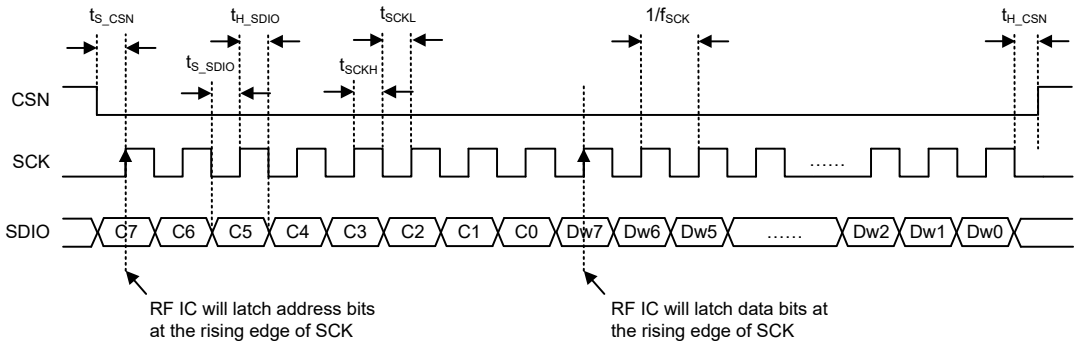


Figure 6. 3-Wire SPI Interface Write 1-byte Data Operation

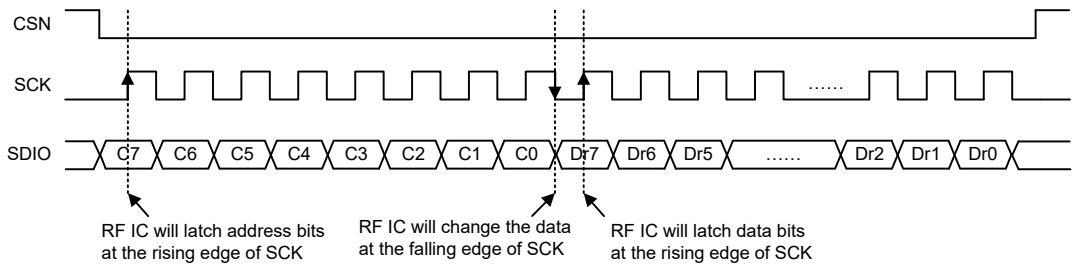


Figure 7. 3-Wire SPI Interface Read 1-byte Data Operation

System Clock

The main system clock of the RF module comes from the X'tal oscillator. All internal operation clocks of various functional blocks are derived from the X'tal oscillator.

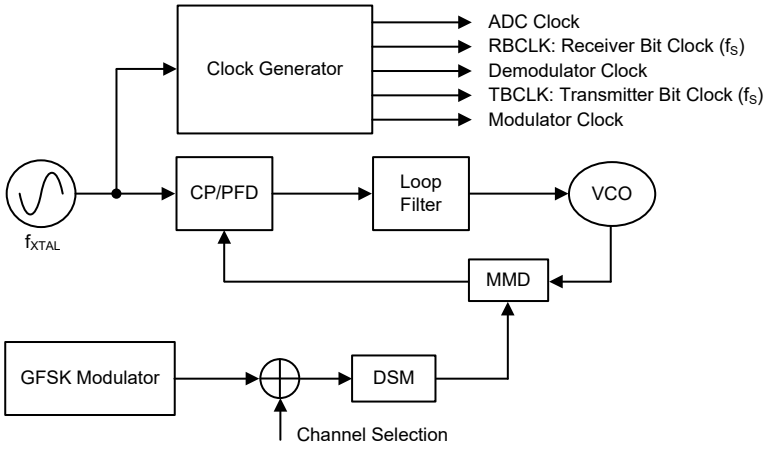


Figure 8. RF Transceiver System Clock

Frequency Synthesizer

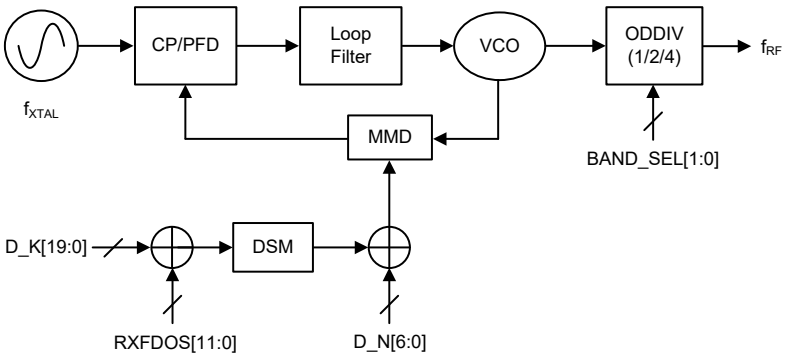


Figure 9. RF Transceiver Frequency Synthesizer

The RF transceiver frequency is generated by a high resolution fractional-N Delta Sigma frequency synthesizer. By appropriate setting on the configuration parameters D_N[6:0] and D_K[19:0], a low-noise LO frequency can be generated to comply with various radio regulatory standards including ETSI EN, FCC, etc.

$$D\_N[6:0] = Floor(\frac{f_{RF} \times ODDIV}{f_{XTAL}})$$

$$D\_K[19:0] = Floor((\frac{f_{RF} \times ODDIV}{f_{XTAL}} - D\_N[6:0]) \times 2^{20})$$

$$RXFDOS[11:0] = Floor((\frac{f_{IF}}{f_{XTAL}}) \times 2^{17})$$

State Machine

There are seven operating modes in the RF module. The operation modes and key funcitons on/off state in the corresponding mode are listed below.

1. Power Down mode
2. Deep Sleep mode
3. Light Sleep mode
4. Standby mode
5. Idle mode
6. TX mode
7. RX mode

Mode	Register Retention	3.3 V	LIRC	Regulator	XO	Standby + VCO	TX	RX	Strobe Command
Power Down	No	OFF	OFF	OFF	OFF	OFF	OFF	OFF	—
Deep Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	OFF	0000_1010
Light Sleep	Yes	ON	OFF	ON	ON	OFF	OFF	OFF	0000_1100
Idle	Yes	ON	ON	OFF	OFF	OFF	OFF	OFF	0000_1011
Standby	Yes	ON	OFF	ON	ON	ON	OFF	OFF	0000_1101
TX	Yes	ON	OFF	ON	ON	ON	ON	OFF	0000_1110
RX	Yes	ON	OFF	ON	ON	ON	OFF	ON	1000_1110

TX/RX FIFO Mode (DIR_EN = 0) State Machine

If the DIR_EN bit is cleared to 0, the device mode transactions are implemented by strobe command from the MCU and the TX/RX data are derived from the packet handling hardware.

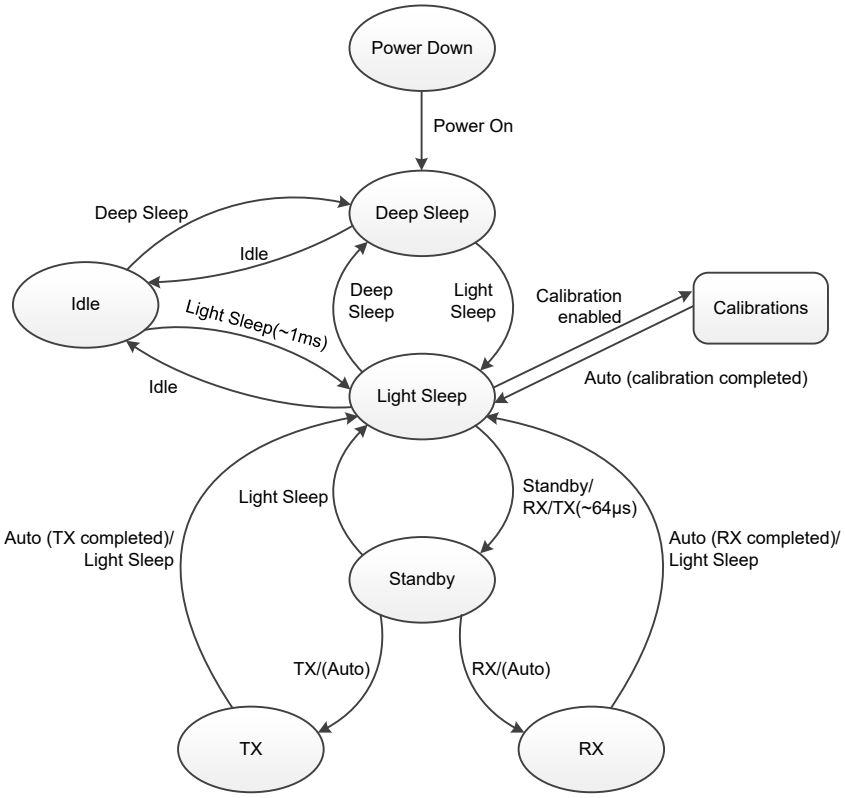


Figure 10. FIFO Mode State Diagram

Initially, the RF module is in the Power Down mode. After the device completes the internal power on reset, it will enter the Deep Sleep mode and wait for further strobe commands from the MCU. If the Light Sleep command is received, the device will enable the internal LDO, oscillate the XO and enter the Light Sleep mode. In this state, the MCU can have the RF module execute calibration process if necessary. For normal TRX operations, the MCU can issue an RX or TX command to the RF module. After receiving the TX or RX command, the device will first enter the Standby mode which lasts a certain period known as TX/RX settling time. After the settling time has escaped, the device will finally enter the RX or TX mode. The device will stay in the TX/RX sate until the TX/RX event is completed, after which the device will return to the Light Sleep mode automatically.

For low power periodical wireless transmission, the device supports low power Idle mode where the LIRC and wake-up timer are turned on. By appropriate timer setting and issuing the Idle mode command, the device will turn off the LDO and XO and enter the Idle mode. The wake-up timer starts to count after ATR_EN is set to "1". The device stays in the Idle mode until the timer expires and then an IRQ will be asserted on the GIO to wake up the MCU. Then the MCU can have the device enter the Light Sleep mode and continue to execute normal TX/RX operations. After the TX/RX event is completed, the MCU can issue the Idle command to have the device return to the Idle mode again.

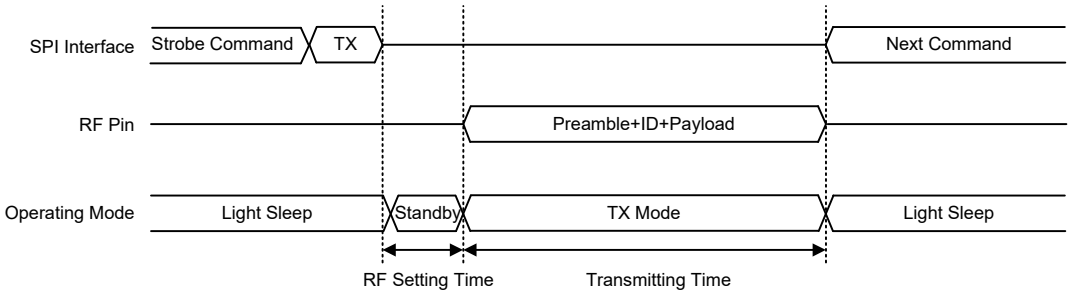


Figure 11. TX Timing in FIFO Mode

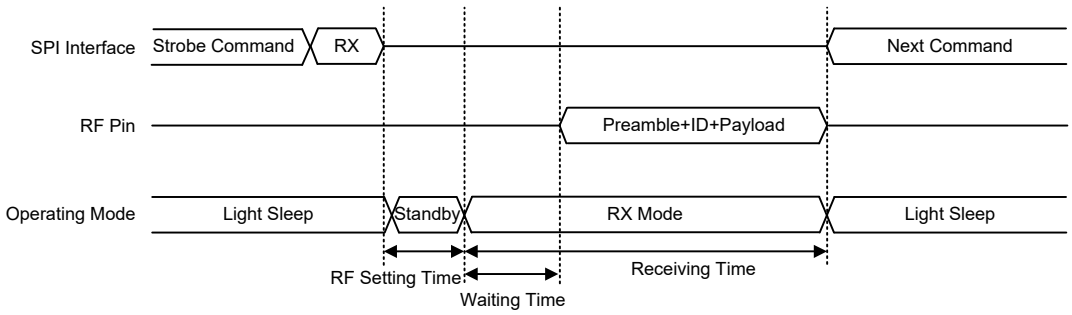


Figure 12. RX Timing in FIFO Mode

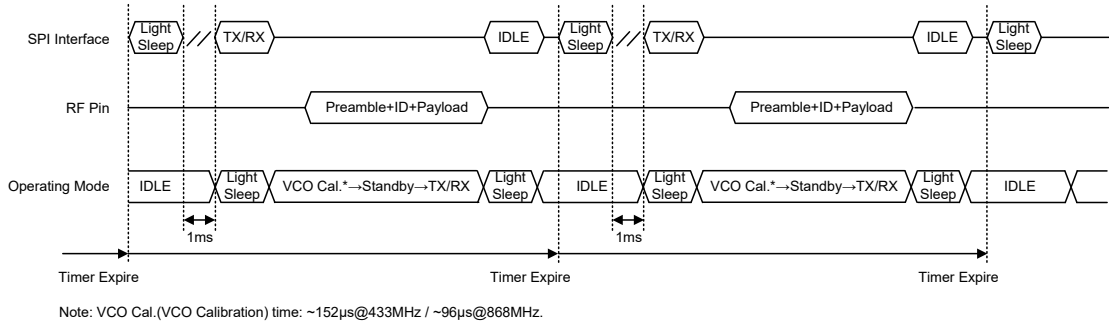


Figure 13. Periodical TX/RX Timing

TX/RX Direct Mode (DIR_EN = 1) State Machine

If the DIR_EN bit is set to 1, TX data is derived directly from the MCU to RF module and RX data is sent directly from the RF module to the MCU. In order to simplify the data bit clock synchronization between the RF module and the MCU, the RF module outputs the TBCLK/RCLK from GIO3 by setting GIO3S[3:0]. Both TBCLK and RBCLK are in 50/50 duty cycle. In the transmitting mode, the MCU outputs bit data at the rising edge of the TBCLK signal and the RF module samples the TX bit data at the falling edge of the TBCLK signal. In the receiving mode, the MCU receives data at the rising edge of the RBCLK signal and the RF module outputs bit data at the falling edge of the RBCLK signal. The MCU can select GIO1 or GIO2 for the TX/RX bit data transmission by setting GIO1S[2:0] or GIO2S[2:0].

For TX operations in the direct mode, the MCU needs to set the OM[1:0] bits, i.e. RTX_SEL and SX_EN, to 11b to select the TX mode and have the RF module enter standby mode first, then set the OM[2] bit, RTX_EN, to 1 to have the RF module start to transmit the TX data. As long as the MCU sets OM[2:0] to 000b, the RF module will return to the Light Sleep mode.

For RX operations in the direct mode, the MCU needs to set OM[1:0] to 01b first, then set OM[2] to 1 to have the RF module start to receive data from the air. After the RF module receives the matched SYNCWORD code, it will output the RBCLK clock, receive data bit (payload part) and then transmit to the MCU.

In direct mode, the transmission data length has no limit.

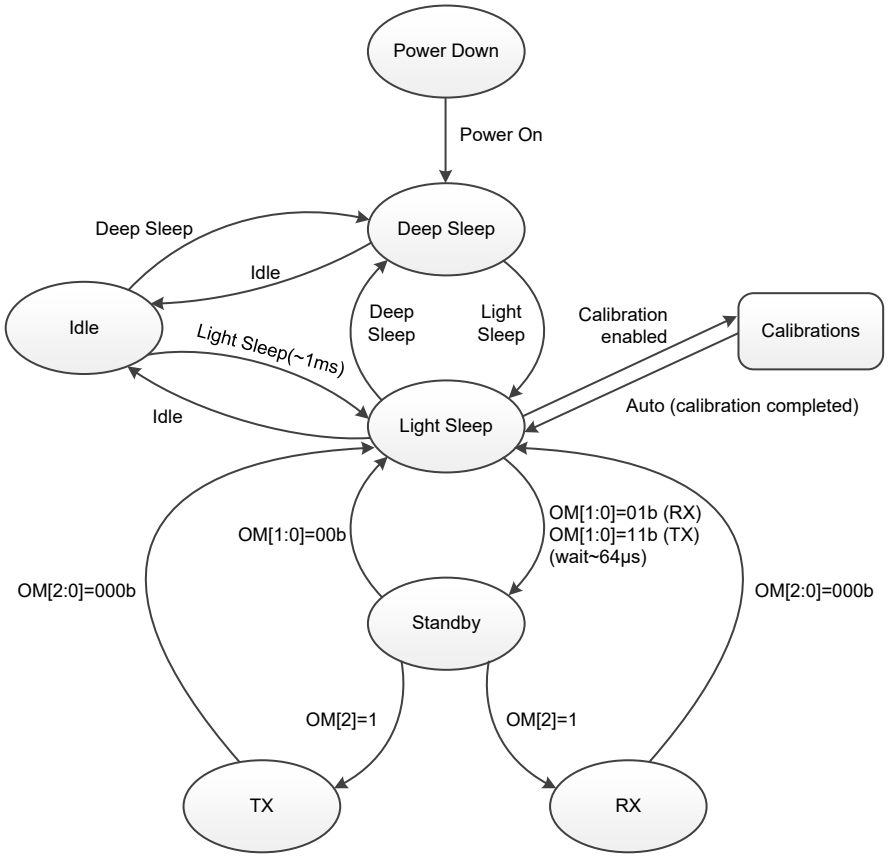


Figure 14. Direct Mode State Diagram

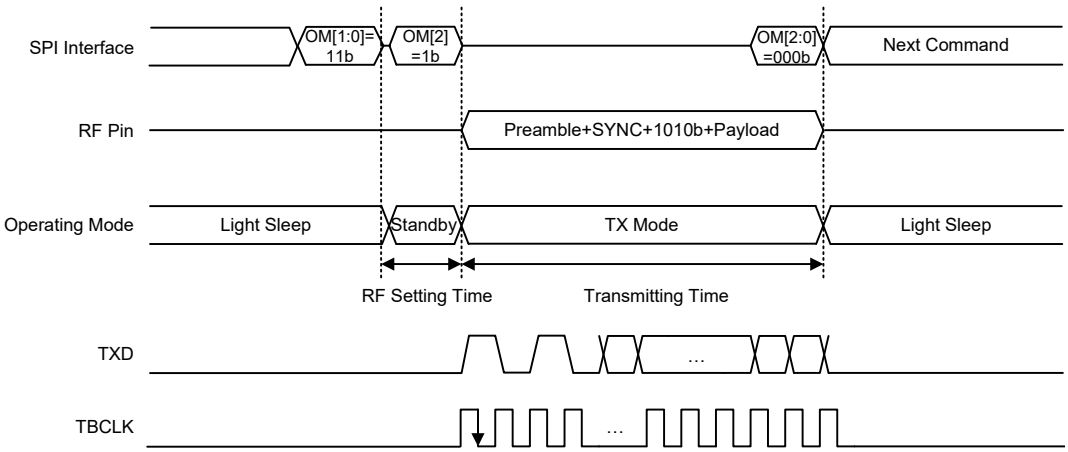


Figure 15. TX Timing in Direct Mode

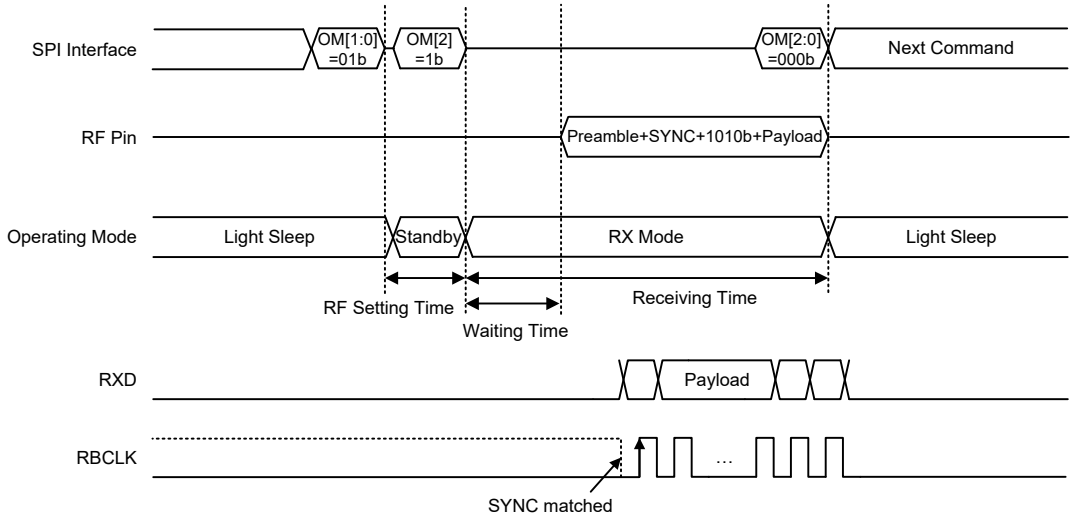


Figure 16. RX Timing in Direct Mode

Calibration

The device has three calibration functions, VCO, RC and LIRC calibrations, allowing users to auto select proper setting to compensate the PVT (Process-Voltage-Temperature) variation effect. The control bit, ACAL_EN, is used to enable the VCO and RC calibration functions at the same time and both calibration functions will be automatically implemented after this bit is set high. When the calibrations are completed, the ACAL_EN bit is cleared to zero by hardware. The MCU can poll the ACAL_EN bit status or use the calibration complete interrupt flag CALCMPF to check the calibration status. The device also has an independent enable bit, LIRCCAL_EN, for the LIRC calibration function, allowing to independently implementing the LIRC calibration function.

LIRC Calibration

There is an internal low frequency RC oscillator in the RF module providing a clock source for the wake-up timer in the Idle mode. In order to compensate the PVT (Process-Voltage-Temperature) variation error (up to ±10 %) impact on the accuracy of LIRC, the MCU can trigger the LIRC calibration to improve the wake-up timer accuracy error to be less than ±1 %.

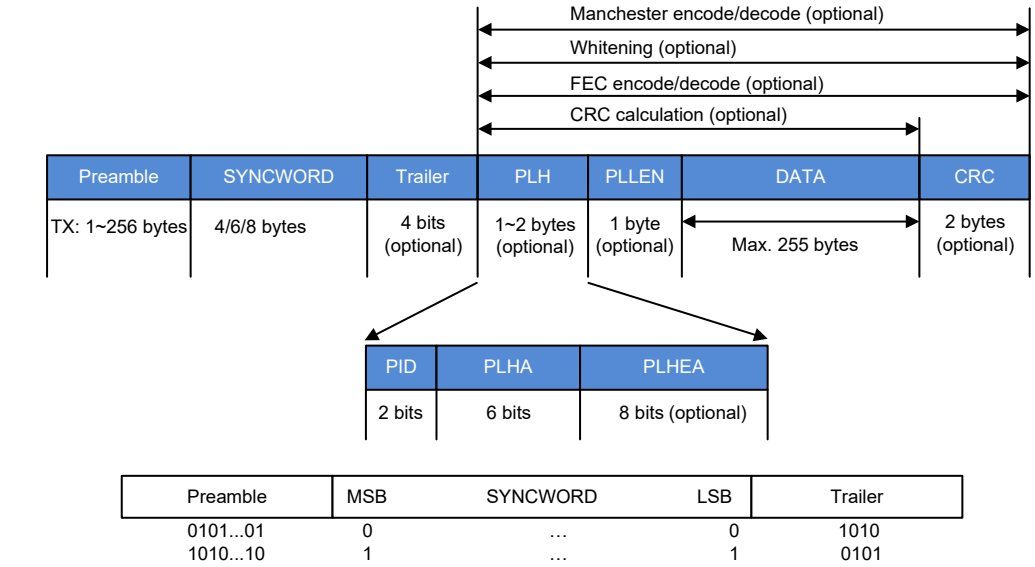
The MCU need to configure LIRC_OW = 0 and LIRC_EN = 1 before the LIRC calibration. Then the RF module will do LIRC calibration when LIRCCAL_EN is set to 1 by the MCU during the Light Sleep mode. The LIRCCAL_EN bit is reset to 0 by hardware on the completion of LIRC calibration. The LIRC calibration process would take about 4 ms.

Packet Handler

In the TX mode, the packet handler is used to move the transmitting data out of FIFO and implement channel coding according to the packet format, then sends the packet to the modulator. In the RX mode, the packet handler is used to implement channel decoding with data from the demodulator and store the payload data into FIFO.

The packet handler performs several tasks such as Preamble and SYNCWORD insertion, Forward Error Correction, CRC calculation/checking, whitening/de-whiteing and Manchester encode/decode.

Packet Format



Note: 1. Preamble format will follow SYNCWORD MSB to inverse.
If MSB = 0, Preamble format = 0101…01
If MSB = 1, Preamble format = 1010…10
2. Trailer format will follow SYNCWORD LSB to inverse.
If LSB = 0, Trailer format = 1010
If LSB = 1, Trailer format = 0101
3. The Trailer field contains 4 bits and is an optional field which is enabled by TRAILER_EN.

Figure 17. RF Transceiver Packet Format

Preamble

The packet starts with a preamble with a length of 1 ~ 256 words set by TXPMLEN[7:0] in the TX mode. The word length is determined by the preamble mode. There are two preamble modes switched by PMLP_EN.

PMLP_EN = 0 – auto preamble pattern mode (compatible with BC360x/BC66F36x2)

The first bit of the preamble pattern is equal to the inverted SYNCWORD MSB and then continue with 1/0 toggle. In this mode, word unit = 1 byte.

PMLP_EN = 1 – preamble pattern by register mode

The preamble pattern is defined by PMLPAT[15:0] and the length is defined by PMLPLEN.

PMLPLEN = 0, preamble pattern = PMLPAT[7:0]; word length = 1 byte

PMLPLEN = 1, preamble pattern = PMLPAT[15:0]; word length = 2 bytes

SYNCWORD

The SYNCWORD length, which is set by ({SYNCLEN[1:0], SYNCLENLB} + 1), can be 4/6/8 bytes in both TX and RX modes. When the RX side receives a matched SYNCWORD packet, the DATA field will be stored in the FIFO. Syncword Low Byte cannot be 0x55 or 0xAA.

Trailer

The trailer field length is fixed at 4 bits which is optional and enabled by the TRAILER_EN bit.

PLH (Payload Header)

The PLH is optional and enabled by PLH_EN. The payload header length can be 1 or 2 bytes set by PLHLEN. When the PLHLEN bit is 0, only {PID[1:0], PLHA[5:0]} field appears in the packet. PID[1:0] is located in bit[7:6] of the payload header field. When the PLHLEN bit is set to 1, the payload header address is extended to 2 bytes which is formed by PLHA[5:0] and PLHEA[7:0].

PLHA[5:0] and PLHEA[7:0](when PLHLEN = 1) have two functions controlled by the PLHAC_EN bit. If PLHAC_EN = 0, PLHA[5:0] and PLHEA[7:0] can be used as software flags and the actual function can be defined by users. If PLHAC_EN = 1, the device will compare the local {PLHA[5:0], PLHEA[7:0]} field with the received {PLHA[5:0], PLHEA[7:0]} field. If matched, the receiving data will be moved into the RX FIFO, otherwise the following incoming data will be abandoned. PLHA[5:0] = 0 and PLHEA[7:0] = 0(checked when PLHLEN = 1) is a special address that the hardware will not check whether the address is matched or not. It is used to support broadcast function for devices with same SYNCWORD but different payload header address values.

PLLEN (Payload Length)

The PLLEN field is optional and its length is fixed at 1 byte once being enabled by PLLEN_EN. When this bit is set high, the DATA field length is variable and is determined by the PLLEN field. In TX mode, the transmitter sends the TXDLEN defined bytes of data from TX FIFO and the TXDLEN is automatically latched into the PLLEN field. In RX mode, the receiver gets the PLLEN and receives the PLLEN defined bytes data into RX FIFO.

DATA

When in the TX mode, the TX data length is determined by the TXDLEN[7:0] field. The maximum length is 255 bytes in the extend FIFO mode. In the special case of infinite FIFO mode, the length can exceed 255 with an infinite length. If PLLEN_EN = 1, the PLLEN field in the TX packet is enabled and the PLLEN content is equal to TXDLEN[7:0]. When in the RX mode, the RX data length is set by RXDLEN[7:0] if PLLEN_EN = 0 and by PLLEN field in the receiving packet if PLLEN_EN = 1.

CRC

The CRC field is optional and is enabled by CRC_EN. It is recommend to always set CRC_EN to 1 for data correctness checking. There are two CRC formulas selected by setting the CRCFMT bit.

CRCFMT = 0: CCITT-16-CRC $G(X) = X^{16} + X^{12} + X^5 + 1$

CRCFMT = 1: IBC-16-CRC $G(X) = X^{16} + X^{15} + X^2 + 1$

FEC

The optional data encode/decode function can be enabled by FEC_EN. Use (7,4) Hamming code to correct 1-bit error and more than 1-bit error detect for each 4-bit data. After FEC, the data length for each data will be $(4 + 3) \times 2 = 14$ bits.

- **Hamming Code Function Table**

Bit	7	6	5	4	3	2	1
Transmitted Bit	D3	D2	D1	P2	D0	P1	P0
P0	Y	N	Y	N	Y	N	Y
P1	Y	Y	N	N	Y	Y	N
P2	Y	Y	Y	Y	N	N	N

Data Whitening

The optional data whitening/de-whitening function can be enabled by WHT_EN. Use PN7/PN9 code to implement XOR operation with the transmitted data. The whitening seed is set by WHTSD[8:0].

Manchester Code

The optional Manchester encode/decode function can be enabled by MCH_EN. Each bit after Manchester encoding will be extended into two bits and recovered to one bit data after decoding.

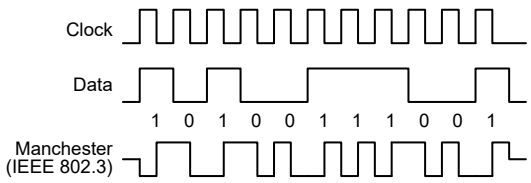


Figure 18. Manchester Code Example

FIFO Operation Modes

In Burst mode, data transmission to the RF transmitter is derived from FIFO and is pre-written by the MCU. There are 4 FIFO modes to support various applications. They are the Simple FIFO mode, Block FIFO mode, Extend FIFO mode and Infinite FIFO mode.

FIFO Reset

To use the FIFO in the burst mode, issue the TX FIFO address pointer reset command and RX FIFO address pointer reset command to reset the FIFO pointer and buffer first. After this, the FIFO is in the initial state same as reset.

Simple FIFO Mode

This FIFO mode is used for general applications with a TX/RX data length less then or equal to 64 bytes. The data length should not exceed 64 bytes. To use the simple FIFO mode, the MCU must write the transmitting data to FIFO by the SPI write FIFOcommand. The transmitting sequence is first written byte first out and the MSB in each byte first out to the transmitter. Users should determine all transmitting data packet format including the preamble, SYNCWORDand packet encoding such as FEC, CRC, whiting. After FIFO data filling out is completed, clear the TXFFSA[5:0] field and set TXDLEN[7:0]/RXDLEN[7:0] field to the desired transmitting/receiving length in bytes. Then issue the TX command to start the transmission. After the current transmitting is completed, the data will be kept in FIFO to wait for the next transmission.

Programming procedure:

1. Reset TX FIFO by the SPI reset TX FIFO command.
2. Reset RX FIFO by the SPI reset RX FIFO command.
3. TXFFSA[5:0] must be cleared to 0.
4. Fill out TX FIFO by the SPI write FIFO command.
5. Set TXDLEN[7:0]/RXDLEN[7:0] to control the TX/RX length in bytes.
6. Issue the TX command for transmitter and RX command for receiver.
7. TX/RX completion is acknowledged by the TX/RX complete IRQ.
8. Re-transmitting TX packet with the same data will auto-reset TXFF_RPTR to 0.

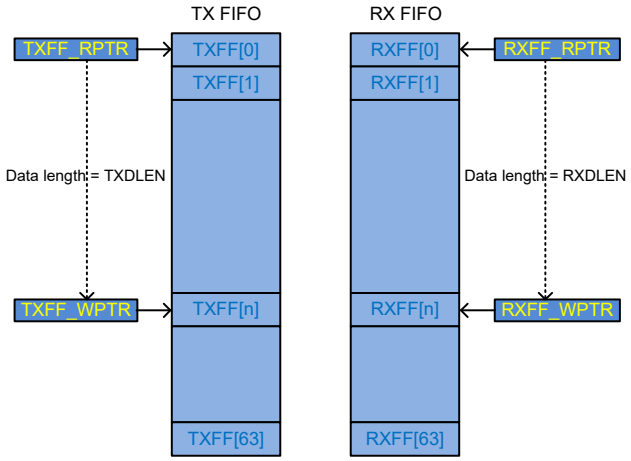


Figure 19. Simple FIFO Mode Programming Procedure

Block FIFO Mode

The Bock FIFO mode is used to support multi-key code applications. Users should write all the key codes to FIFO first. When a key is pressed, the MCU will detect the key and set TXFFSA[5:0] to the target key code start address and set TXDLEN[7:0] to indicate the key code length and issue the TX strobe command to start the transmission. The maximum FIFO length is also limited to 64 bytes.

Programming procedure:

1. Write key code 0 ~ n to TX FIFO by SPI write FIFO command.
2. When a key is pressed, the MCU will set TXFFSA[5:0] to the start address of the corresponding key code.
3. Set TXDLEN[7:0] for key code length.
4. Set the RXDLEN[7:0] to key code length and then enter the RX mode by SPI command.
5. Issue TX command for transmitter and RX command for receiver.
6. TX/RX completion is acknowledged by the TX/RX complete IRQ.

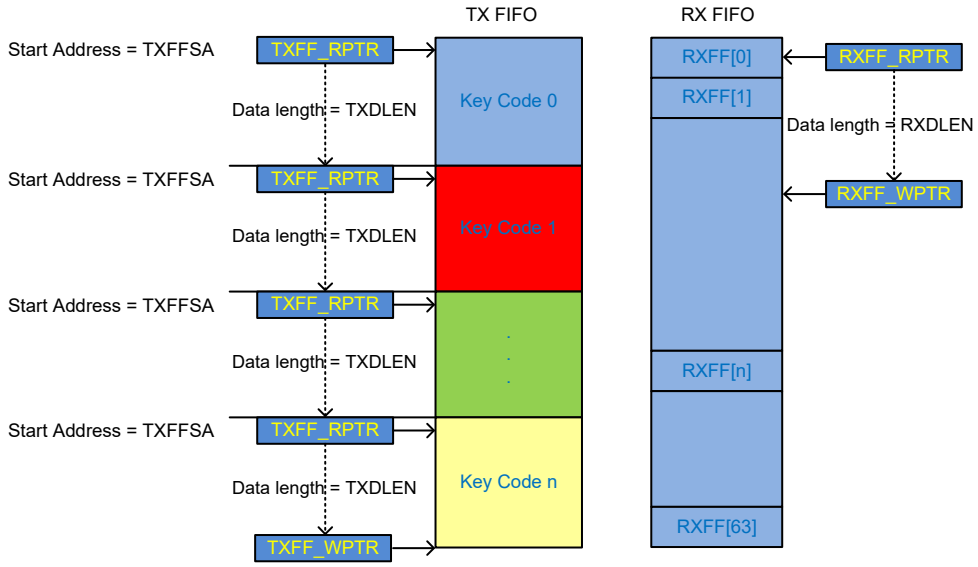


Figure 20. Block FIFO Mode Programming Procedure

Extend FIFO Mode

The Extend FIFO mode is used for transmissions with a long payload data packet. The maximum length is 255 bytes. As the physical FIFO length is 64 bytes, to extend the available transmitting length in one packet, a handshake mechanism is needed between the MCU and the FIFO controller.

Set FFMG[1:0] to determine the FIFO data length margin and set FFMG_EN to enable the margin detect function to inform the MCU when the TX FIFO data fullness level is less than the margin. The MCU should write data to TX FIFO fast enough when receiving this reminding signal to avoid transmission being terminated by TX FIFO data length low to zero.

Programming procedure:

1. Set FFMG_EN to enable FIFO length margin detection function (i.e. FIFO low threshold detect function) and set FFMG[1:0] to select the threshold, 4, 8, 16 or 32 bytes.
2. Set the FIFOLTIE bit to 1 to enable the FIFO low threshold IRQ.
3. Set GIOnS field (n = 1 ~ 3) = 101b to output IRQ on GIO1 ~ 3.
4. TX: If MCU detects the FIFO low threshold IRQ signal, it will move data into TX FIFO with a data length less than or equal to (64-threshold). Then the MCU clears the FIFO low threshold IRQ flag FIFOLTIF and repeats the same routine until all TX data are completely written to TX FIFO.
5. RX: If MCU detects the FIFO low threshold IRQ signal, it will read data from RX FIFO. Then the MCU clears the FIFO low threshold IRQ flag FIFOLTIF and repeats the same routine until receiving the RX completion IRQ to read the remaining data from RX FIFO.

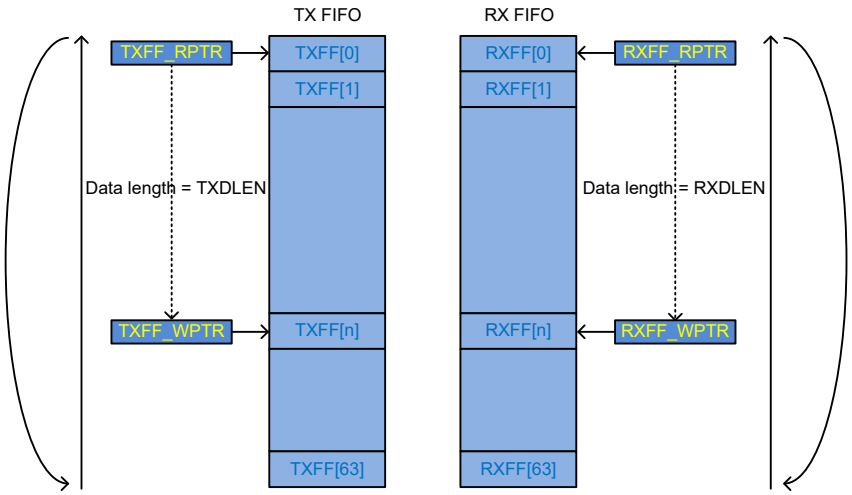


Figure 21. Extend FIFO Mode Programming Procedure

Infinite FIFO Mode

Programming procedure:

1. Set FFINF_EN to 1 to enable the Infinite FIFO mode.
2. The handshaking and IRQ function are identical with the Extend FIFO mode.
3. TX: If receiving the FIFO low threshold IRQ, the MCU continues to write TX data to TX FIFO with a data length less than or equal to (64-threshold). Then the MCU clears the FIFO low threshold IRQ flag and repeats the same routine until it wants to terminate the infinite FIFO mode. To terminate the infinite FIFO mode, after receiving IRQ and moving data to TX FIFO, the MCU should clear FFINF_EN to zero and set TXDLEN[7:0] to the remaining data length if the remaining transmitting length is less than 192 bytes and longer than 64 bytes. The packet will be terminated when all of the target data are transmitted completely.
4. RX: If receiving the FIFO low threshold IRQ, the MCU reads data from RX FIFO. Then the MCU clears the FIFO low threshold IRQ flag and repeats the same routine until it wants to terminate the infinite FIFO mode. To terminate the infinite FIFO mode, after receiving IRQ and reading data from RX FIFO, the MCU should clear FFINF_EN to zero and set RXDLEN[7:0] to the remaining data length if the remaining receiving length is less than 192 bytes and longer than 64 bytes. The packet will be terminated when all of the target data are received completely.

Receiving Packet Judgement

In normal RX operating mode, package reception follows the following judgement criteria.

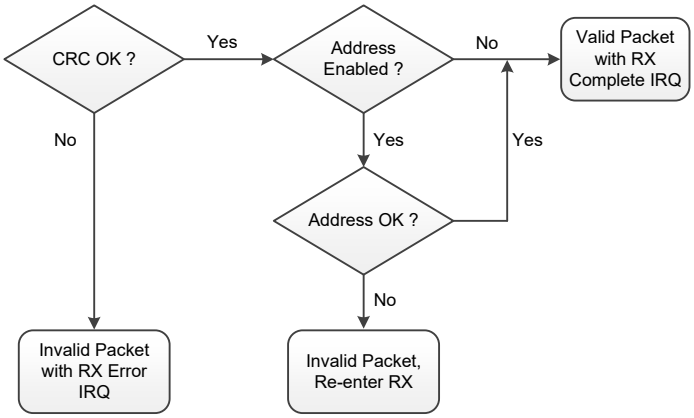


Figure 22. RX Mode Packet Judgement

The RF module adopts extra receiver packet judgment for the continuous RX mode and auto-acknowledge mode. The main purpose of these special link layer functions are used to alleviate MCU loading when handling TRX packet transaction.

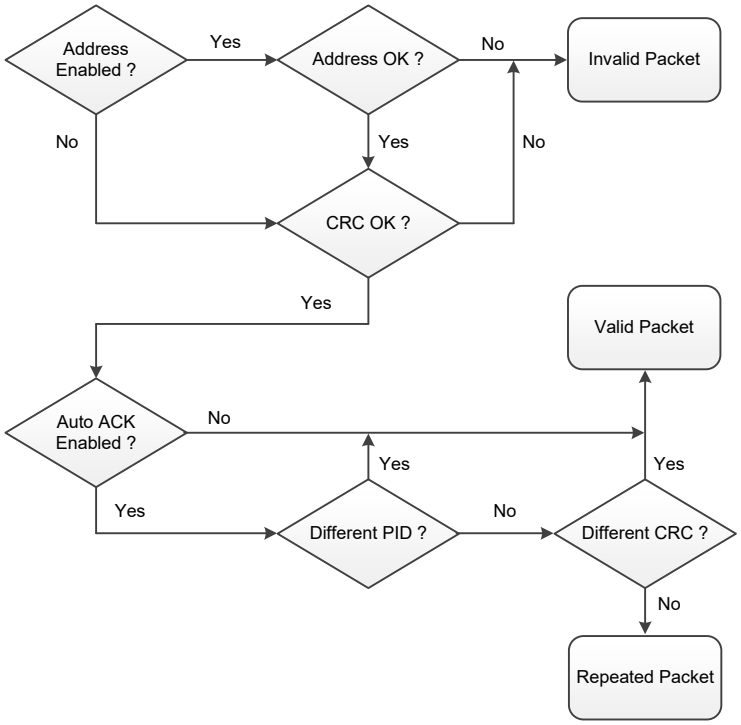


Figure 23. ARK Mode Packet Judgement

Continuous RX Mode

There is a special continuous RX operating mode supported in the RF module. The MCU can enable this continuous RX mode by setting the RXCON_EN bit high and start the continuous RX mode by issuing the RX strobe command to the device. If there is a valid RX packet received, the RF module will issue an RX completion IRQ to the MCU. The device then repeats the RX operation after a duration defined by DLY_TXS[2:0] to keep listening for incoming packets. If an invalid packet is received, the RF module would only repeat the RX operation without issuing the RX completion IRQ to the MCU. The MCU stops the continuous RX by issuing the Light Sleep strobe command to the RF module. In the continuous RX mode, only simple FIFO mode can be used. In order to prevent the receiving packet data length field from being corrupted by new incoming packets before the MCU reads data from RX FIFO, users should set RXPL2F_EN = 1 and PLLEN_EN = 1 to have the PLLEN information stored into the RX FIFO. Because of the existence of PLLEN byte, the maximum packet data length becomes 63 bytes. If a new incoming packet arrives before the MCU reads RX FIFO, a FIFO overflow error will happen, in which condition the RF module will issue an RX error IRQ to the MCU with FIFO overflow error flag RXERRIF set. At this moment, the MCU should exit the continuous RX mode and reset the RX FIFO pointer.

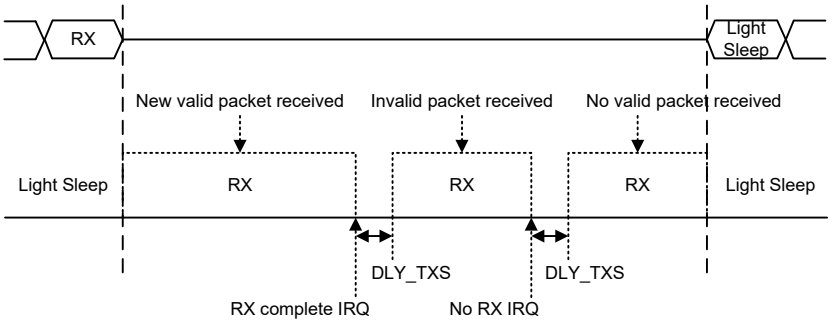


Figure 24. Continuous RX Mode

ARK Mode: Auto-Resend and Auto-Ack

The RF module supports auto-resend and auto-ack mechanism by setting the ARK_EN bit high. This mechanism enables an easy two-way communication implementation however can only be operated in the simple FIFO mode.

Set ARK_EN to 1 to enable the device to enter the auto-resend and auto-ack ready mode. Then, auto-resend is triggered by the TX strobe command from the MCU and auto-ack is triggered by RX strobe command from the MCU. Packet format transmitted from the master to the slave in the auto-resend mode are illustrated below.

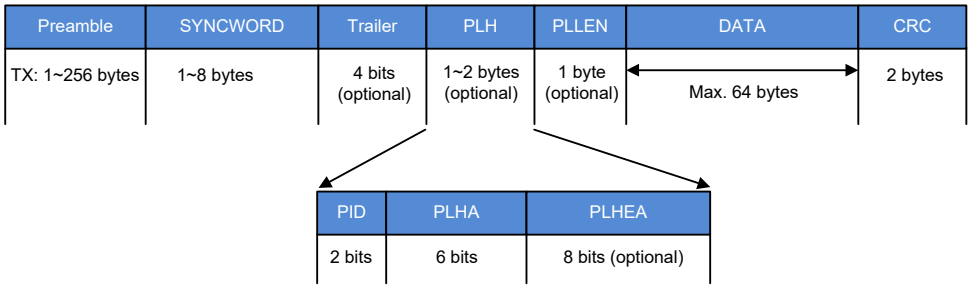


Figure 25. ARK: Packet Format

The slave side in the auto-ack mode uses the packet format as the following to be an acknowledge packet transmitted to master. Note that there is no payload data field used in the acknowledge packet.

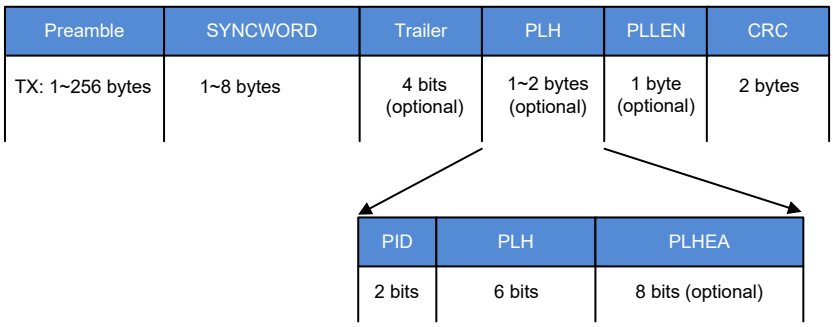


Figure 26. Auto-Resend: Packet Format

If the address field is used for the ARK mode, the auto-resend (master) side should configure the same address as the auto-ack (slave) side.

After configuring ARKNM[3:0], ARK_EN and ARKRXAP[7:0], the MCU starts the auo-resend process by issuing the TX strobe command. The RF module starts to transmit data from the TX FIFO and then enters the RX mode after the TX completion. The RX period is in multiples of 250 μs (default) which is determined by (ARKRXAP[7:0] + 1). If the RF module receives a valid acknowledge packet from the slave side within the RX period with CRC checked correct, it will return to the Light Sleep mode and issue a TX completion IRQ to the MCU. Otherwise, the RF module will check if the resend number has reached the limit set by (ARKNM[3:0] + 1), if not, it will go to the TX mode to transmit the same TX data from the TX FIFO and the resend number will be increased by one.

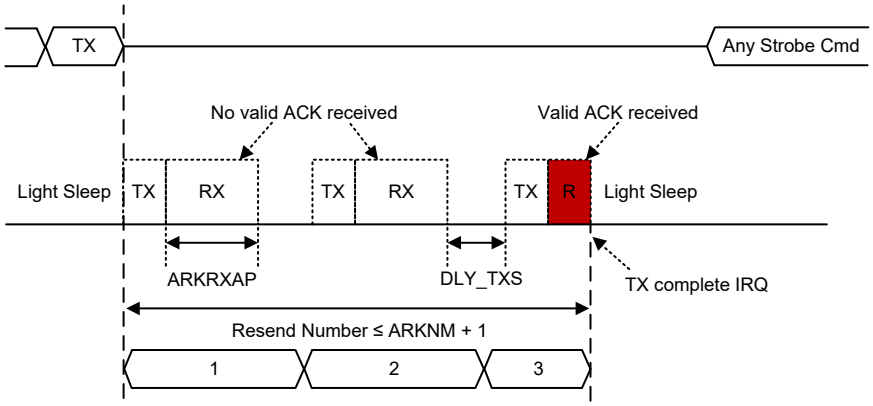


Figure 27. Auto-resend: ACK Packet Received before ARKNM Limit

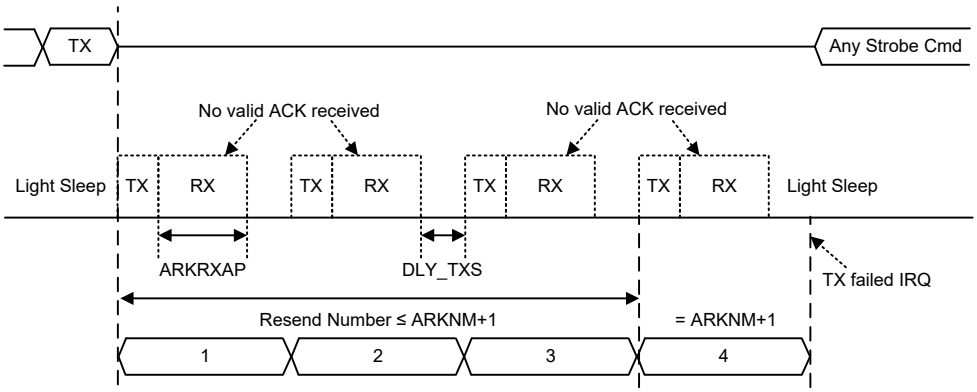


Figure 28. Auto-resend: No Valid Packet Received before ARKNM Limit

Regarding the auto-ack in the slave side, the MCU issues the RX strobe command to start the auto-ack process and issues the Light Sleep strobe command to stop the auto-ack process. In the auto-ack mode, an extra PID/CRC filtering function will be applied for the slave side to check the packet received. If the PID/CRC of the new incoming packet is same as the stored PID/CRC of the last packet, then the newly received packet would be treated as a repeated packet.

During the auto-ack process, if the device receives a valid packet with different PID/CRC and CRC/address checked correct, it will issue an RX completion IRQ to the MCU and auto-transmit the ACK packet to the master. If the device receives a packet with the same PID/CRC and CRC/address checked correct, it will treat this packet as the repeated packet. Then the device will not issue the RX IRQ to the MCU but still auto-transmit the ACK packet to the master. If the device receives a packet with CRC/address checked failed, no IRQ is issued and the device will automatically re-do the RX operation to continually listening for incoming packets.

The gap period for the device to restart the next RX operation after the current RX completion is defined by ARKRXAP[7:0]. In general cases, the MCU should fetch the receiver FIFO data within this period after receiving the RX completion IRQ. Besides, the MCU needs to wait for a same duration if it wants to leave the ARK mode after receiving the RX completion IRQ.

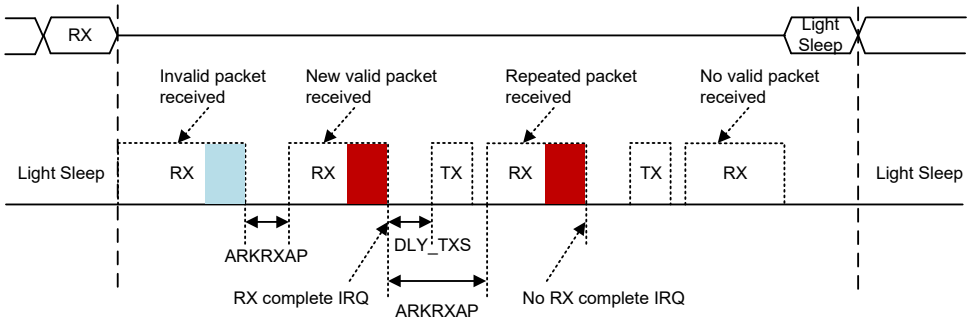


Figure 29. Auto-ACK Process

ATR Mode: Auto-Transmit-Receive

There is a special ATR operation mode in the RF module to reduce the external host's loading. Two ATR functions are implemented within the device, one is WOR (Wake-On-RX) and the other is WOT (Wake-On-TX). They can only be operated with simple FIFO mode. These two operating modes need to co-work with an Idle mode timer which operates at a low frequency. The low frequency clock can be sourced from the internal LIRC or from the external ROSCi clock by setting the ATRCLKS bit in the ATR1 register. There are two operation modes for the ATRCT timer which is selected using the ATRCTM bit. Clearing the ATRCTM bit to 0 will select the single mode, where the ATRCT timer will restart upon every ATR transation when entering the Idle state. The ATRCT timer will stop and leave the ATR mode upon receiving the Light Sleep command. Setting the ATRCTM bit to 1 will select the continuous mode, where the ATRCT timer will start to operate upon receiving the Idle command and continuously run until the ATR_EN bit or the ATRCTM bit is cleared to zero.

After entering the ATR mode, only the Idle, Light Sleep, Set Register Bank and control register read/write commands can be recognized by the RF module.

WOT (Wake-On-TX) Function

When the WOT function is enabled by setting the ATR_EN bit to 1 and the ATRM[1:0] bits to 00b, the device will periodically wake up from the Idle mode and transmit TX FIFO contents without interaction with the MCU. The device starts the WOT process upon receiving the Idle strobe command from the MCU and stops the WOT process upon receiving the Light Sleep strobe command from the MCU. The ATRCYC[15:0] bits are used to set the wake-up period for the WOT function. At the moment of timer expiration, the wake-up timer will trigger the device to leave the Idle state and enter the active state to transmit data, at the same time the ATRCYC[15:0] content will be reloaded into the timer's counter. After finishing the TX operation, the device will return to the Idle mode and stay in this state until next wake-up timer expiration occurs. In the active state, the device only implements wake-up transmission once by default. Users can extend the wake-up transmitting mechanism by combining with the ARK function. The repeated transmitting number is controlled by (ARKNM[3:0] + 1). The time duration between the repeated transmitting packets is inserted with one RX slot and controlled by ARKRXAP[7:0] in the ATR8 register. If the device receives ACK in the RX slot, a TX completion IRQ will be issued to inform the MCU.

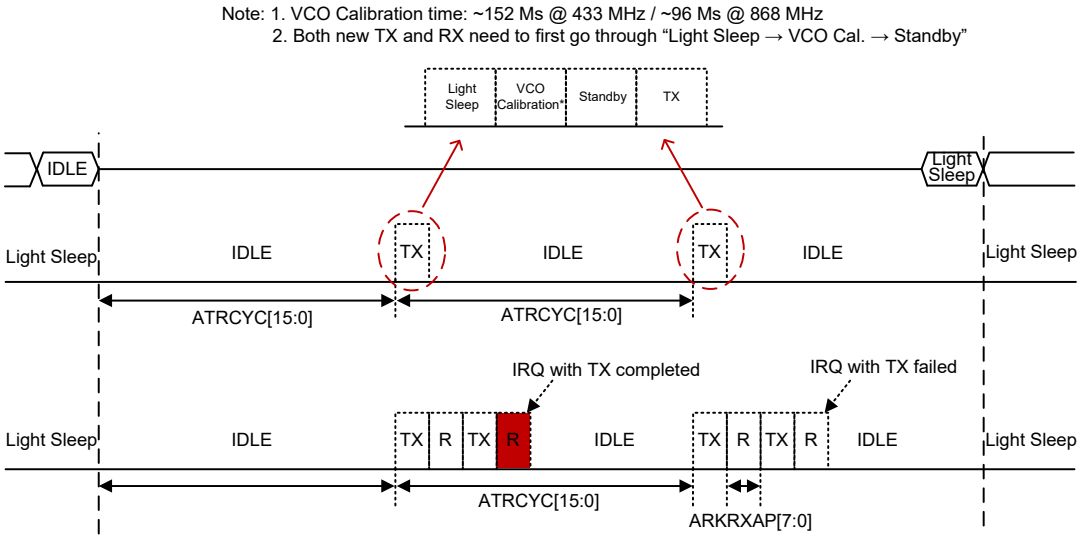


Figure 30. WOT Process

WOR (Wake-On-RX) Function

When the WOR function is enabled by setting the ATR_EN bit to 1 and the ATRM[1:0] bits to 01b, the device will periodically wake up from the Idle mode and listen for the incoming packets without interaction with the MCU. The device starts the WOR process upon receiving the Idle strobe command from the MCU and stops the WOR process upon receiving the Light Sleep strobe command from the MCU. The ATRCYC[15:0] bits are used to set the wake-up period for the WOR function. At the moment of ATR timer expiration, the wake-up timer will trigger the device to leave the Idle mode and enter the active state to listen for the incoming packet, at the same time the ATRCYC[15:0] content will be reloaded into the timer's counter. The receiving active period is defined by the ATRRXAP[10:0] bits. The active period is in multiples of 250 μs (defalut) and starts from 250 μs. If there is no incoming packet received in the RX active period, the device will return to the Idle mode and wait for the next WOR cycle.

The active period is auto-extended when the "preamble + SYNCWORD" is detected. The extend period is defined by (ATRRXEP[15:0] + 1). The extend period is also in multiples of 250 μs (defalut) and starts from 250 μs. Once the SYNCWORD is received, the receiving period would be auto-extended until the whole packet is completely received. After the RX receiving is done with CRC checked correct, the RF module would acknowledge the MCU with RX complete IRQ and stay at light sleep mode. MCU can read the incoming packet from the RX FIFO and then restart the next WOR session by issuing Idle strobe command. If MCU wants to leave WOR mode, MCU still needs to issue Light Sleep command to the RF module.

Note: 1. VCO Calibration time: ~152 Ms @ 433 MHz / ~96 Ms @ 868 MHz
2. Both new RX and TX need to first go through"Light Sleep → VCO Cal. → Standby"

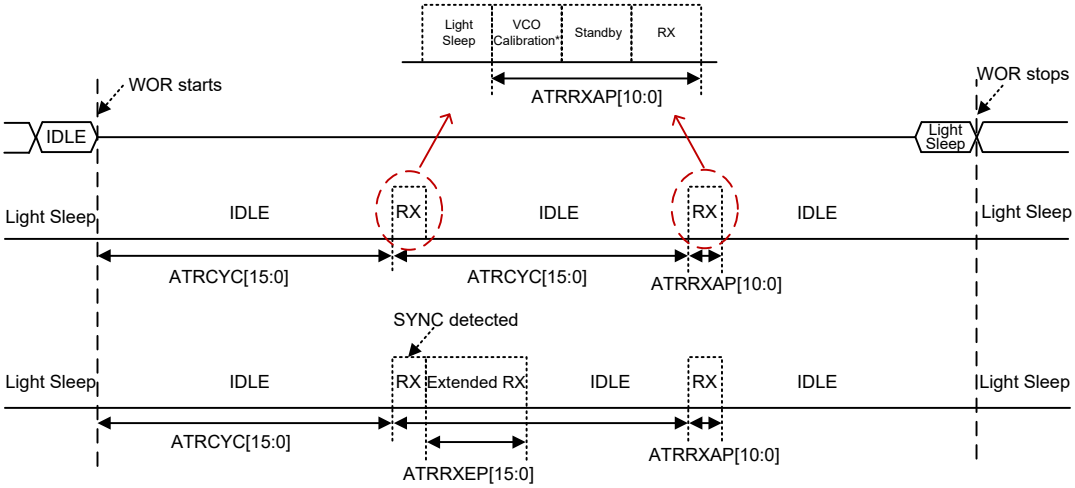


Figure 31. WOR Without Incoming Packet Received

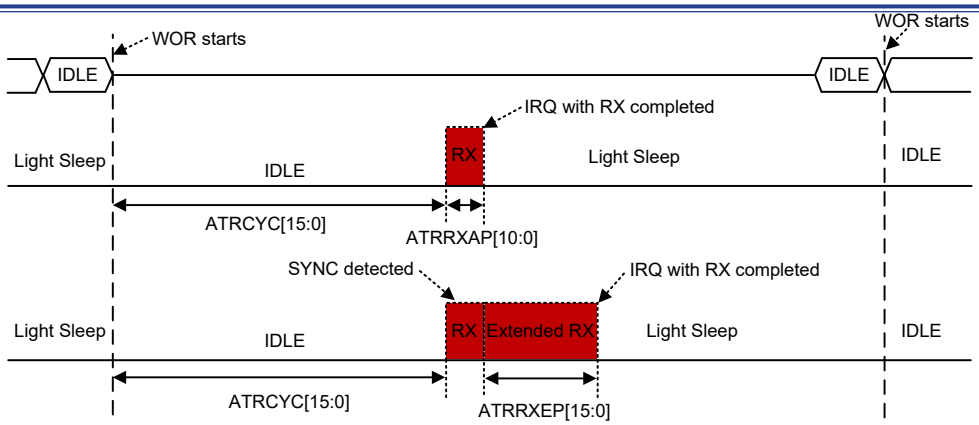


Figure 32. WOR With Incoming Packet Received

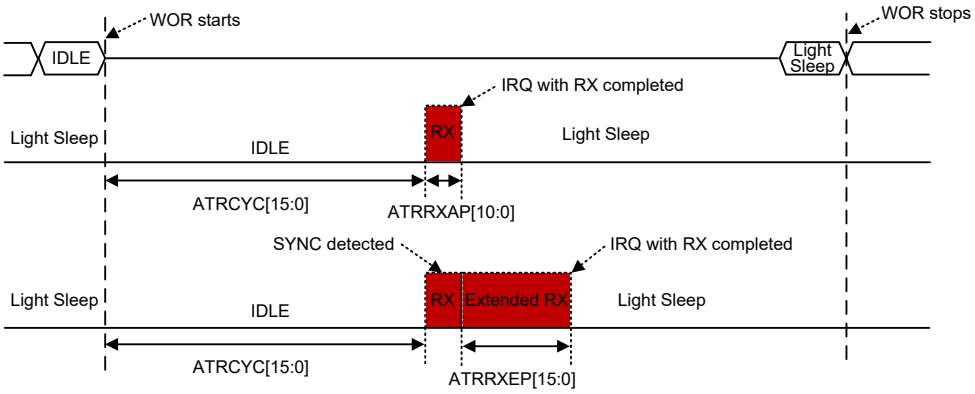


Figure 33. WOR Stops after Receiving Incoming Packet

In the WOR active period, the device only implements RX operation once by default. Users can extend the wake-up receiving mechanism by combining with the ARK function. In WOR + ARK mode, the time duration between the repeated receiving packets is inserted with one TX slot for acknowledgement. The TX duration depends on the transmitting data rate. The device stays in the RX mode for a maximum period of time defined by ATRRXAP + ATRRXEP. If a valid imcoming packet, with CRC checked correct and a different PID/CRC, is received before the timer expires, the device will issue an RX completion IRQ to the MCU and automatically enter the TX mode. If a repeated packet, with CRC checked correct and a same PID/CRC, is received, the device will only automatically enter the TX mode with no IRQ to the MCU. After the TX completion, the device will return to the RX mode again and listen for the incoming packets until the timer expires if no incoming packet is received.

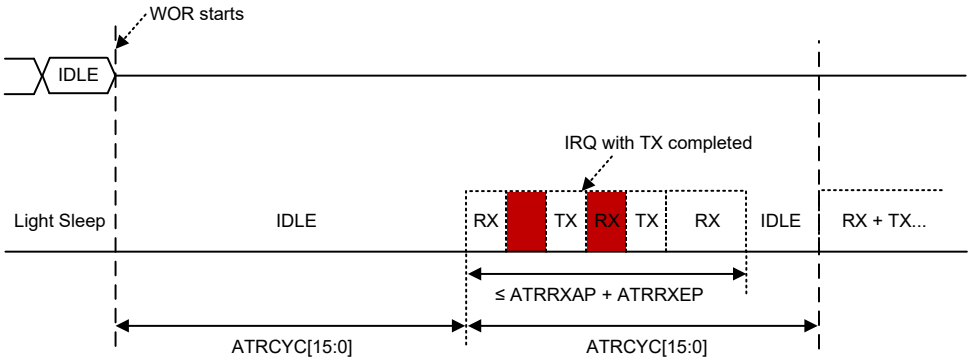


Figure 34. WOR + ARK Process

WTM (Wake-up Timer Mode)

The RF module can be set as a programmable timer to output a periodical waveform on GIOs. User can use this signal to wake up the CPU. Set ATR_EN = 1 and ATRM = 10b/11b to enable the WTM mode. The device starts the WTM mode upon receiving the Idle strobe command from the MCU and stops the WTM mode upon receiving the Light Sleep strobe command. The device will stay in the Idle mode for the whole WTM process.

Message Flowchart Examples

ATR: WOT & WOR

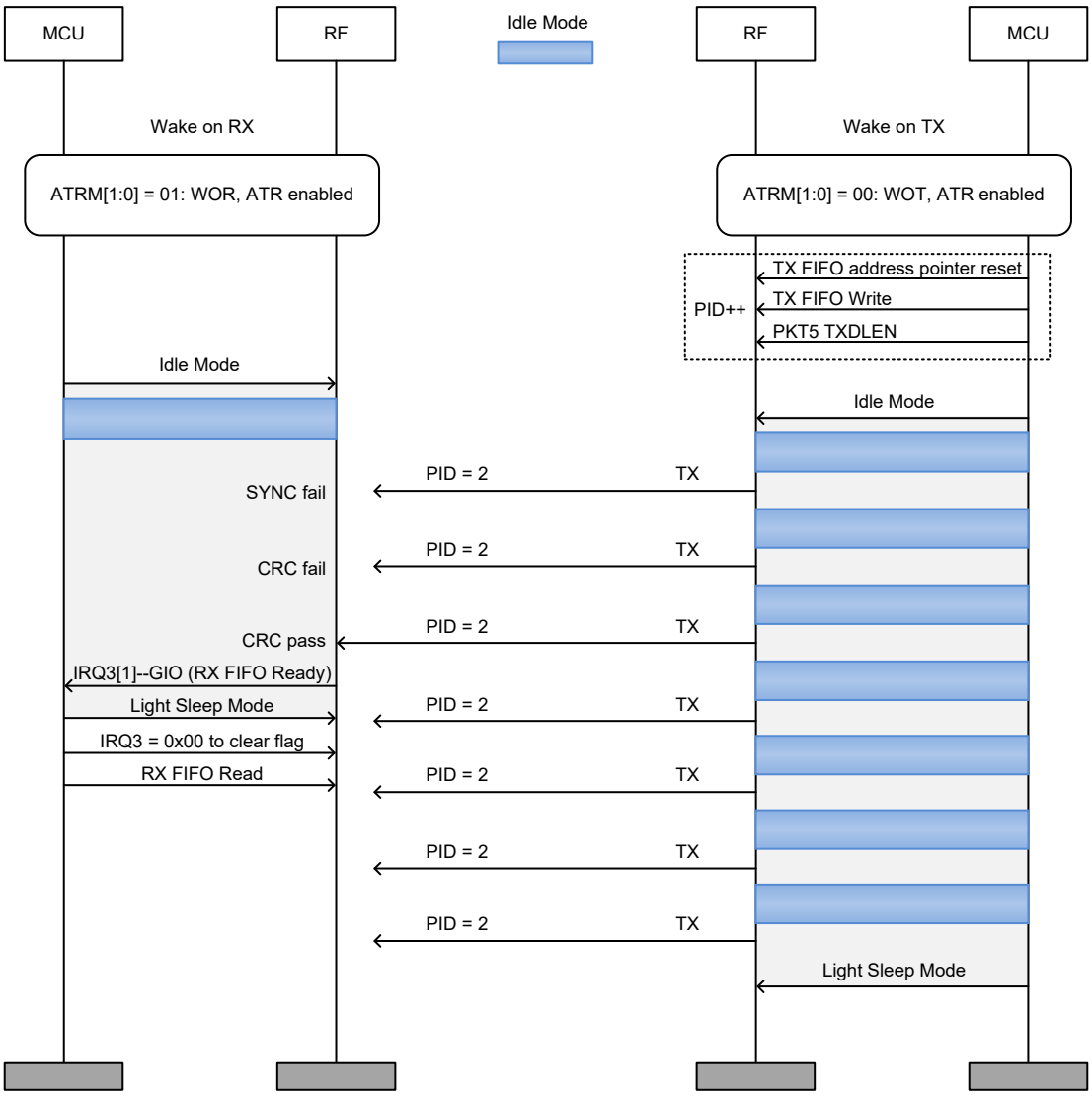


Figure 35. ATR Message Flowchart

ATR + ARK: WOT + Auto-Resend & WOR + Auto-Ack

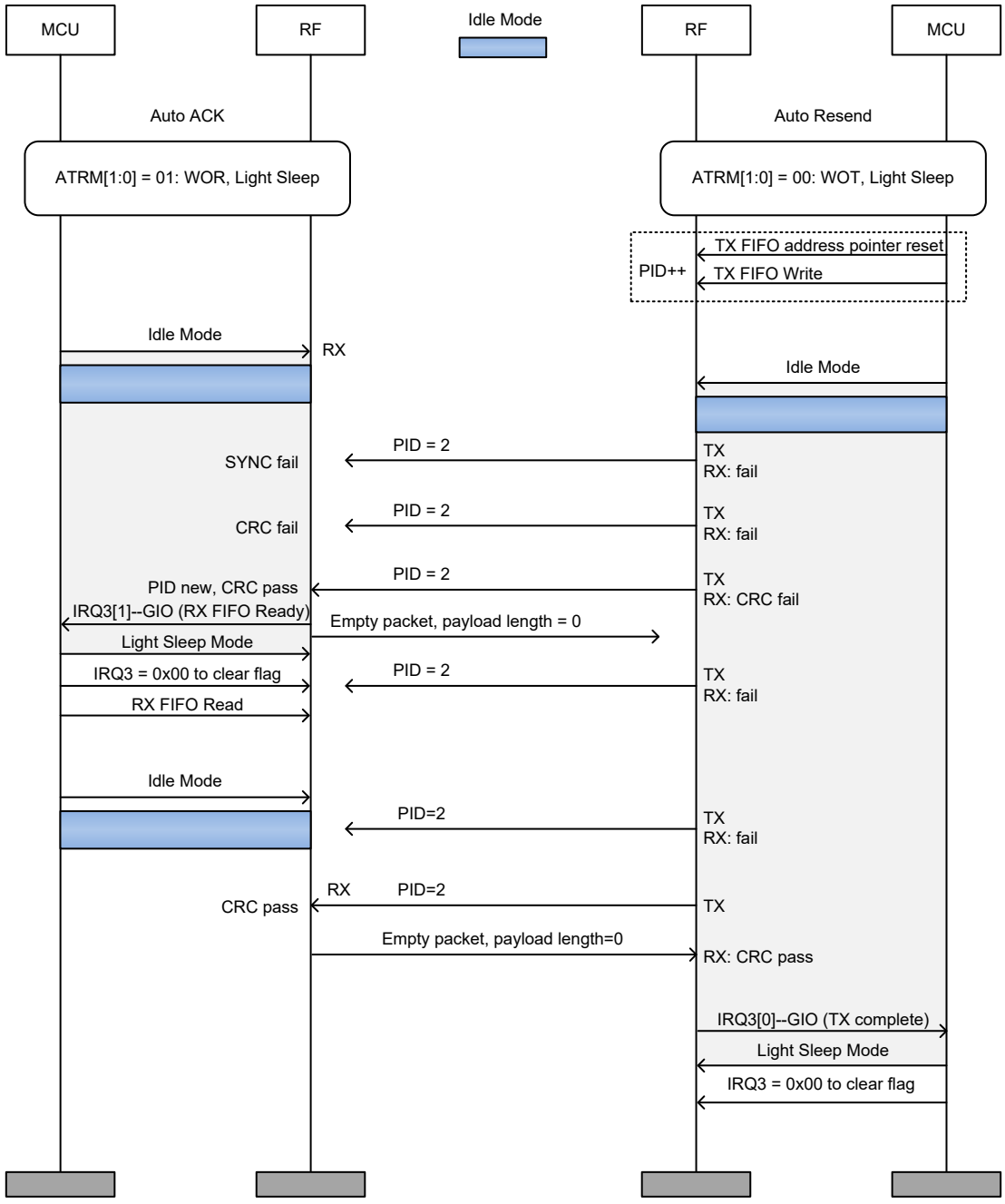


Figure 36. ATR + ARK Message Flowchart Example 1

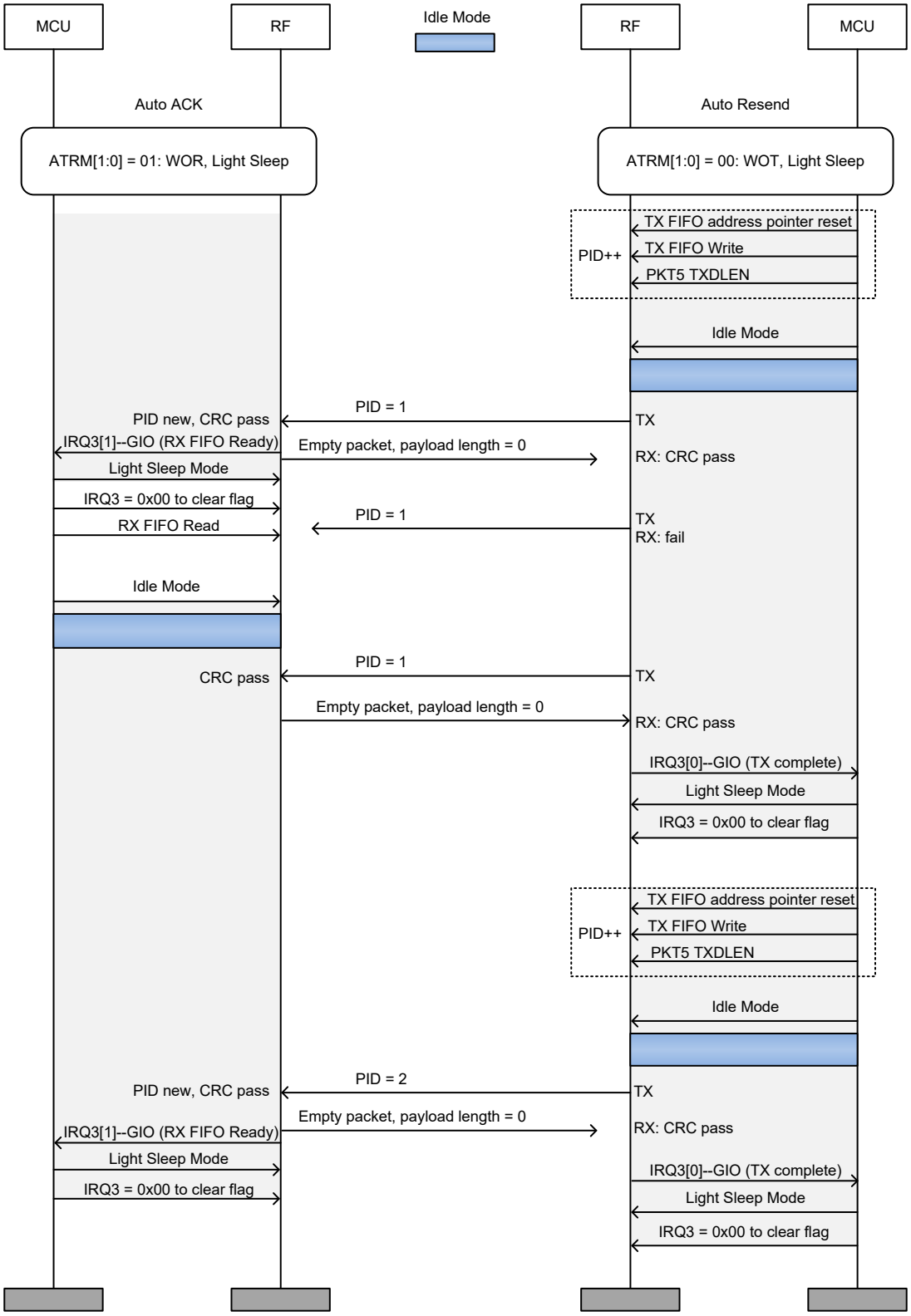


Figure 37. ATR + ARK Message Flowchart Example 2

Abbreviation

ADC: Analog to Digital Converter

AFC: Automatic Frequency Compensation

AGC: Automatic Gain Control

ARK: Auto-Resend and Auto-Ack

ATR: Automatic-Transmit-Receive

BER: Bit Error Rate

CD: Carrier Detect

CFO: Carrier Frequency Offset

CP: Charge Pump

CRC: Cyclic Redundancy Check

DCOC: DC Offset Correct

DSM: Delta Sigma Modulator

FEC: Forward Error Correction

FIFO: First In First Out

GFSK: Gaussian Frequency Shift Keying

ID: Identifier

IF: Intermedia Frequency

IIR: Infinite Impulse Response

IRQ: Interrupt Request

ISM: Industrial, Scientific and Medical

LNA: Low Noise Amplifier

LO: Local Oscillator

MCU: Mico Controller Unit

MMD: Multi-Mode Divider

OW: Overwrite

PA: Power Amplifier

PD: Power Down

PFD: Phase Frequency Detector (for PLL)

PLL: Phase Lock Loop

POR: Power On Reset

PVT: Process-Voltage-Temperature

RBCLK: RX Bit Clock

RSSI: Received Signal Strength Indicator

RX: Receiver

SNR: Signal Noise Ratio

SPI: Serial Port Interface

SX: Synthesizer

SYCK: System Clock for digital circuit

SYNC/SYNCWORD: Synchronization Word

TBCLK: TX Bit Clock

TRX: TX/RX

TX: Transmitter

VCO: Voltage Controlled Oscillator

WOR: Wake-on-RX

WOT: Wake-on-TX

WTM: Wake-up Timer Mode

XCLK: Crystal Clock

XO: Crystal Oscillator

XTAL: Crystal

Application Circuits

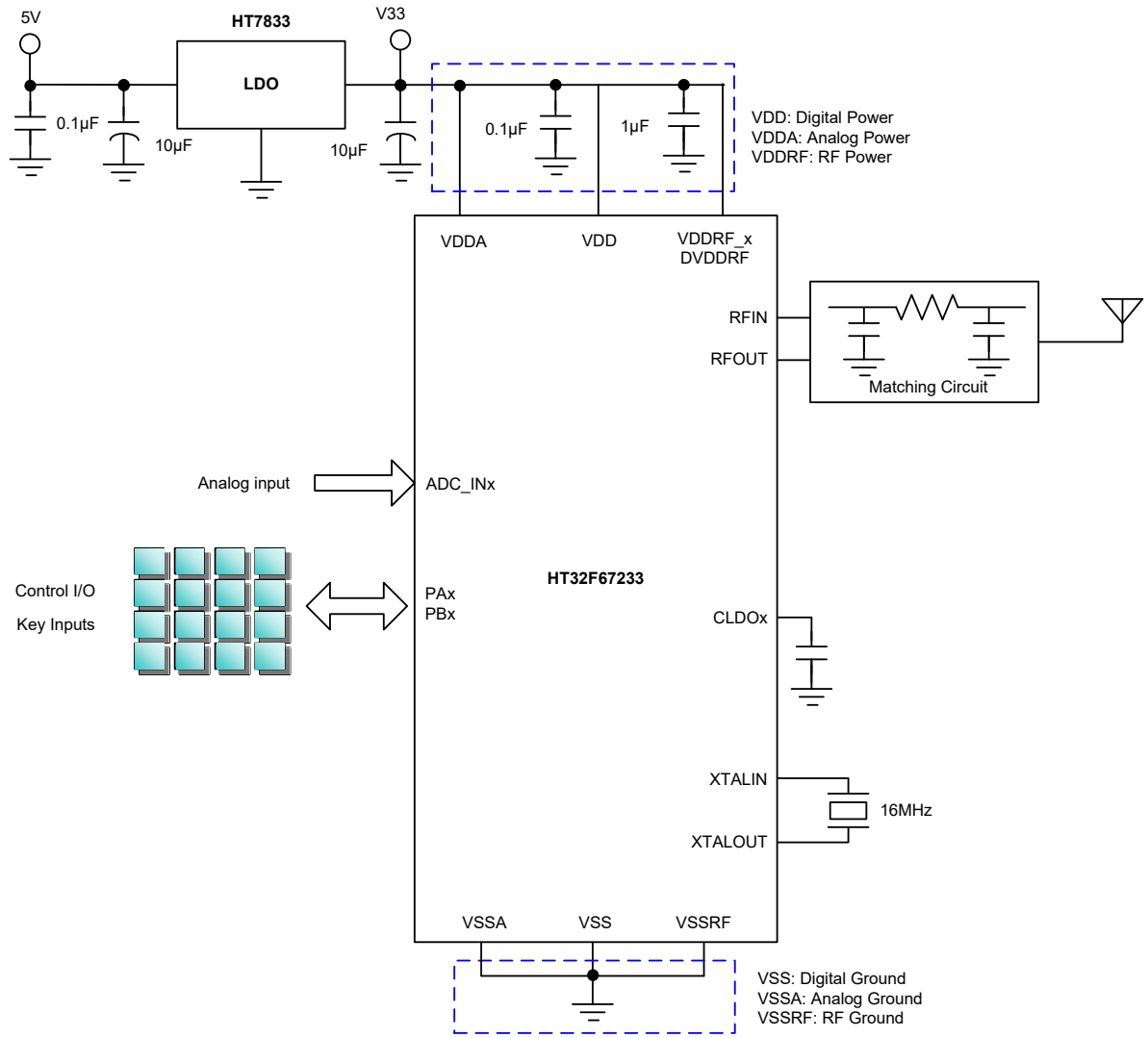


Figure 38. RF Transceiver Application Circuit

5 Pin Assignment

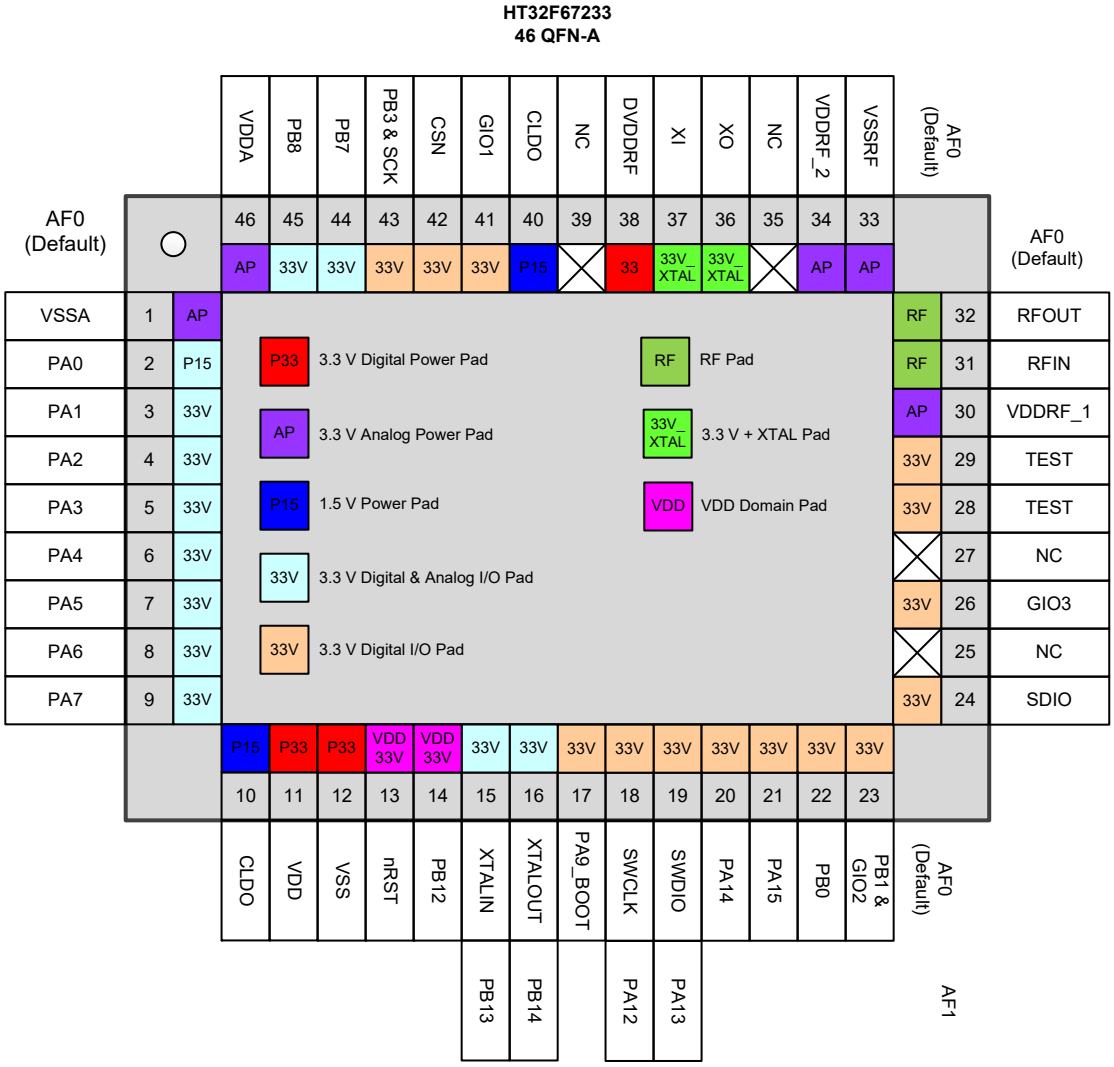


Figure 39. 46-pin QFN Pin Assignment

Table 4. Pin Assignment for 46-pin SSOP Package

Package	Alternate Function Mapping															
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
46QFN	System Default	GPIO	ADC	N/A	GPTM	SPI	USART /UART	I²C	N/A	N/A	N/A	N/A	N/A	SCTM	N/A	System Other
2	PA0		ADC_IN0		GT_CH0	SPI_SCK	USR_RTS	I2C_SCL								
3	PA1		ADC_IN1		GT_CH1	SPI_MOSI	USR_CTS	I2C_SDA								
4	PA2		ADC_IN2		GT_CH2	SPI_MISO	USR_TX									
5	PA3		ADC_IN3		GT_CH3	SPI_SEL	USR_RX									
6	PA4		ADC_IN4		GT_CH0	SPI_SCK	UR_TX	I2C_SCL								
7	PA5		ADC_IN5		GT_CH1	SPI_MOSI	UR_RX	I2C_SDA								
8	PA6		ADC_IN6		GT_CH2	SPI_MISO										
9	PA7		ADC_IN7		GT_CH3	SPI_SEL										
10	CLDO															
11	VDD															
12	VSS															
13	nRST															
14	PB12					SPI_MISO	UR_RX							SCTM0		WAKEUP
15	XTALIN	PB13					UR_TX	I2C_SCL								
16	XTALOUT	PB14					UR_RX	I2C_SDA								
17	PA9_BOOT					SPI_MOSI								SCTM1		CKOUT
18	SWCLK	PA12														
19	SWDIO	PA13														
20	PA14				GT_CH0	SPI_SEL	USR_RTS	I2C_SCL								
21	PA15				GT_CH0	SPI_SCK	USR_CTS	I2C_SDA						SCTM1		
22	PB0				GT_CH1	SPI_MOSI	USR_TX	I2C_SCL								
23	PB1 & GIO2				GT_CH1	SPI_MISO	USR_RX	I2C_SDA						SCTM0		
24	SDIO															
25	NC															
26	GIO3															
27	NC															
28	TEST															
29	TEST															
30	VDDRF															
31	RFIN															
32	RFOUT															
33	VSSRF															
34	VDDRF															
35	NC															
36	XO															
37	XI															
38	DVDDRF															
39	NC															
40	CLDO															
41	GIO1															
42	CSN															
43	PB3 & SCK				GT_CH2	SPI_SCK	UR_RX							SCTM1		
44	PB7				GT_CH3	SPI_MISO	UR_TX	I2C_SCL								
45	PB8				GT_CH3	SPI_SEL	UR_RX	I2C_SDA								
46	VDDA															
1	VSSA															

Table 5. Pin Description

Pin number	Pin Name	Type (1)	I/O Structure (2)	Output Driving	Description
46QFN					Default function (AF0)
44	PB7	AI/O	33V	4/8/12/16 mA	PB7
45	PB8	AI/O	33V	4/8/12/16 mA	PB8
46	VDDA	P	—	—	Analog voltage for ADC
1	VSSA	P	—	—	Analog ground for ADC
12	VSS	P	—	—	Ground reference for digital I/O
2	PA0	AI/O	33V	4/8/12/16 mA	PA0
3	PA1	AI/O	33V	4/8/12/16 mA	PA1
4	PA2	AI/O	33V	4/8/12/16 mA	PA2
5	PA3	AI/O	33V	4/8/12/16 mA	PA3
6	PA4	AI/O	33V	4/8/12/16 mA	PA4, this pin provides a UART_TX function in the Boot loader mode.
7	PA5	AI/O	33V	4/8/12/16 mA	PA5, this pin provides a UART_RX function in the Boot loader mode.
8	PA6	AI/O	33V	4/8/12/16 mA	PA6
9	PA7	AI/O	33V	4/8/12/16 mA	PA7
10	CLDO	P	—	—	Core power LDO V_{CORE} output It must be connected a 1 μF capacitor as close as possible between this pin and VSS pin.
11	VDD	P	—	—	Voltage for digital I/O
12	VSS	P	—	—	Ground reference for digital I/O
13	nRST (3)	I (V_{DD})	33V_PU	—	External reset pin and external wakeup pin in the Power-Down mode
14	PB12 (3)	I/O (V_{DD})	33V	4/8/12/16 mA	PB12
15	PB13	AI/O	33V	4/8/12/16 mA	XTALIN
16	PB14	AI/O	33V	4/8/12/16 mA	XTALOUT
17	PA9	I/O	33V_PU	4/8/12/16 mA	PA9_BOOT
18	PA12	I/O	33V_PU	4/8/12/16 mA	SWCLK
19	PA13	I/O	33V_PU	4/8/12/16 mA	SWDIO
20	PA14	I/O	33V	4/8/12/16 mA	PA14
21	PA15	I/O	33V	4/8/12/16 mA	PA15
22	PB0	I/O	33V	4/8/12/16 mA	PB0
23	PB1 & GIO2	I/O	33V	4/8/12/16 mA	PB1 If the RF function is to be used, the PB1 pin should be set to AF5 (SPI_MISO) and the GIO2S[2:0] bits must be fixed at 001.
24	SDIO	DI/O	—	—	RF SPI data input/output
25	NC	—	—	—	—
26	GIO3	DI/O	—	—	RF Multi-function I/O 3
27	NC	–	—	—	—
28	TEST	–	—	—	Recommend no connection
29	TEST	–	—	—	Recommend no connection
30	VDDRF_1	P	—	—	RF Analog positive power supply
31	RFIN	AI	—	—	RF LNA input
32	RFOUT	AO	—	—	RF power amplifier output
33	VSSRF	P	—	—	RF ground

Pin number	Pin Name	Type (1)	I/O Structure (2)	Output Driving	Description
46QFN					Default function (AF0)
34	VDDRF_2	P	—	—	RF Analog positive power supply
35	NC	—	—	—	—
36	XO	AO	—	—	RF Crystal oscillator output
37	XI	AI	—	—	RF Crystal oscillator input
38	DVDDRF	P	—	—	RF Digital positive power supply
39	NC	—	—	—	—
40	CLDO	P	—	—	LDO output, connected to a bypass capacitor
41	GIO1	DI/O	—	—	RF Multi-function I/O 1
42	CSN	DI	—	—	RF SPI chip select input, low active
43	PB3 & SCK	I/O	33V	4/8/12/16 mA	PB3 If the RF function is to be used, the PB3 pin should be set to AF5(SPI_SCK).
	VSS/EP (4)	P	—	—	Exposed pad, must be connected to ground

Note: 1. I = Input, O = Output, A = Analog Port, P = Power Supply, V_{DD} = V_{DD} Power.
2. 33V = 3.3 V operation I/O type, PU = Pull-up.
3. These pins are located at the V_{DD} power domain.
4. The backside plate of EP shall be well soldered to ground on PCB, otherwise it will downgrade RF performance.
5. In the Boot loader mode, the UART interface is available for communication.

6 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	External Main Supply Voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External Analog Supply Voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{IN}	Input Voltage on I/O	V_{SS} - 0.3	V_{DD} + 0.3	V
T_A	Ambient Operating Temperature Range	-40	85	°C
T_{STG}	Storage Temperature Range	-60	150	°C
T_J	Maximum Junction Temperature	—	125	°C
P_D	Total Power Dissipation	—	500	mW
V_{ESD}	Electrostatic Discharge Voltage – Human Body Mode	-2000	2000	V

The device is ESD sensitive. HBM (Human Body Mode) is based on MIL-STD-883.

Recommended DC Operating Conditions

Table 7. Recommended DC Operating Conditions

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	I/O OPerating Voltage	—	2.0	3.3	3.6	V
V_{DDA}	Analog Operating Voltage	—	2.5	3.3	3.6	V

RF Characteristics

Table 8. RF Characteristics

T_A = 25 °C, V_{DD} = 3.3 V, f_{XTAL} = 16 MHz, FSK modulation with matching circuit and low/high pass filter, RF output is powered by V_{DD} (3.3 V), unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
T_{OP}	Operating Temperature	—	-40	—	85	°C
V_{DD}	Supply Voltage	—	2.0	3.3	3.6	V
Digital I/Os						
V_{IH}	High Level Input Voltage	—	0.7 × V_{DD}	—	V_{DD}	V
V_{IL}	Low Level Input Voltage	—	0	—	0.3 × V_{DD}	V
V_{OH}	High Level Output Voltage	I_{OH} = -5 mA	0.8 × V_{DD}	—	V_{DD}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 5 mA	0	—	0.2 × V_{DD}	V

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Current Consumption						
I_{Sleep}	Deep Sleep Mode Current Consumption	—	—	0.4	1.0	μA
I_{IL}	Idle Mode Current Consumption	LIRC on, X'tal off	—	1.6	—	μA
	Light Sleep Mode Current Consumption	X'tal on	—	0.6	—	mA
$I_{Standby}$	Standby Mode Current Consumption @ 315/433 MHz	X'tal on, Synthesizer on	—	3.9	—	mA
	Standby Mode Current Consumption @ 868/915 MHz		—	3.9	—	
	433 MHz Band Current Consumption	RX mode @ 2 Kbps	—	5.8	—	mA
		RX mode @ 250 Kbps	—	6.4	—	
		TX mode @ 0 dBm P_{OUT}	—	19	—	
		TX mode @ 10 dBm P_{OUT}	—	33	—	
		TX mode @ 13 dBm P_{OUT}	—	43	—	
		TX mode @ 19 dBm P_{OUT}	—	71	—	
	868 MHz Band Current Consumption	RX mode @ 2 Kbps	—	6.8	—	mA
		RX mode @ 250 Kbps	—	7.5	—	
		TX mode @ 0 dBm P_{OUT}	—	19	—	
		TX mode @ 10 dBm P_{OUT}	—	35	—	
		TX mode @ 13 dBm P_{OUT}	—	47	—	
		TX mode @ 19 dBm P_{OUT}	—	88	—	
R_{PH}	Pull-high Resistance for I/O Ports	3.3 V	—	33	—	kΩ
RF Characteristics						
f_{RF}	RF Frequency Band	315 MHz band	—	315	—	MHz
		433 MHz band	—	433.92	—	
		470 ~ 510 MHz band	—	490	—	
		868 MHz band	—	868.3	—	
		915 MHz band	—	915	—	
DR	Data Rate	OOK modulation	0.5	—	20	Kbps
		GFSK modulation	2	—	250	
f_{LIRC}	RF Internal Low Frequency RC Oscillator	3.3 V	-10%	32.768	+10%	kHz
Transmitter						
P_{OUT}	TX Output Power	433 MHz band	0	—	20	dBm
		868 MHz band	0	—	20	
S.E.$_{TX}$	TX Spurious Emission (P_{OUT} = 10 dBm)	f < 1 GHz	—	—	-36	dBm
		47 MHz < f < 74 MHz	—	—	-54	
		87.5 MHz < f < 118 MHz				
		174 MHz < f < 230 MHz				
		470 MHz < f < 862 MHz				
		2nd, 3rd Harmonic	—	—	-30	

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Receiver						
$t_{ST,RX}$	RX Settling Time	Light Sleep mode to RX mode	—	150	—	μs
P_{Sens}	433 MHz RX Sensitivity @ BER = 0.1 %	2 Kbps (f_{DEV} = 8 kHz)	—	-117	—	dBm
		10 Kbps (f_{DEV} = 40 kHz)	—	-110	—	
		50 Kbps (f_{DEV} = 18.75 kHz)	—	-107	—	
		125 Kbps (f_{DEV} = 46.875 kHz)	—	-103	—	
		250 Kbps (f_{DEV} = 93.75 kHz)	—	-100	—	
	868 MHz RX Sensitivity @ BER = 0.1 %	2 Kbps (f_{DEV} = 8 kHz)	—	-116	—	dBm
		10 Kbps (f_{DEV} = 40 kHz)	—	-110	—	
		50 Kbps (f_{DEV} = 18.75 kHz)	—	-106	—	
		125 Kbps (f_{DEV} = 46.875 kHz)	—	-103	—	
		250 Kbps (f_{DEV} = 93.75 kHz)	—	-100	—	
$P_{IN,max}$	Maxmum Input Power	@ BER < 0.1 %	—	—	10	dBm
IR	Image Rejection	—	—	25	–	dB
S.E.$_{RX}$	RX Spurious	25 MHz ~ 1 GHz	—	—	-57	dBm
		Above 1 GHz	—	—	-47	
	RSSI Range	AGC on	-110	—	-10	dBm
LO Characteristics						
f_{LO}	RF Frequency Coverage Range	315 MHz band	290	—	335	MHz
		433 MHz band	415	—	490	
		470 ~ 510 MHz band	470	—	510	
		868 MHz band	830	—	1000	
		915 MHz band	870	—	1050	
f_{STEP}	LO Frequency Resolution	—	—	—	1	kHz
PN_{LO}	433 MHz Phase Noise	@ 100 kHz offset	—	-91	—	dBc/Hz
		@ 1 MHz offset	—	-110	—	
	868 MHz Phase Noise	@ 100 kHz offset	—	-82	—	
		@ 1 MHz offset	—	-105	—	
Crystal Oscillator						
f_{XTAL}	X'tal Frequency	—	—	16	—	MHz
ESR	X'tal Equivalent Series Resistance	—	—	—	100	Ω
C_{LOAD}	X'tal Capacitor Load	—	12	16	20	pF
TOL	X'tal Tolerance (Note)	—	-20	—	+20	ppm
t_{SU}	X'tal Startup Time	49US XO	—	—	1	ms

Note: 1. When the data rate is 2 Kbps at 315/433.92 MHz, an X'tal with a tolerance of ±10 ppm should be used.
2. When the data rate is 2 Kbps at 868/915 MHz, an X'tal with a tolerance of ±5 ppm should be used.

RF SPI Characteristics

Table 9. RF SPI Characteristics

T_A = 25 °C

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
f_{SCK}	RF SCK Frequency	—	—	4	—	MHz
t_{SCKH}	RF SCK High Time	—	62.5	—	—	ns
t_{SCKL}	RF SCK Low Time	—	62.5	—	—	ns
t_{S_SDIO}	RF SDIO Input Setup Time	—	20	—	—	ns
t_{H_SDIO}	RF SDIO Input Hold Time	—	20	—	—	ns
t_{S_CSN}	RF CSN to SCK Active	—	30	—	—	ns
t_{H_CSN}	RF SCK Inactive to CSN Inactive	—	30	—	—	ns

On-Chip LDO Voltage Regulator Characteristics

Table 10. LDO Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{LDO}	Internal Regulator Output Voltage	V_{DD} ≥ 2.0 V Regulator input @ I_{LDO} = 35 mA and voltage variant = ±5 %, After trimming.	1.425	1.5	1.57	V
I_{LDO}	Output Current	V_{DD} = 2.0 V Regulator input @ V_{LDO} = 1.5 V	—	30	35	mA
C_{LDO}	External Filter Capacitor Value for Internal Core Power Supply	The capacitor value is dependent on the core power current consumption	—	1	—	μF

Power Consumption

Table 11. Power Consumption Characteristics

T_A = 25 °C, unless otherwise specified

Symbol	Parameter	Conditions	Typ.	Max.		Unit
				25 °C	85 °C	
I_{DD}	Supply Current (Run Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 40 MHz, f_{BUS} = 40 MHz, All peripherals enabled	9.3	10.6	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 40 MHz, f_{BUS} = 40 MHz, All peripherals disabled	6.0	6.8	—	mA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, All peripherals enabled	39	52	—	μA
		V_{DD} = 3.3 V, HSI off, PLL off, LSI on, f_{CPU} = 32 kHz, f_{BUS} = 32 kHz, All peripherals disabled	36	48	—	μA
	Supply Current (Sleep Mode)	V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 0 MHz, f_{BUS} = 40 MHz, All peripherals enabled	4.9	5.6	—	mA
		V_{DD} = 3.3 V, HSI = 8 MHz, PLL = 40 MHz, f_{CPU} = 0 MHz, f_{BUS} = 40 MHz, All peripherals disabled	1.0	1.15	—	mA
	Supply Current (Deep-Sleep1 Mode)	V_{DD} = 3.3 V, All clock off (HSE/HSI/PLL), LDO in low power mode, LSI on	32.0	49.0	—	μA
	Supply Current (Deep-Sleep2 Mode)	V_{DD} = 3.3 V, All clock off (HSE/HSI/PLL), LDO off DMOS on, LSI on	3.67	7.5	—	μA
	Supply Current (Power-Down Mode)	V_{DD} = 3.3 V, LDO off, DMOS off, LSI on	1.3	2.0	—	μA

Note: 1. HSE means high speed external oscillator. HSI means 8 MHz high speed internal oscillator.
2. LSI means 32 kHz low speed internal oscillator.
3. Code = while (1) { 208 NOP } executed in Flash.
4. f_{BUS} means f_{HCLK} and f_{PCLK}.

Reset and Supply Monitor Characteristics

Table 12. V_{DD} Power Reset Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{POR}	Power on reset threshold (Rising Voltage on V_{DD})	T_A = -40 °C ~ 85 °C	1.66	1.79	1.90	V
V_{PDR}	Power down reset threshold (Falling Voltage on V_{DD})		1.49	1.64	1.78	V
$V_{PORHYST}$	POR hysteresis	—	—	150	—	mV
t_{POR}	Reset delay time	V_{DD} = 3.3 V	—	0.1	0.2	ms

Note: 1. Data based on characterization results only, not tested in production.
2. If the LDO is turned on, the V_{DD} POR has to be in the de-assertion condition. When the V_{DD} POR is in the assertion state then the LDO will be turned off.

Table 13. LVD/BOD Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{BOD}	Voltage of Brown Out Detection	After factory-trimmed (V_{DD} Falling edge)		2.02	2.1	2.18	V
V_{LVD}	Voltage of Low Voltage Detection	(V_{DD} Falling edge)	LVDS = 000	2.17	2.25	2.33	V
			LVDS = 001	2.32	2.4	2.48	V
			LVDS = 010	2.47	2.55	2.63	V
			LVDS = 011	2.62	2.7	2.78	V
			LVDS = 100	2.77	2.85	2.93	V
			LVDS = 101	2.92	3.0	3.08	V
			LVDS = 110	3.07	3.15	3.23	V
			LVDS = 111	3.22	3.3	3.38	V
$V_{LVDHTST}$	LVD Hysteresis	V_{DD} = 3.3 V	—	—	100	—	mV
t_{suLVD}	LVD Setup Time	V_{DD} = 3.3 V	—	—	—	5	μs
t_{atLVD}	LVD Active Delay Time	V_{DD} = 3.3 V	—	—	—	—	μs
I_{DDLVD}	Operation Current (2)	V_{DD} = 3.3 V	—	—	5	15	μA

Note: 1. Data based on characterization results only, not tested in production.
2. Bandgap current is not included.
3. LVDS field is in the PWRCU LVDCSR register

External Clock Characteristics

Table 14. High Speed External Clock (HSE) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSE}	High Speed External Oscillator Frequency (HSE)	—	4	—	16	MHz
C_L	Load Capacitance	V_{DD} = 3.3 V, R_{ESR} = 100 Ω @ 16 MHz	—	—	22	pF
R_{FHSE}	Internal Feedback Resistor Between XTALIN and XTALOUT Pins	—	—	1	—	MΩ
R_{ESR}	Equivalent Series Resistance	V_{DD} = 3.3 V, C_L = 12 pF @ 16 MHz, HSEDR = 0	—	—	160	Ω
		V_{DD} = 2.4 V, C_L = 12 pF @ 16 MHz, HSEDR = 1				
D_{HSE}	HSE Oscillator Duty Cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Current Consumption	V_{DD} = 3.3 V @ 16 MHz	—	TBD	—	mA
I_{PWDHSE}	HSE Oscillator Power Down Current	V_{DD} = 3.3 V	—	—	0.01	μA
t_{SUHSE}	HSE Oscillator Startup Time	V_{DD} = 3.3 V	—	—	4	ms

Note: The following guidelines are recommended to increase the stability of the crystal circuit of the HSE clock in the PCB layout:
1. The crystal oscillator should be located as close as possible to the MCU to keep the trace lengths as short as possible to reduce any parasitic capacitance.
2. Shield lines in the vicinity of the crystal by using a ground plane to isolate signals and reduce noise.
3. Keep any high frequency signal lines away from the crystal area to prevent any crosstalk adverse effects.

Internal Clock Characteristics

Table 15. High Speed Internal Clock (HSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Operation Range	—	2.0	—	3.6	V
f_{HSI}	HSI Frequency	V_{DD} = 3.3 V @ 25 °C	—	8	—	MHz
ACC_{HSI}	Factory Calibrated Hsi Oscillator FRequency Accuracy	V_{DD} = 3.3 V, T_A = 25 °C	-2	—	2	%
		V_{DD} = 2.5 V ~ 3.6 V, T_A = -40 °C ~ 85 °C	-3	—	3	%
		V_{DD} = 2.0 V ~ 3.6 V T_A = -40 °C ~ 85 °C	-4	—	4	%
Duty	HSI Duty Cycle	f_{HSI} = 8 MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator Supply Current	f_{HSI} = 8 MHz	—	300	500	μA
	HSI Power Down Current		—	—	0.05	μA
t_{suHSI}	HSI Startup Time	f_{HSI} = 8 MHz	-—	—	10	μs

Table 16. Low Speed Internal Clock (LSI) Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency (LSI)	V_{DD} = 3.3 V, T_A = -40 °C ~ 85 °C	21	32	43	kHz
ACC_{LSI}	LSI Frequency Accuracy	After factory-trimmed, V_{DD} = 3.3 V, T_A = 25 °C	-10	—	+10	%
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD} = 3.3 V, T_A = 25 °C	—	0.4	0.8	μA
t_{SULSI}	LSI Oscillator Startup Time	V_{DD} = 3.3 V, T_A = 25 °C	—	—	100	μs

PLL Characteristics

Table 17. PLL Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLLIN}	PLL Input Clock	—	4	—	16	MHz
f_{CK_PLL}	PLL Output Clock	—	16	—	48	MHz
t_{LOCK}	PLL Lock Time	—	—	200	—	μs

Memory Characteristics

Table 18. Flash Memory Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{ENDU}	Number of Guaranteed Program / Erase Cycles before Failure (Endurance)	T_A = -40 °C ~ 85 °C	20	—	—	K cycles
t_{RET}	Data Retention Time	T_A = -40 °C ~ 85 °C	10	—	—	Years
t_{PROG}	Word Programming Time	T_A = -40 °C ~ 85 °C	20	—	—	μs
t_{ERASE}	Page Erase Time	T_A = -40 °C ~ 85 °C	2	—	—	ms
t_{MERASE}	Mass Erase Time	T_A = -40 °C ~ 85 °C	10	—	—	ms

I/O Port Characteristics

Table 19. I/O Port Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I_{IL}	Low Level Input Current	3.3 V I/O	V_I = V_{SS}, On-chip pull-up resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High Level Input Current	3.3 V I/O	V_I = V_{DD}, On-chip pull-down resister disabled.	—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low Level Input Voltage	3.3 V I/O		-0.5	—	V_{DD} × 0.35	V
		Reset pin		-0.5	—	V_{DD} × 0.35	V
V_{IH}	High Level Input Voltage	3.3 V I/O		V_{DD} × 0.65	—	V_{DD} + 0.5	V
		Reset pin		V_{DD} × 0.65	—	V_{DD} + 0.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3 V I/O		—	0.12 × V_{DD}	—	mV
		Reset pin		—	0.12 × V_{DD}	—	mV
I_{OL}	Low Level Output Current (GPIO Sink Current)	3.3 V I/O 4 mA drive, V_{OL} = 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OL} = 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, V_{OL} = 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, V_{OL} = 0.4 V		16	—	—	mA
I_{OH}	High Level Output Current (GPIO Source Current)	3.3 V I/O 4 mA drive, V_{OH} = V_{DD} - 0.4 V		4	—	—	mA
		3.3 V I/O 8 mA drive, V_{OH} = V_{DD} - 0.4 V		8	—	—	mA
		3.3 V I/O 12 mA drive, V_{OH} = V_{DD} - 0.4 V		12	—	—	mA
		3.3 V I/O 16 mA drive, V_{OH} = V_{DD} - 0.4 V		16	—	—	mA
V_{OL}	Low Level Output Voltage	3.3 V 4 mA drive I/O, I_{OL} = 4 mA		—	—	0.4	V
		3.3 V 8 mA drive I/O, I_{OL} = 8 mA		—	—	0.4	V
		3.3 V 12 mA drive I/O, I_{OL} = 12 mA		—	—	0.4	V
		3.3 V 16 mA drive I/O, I_{OL} = 16 mA		—	—	0.4	V
V_{OH}	High Level Output Voltage	3.3 V 4 mA drive I/O, I_{OH} = 4 mA		V_{DD} - 0.4	—	—	V
		3.3 V 8 mA drive I/O, I_{OH} = 8 mA		V_{DD} - 0.4	—	—	V
		3.3 V 12 mA drive I/O, I_{OH} = 12 mA		V_{DD} - 0.4	—	—	V
		3.3 V 16 mA drive I/O, I_{OH} = 16 mA		V_{DD} - 0.4	—	—	V
R_{PU}	Internal Pull-up Resistor	3.3 V I/O		—	46	—	kΩ
R_{PD}	Internal Pull-down Resistor	3.3 V I/O		—	46	—	kΩ

ADC Characteristics

Table 20. ADC Characteristics

T_A = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Operating Voltage	—	2.5	3.3	3.6	V
V_{ADCIN}	A/D Converter Input Voltage Range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference Voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current Consumption	V_{DDA} = 3.3 V	—	1	TBD	mA
I_{ADC_DN}	Power Down Current Consumption	V_{DDA} = 3.3 V	—	—	0.1	μA
f_{ADC}	A/D Converter Clock	—	0.7	—	16	MHz
f_S	Sampling Rate	—	0.05	—	1	Msps
t_{DL}	Data Latency	—	—	12.5	—	$1/f_{ADC}$ Cycles
$t_{S\&H}$	Sampling & Hold Time	—	—	3.5	—	$1/f_{ADC}$ Cycles
$t_{ADCCONV}$	A/D Converter Conversion Time	ADST[7:0] = 0x02	—	16	—	$1/f_{ADC}$ Cycles
R_I	Input Sampling Switch Resistance	—	—	—	1	kΩ
C_I	Input Sampling Capacitance	No pin/pad capacitance included	—	16	—	pF
t_{SU}	Startup Time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-Linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±2	±5	LSB
DNL	Differential Non-Linearity Error	f_S = 750 ksps, V_{DDA} = 3.3 V	—	±1	—	LSB
E_O	Offset Error	—	—	—	±10	LSB
E_G	Gain Error	—	—	—	±10	LSB

Note: 1. Data based on characterization results only, not tested in production.

2. Due to the A/D Converter input channel and GPIO pin-shared function design limitation, the V_{DDA} supply power of the A/D Converter has to be equal to the V_{DD} supply power of the MCU in the application circuit.

3. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, R_I is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $3.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S is not allowed to have an arbitrarily large value.

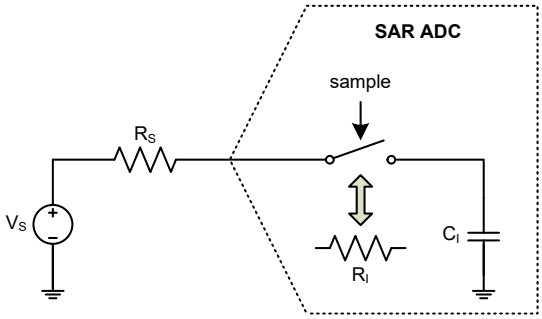


Figure 40. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below ¼ LSB is ensured by using the following equation:

$$R_S < \frac{3.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

Where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where the A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, R_S may be larger than the value indicated by the equation above.

SCTM/GPTM Characteristics

Table 21. SCTM/GPTM Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{TM}	Timer Clock Source for SCTM/GPTM	—	—	—	48	MHz
t_{RES}	Timer Resolution Time	—	—	—	—	f_{TM}
f_{EXT}	External Signal Frequency on Channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer Resolution	—	—	—	16	bits

I²C Characteristics

Table 22. I²C Characteristics

Symbol	Parameter	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
f_{SCL}	SCL Clock Frequency	—	100	—	400	—	1000	kHz
$t_{SCL(H)}$	SCL Clock High Time	4.5	—	1.125	—	0.45	—	μs
$t_{SCL(L)}$	SCL Clock Low Time	4.5	—	1.125	—	0.45	—	μs
t_{FALL}	SCL and SDA Fall Time	—	1.3	—	0.34	—	0.135	μs
t_{RISE}	SCL and SDA Rise Time	—	1.3	—	0.34	—	0.135	μs
$t_{SU(SDA)}$	SDA Data Setup Time	500	—	125	—	50	—	ns
$t_{H(SDA)}$	SDA Data Hold Time (5)	0	—	0	—	0	—	ns
	SDA Data Hold Time (6)	100	—	100	—	100	—	ns
$t_{VD(SDA)}$	SDA Data Valid Time	—	1.6	—	0.475	—	0.25	μs
$t_{SU(STA)}$	Start Condition Setup Time	500	—	125	—	50	—	ns
$t_{H(STA)}$	Start Condition Hold Time	0	—	0	—	0	—	ns
$t_{SU(STO)}$	Stop Condition Setup Time	500	—	125	—	50	—	ns

Note: 1. Data based on characterization results only, not tested in production.
2. To achieve 100 kHz standard mode, the peripheral clock frequency must be higher than 2 MHz.
3. To achieve 400 kHz fast mode, the peripheral clock frequency must be higher than 8 MHz.
4. To achieve 1 MHz fast mode plus, the peripheral clock frequency must be higher than 20 MHz.

5. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 0 and SEQFILTER = 00.
6. The above characteristic parameters of the I²C bus timing are based on: COMBFILTEREN = 1 and SEQFILTER = 00.

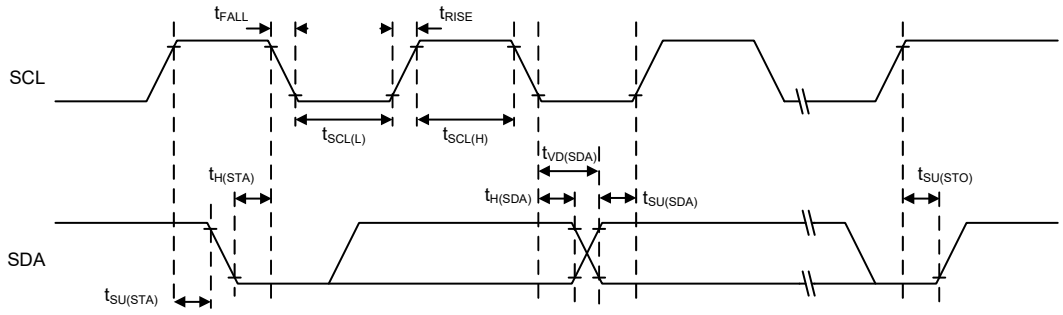


Figure 41. I²C Timing Diagrams

SPI Characteristics

Table 23. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SPI Master mode						
f_{SCK}	SPI Master Output SCK Clock Frequency	SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/2$	MHz
$t_{SCK(H)}$ $t_{SCK(L)}$	SCK Clock High and Low Time	—	$t_{SCK}/2 - 2$	—	$t_{SCK}/2 + 1$	ns
$t_{V(MO)}$	Data Output Valid Time	—	—	—	5	ns
$t_{H(MO)}$	Data Output Hold Time	—	2	—	—	ns
$t_{SU(MI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(MI)}$	Data Input Hold Time	—	5	—	—	ns
SPI Slave mode						
f_{SCK}	SPI Slave Input SCK Clock Frequency	SPI peripheral clock frequency f_{PCLK}	—	—	$f_{PCLK}/3$	MHz
$Duty_{SCK}$	SPI Slave Input SCK Clock Duty Cycle	—	30	—	70	%
$t_{SU(SEL)}$	SEL Enable Setup Time	—	3 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL Enable Hold Time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data Output Access Time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data Output Disable Time	—	—	—	10	ns
$t_{V(SO)}$	Data Output Valid Time	—	—	—	25	ns
$t_{H(SO)}$	Data Output Hold Time	—	15	—	—	ns
$t_{SU(SI)}$	Data Input Setup Time	—	5	—	—	ns
$t_{H(SI)}$	Data Input Hold Time	—	4	—	—	ns

Note: 1. f_{SCK} is SPI output/input clock frequency and $t_{SCK} = 1/f_{SCK}$.
2. f_{PCLK} is SPI peripheral clock frequency and $t_{PCLK} = 1/f_{PCLK}$.

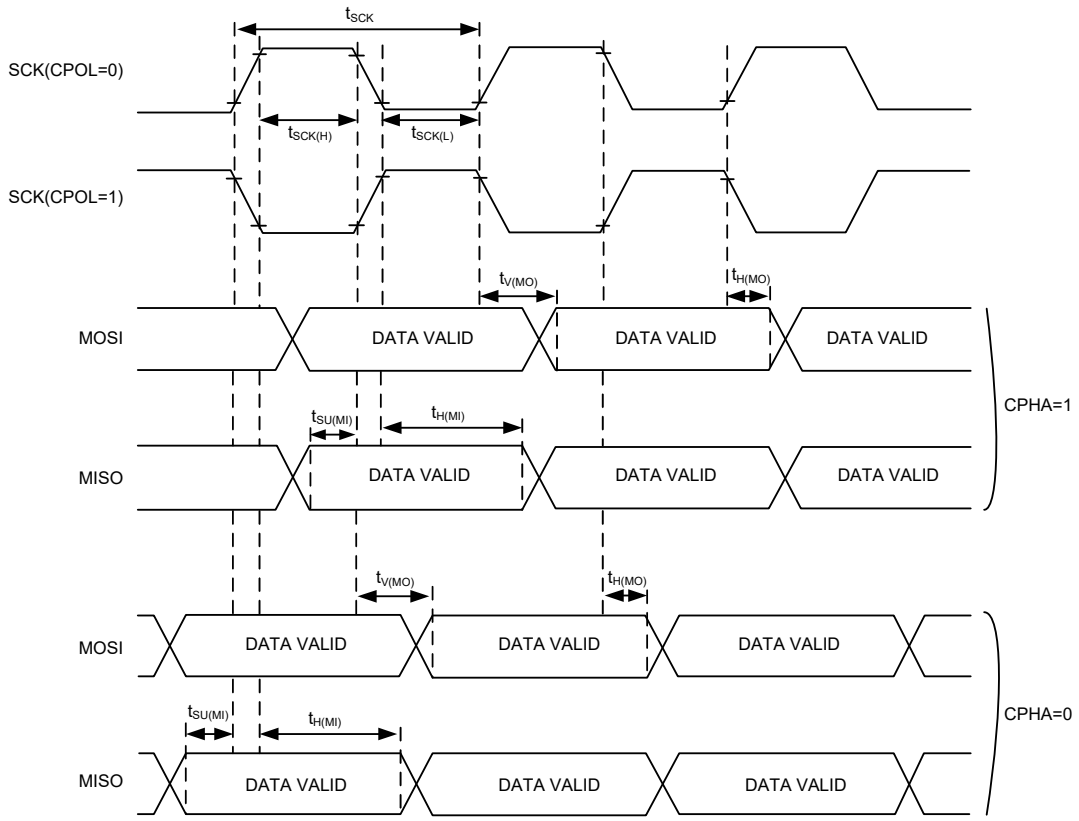


Figure 42. SPI Timing Diagrams – SPI Master Mode

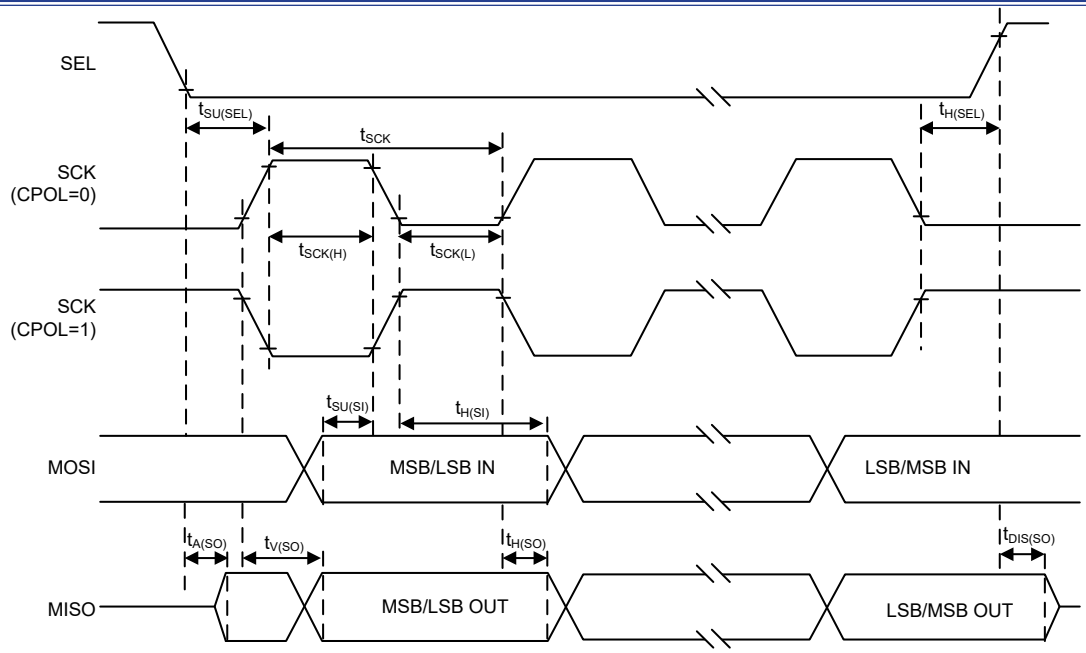


Figure 43. SPI Timing Diagrams – SPI Slave Mode with CPHA = 1

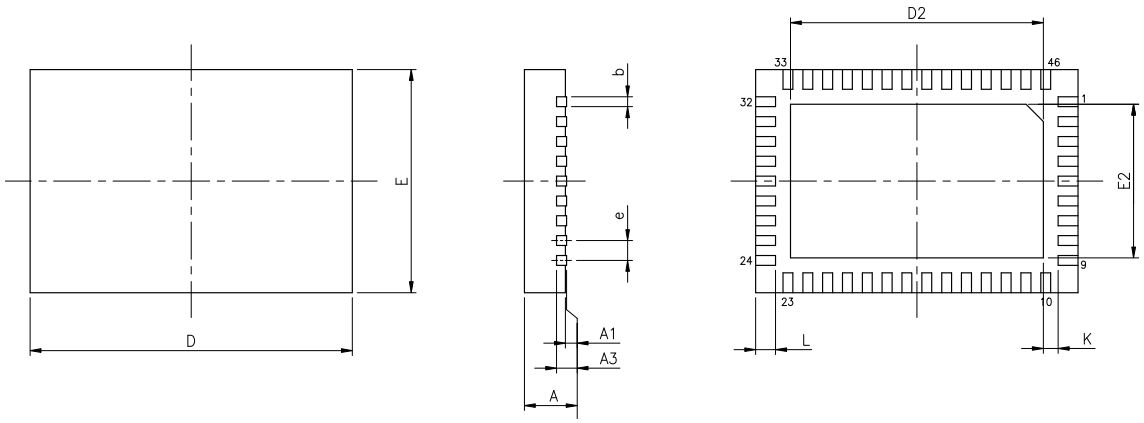
7 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

SAW Type 46-pin QFN (6.5mm × 4.5mm × 0.75mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.028	0.030	0.031
A1	0.000	0.001	0.002
A3	—	0.008 REF	—
b	0.006	0.008	0.010
D	—	0.256 BSC	—
E	—	0.177 BSC	—
e	—	0.016 BSC	—
D2	0.197	—	0.205
E2	0.118	—	0.126
L	0.014	0.016	0.018
K	0.008	—	—

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	—	0.203 REF	—
b	0.15	0.20	0.25
D	—	6.50 BSC	—
E	—	4.50 BSC	—
e	—	0.40 BSC	—
D2	5.00	—	5.20
E2	3.00	—	3.20
L	0.35	0.40	0.45
K	0.20	—	—