HOLT INTEGRATED CIRCUITS INC.

HI-6280

Fully Integrated
MIL-STD-1553 BC/RT/MT

HI-6280, HI-6281, HI-6282, HI-6283 Families

August 2023

DS6280 Rev. New

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1. OVERVIEW

The HI-6280/81/82 family is a fully integrated and dual redundant MIL-STD-1553 BC/RT/MT interface solution which includes 1553 protocol, SRAM and dual transceivers in single ceramic PGA package. The devices are direct pin compatible drop-in replacements for the Data Device Corporation (DDC®) Mini-ACE® and Mini-ACE Plus® Families of MIL-STD-1553 Terminals.

1.1. Bus Controller

The BC greatly reduces the host's processing workload by featuring automatic retries and allowing programmability of frame time, intermessage gap time and response time. In addition, status/error reporting is provided via a flexible interrupt scheme.

1.2. Remote Terminal

The RT has been fully validated by a recognized independent third party. RT memory management options include single, double, and variable-size circular buffer mode for individual subaddresses. The RT performs comprehensive error checking including word and format validation and checks for various transfer errors. The RT supports flexible interrupt conditions, command illegalization and a programmable busy bit by subaddress.

1.3. Monitor Terminal

The family supports three monitor modes including a word monitor mode, a selective message monitor mode and a combined RT/Monitor Mode. For new applications it is recommended to implement the selective message monitor mode. Selective Message Monitor allows monitoring of 1553 messages and provides the ability to filter based on RT address, T/$\overline{R}$ bit and subaddress with no host processor intervention.

1.4. Host Processor Interface

Each device provides an 8/16-bit parallel host bus interface supporting a variety of processor configurations including shared RAM and DMA configurations. The host interface supports both non-multiplexed and multiplexed address/data buses, non-zero wait mode for interfacing to processor address/data buses, and zero wait mode for interfacing to microcontroller I/O ports.

Note: DDC®, Mini-ACE® and Mini-ACE Plus® are registered trademarks of Data Device Corporation, Bohemia, NY, USA. There is no affiliation between Data Device Corporation and Holt Integrated Circuits Inc.

1.5. Features

- Dual Redundant MIL-STD-1553A/B/C Channel
- Optional MIL-STD-1760 boot mode available on select devices (HI-6283 family)
- BC, RT, MT, or RT/MT Modes
- RT only configuration available
- 64Kx17 or 4Kx16 SRAM
- 64Kx17 RAM Devices Have Built-In Parity Check
- External RT Address Inputs
- Generic 8/16-bit Processor Interface
- -40°C to +85°C or -55°C to +125°C
- CPGA-81 Package (HI-628xxCPx devices)
  - 25.4mm x 25.4mm x 3.81mm
- 72-Pin Hermetic Gull Wing Package (HI-628xxCQx devices)
  - 25.4mm x 25.4mm x 3.6mm

1.6. Application Benefits

- Simplified Board Design and Layout
- Third Party RT Validated
- Single Die for Improved Reliability
- Cost Effective Direct Drop-in Replacement for DDC® Mini-ACE® and Mini-ACE Plus® families
- Fully Software Compatible to DDC® ACE, Mini-ACE® and Mini-ACE Plus®

1.7. Cross Reference Guide

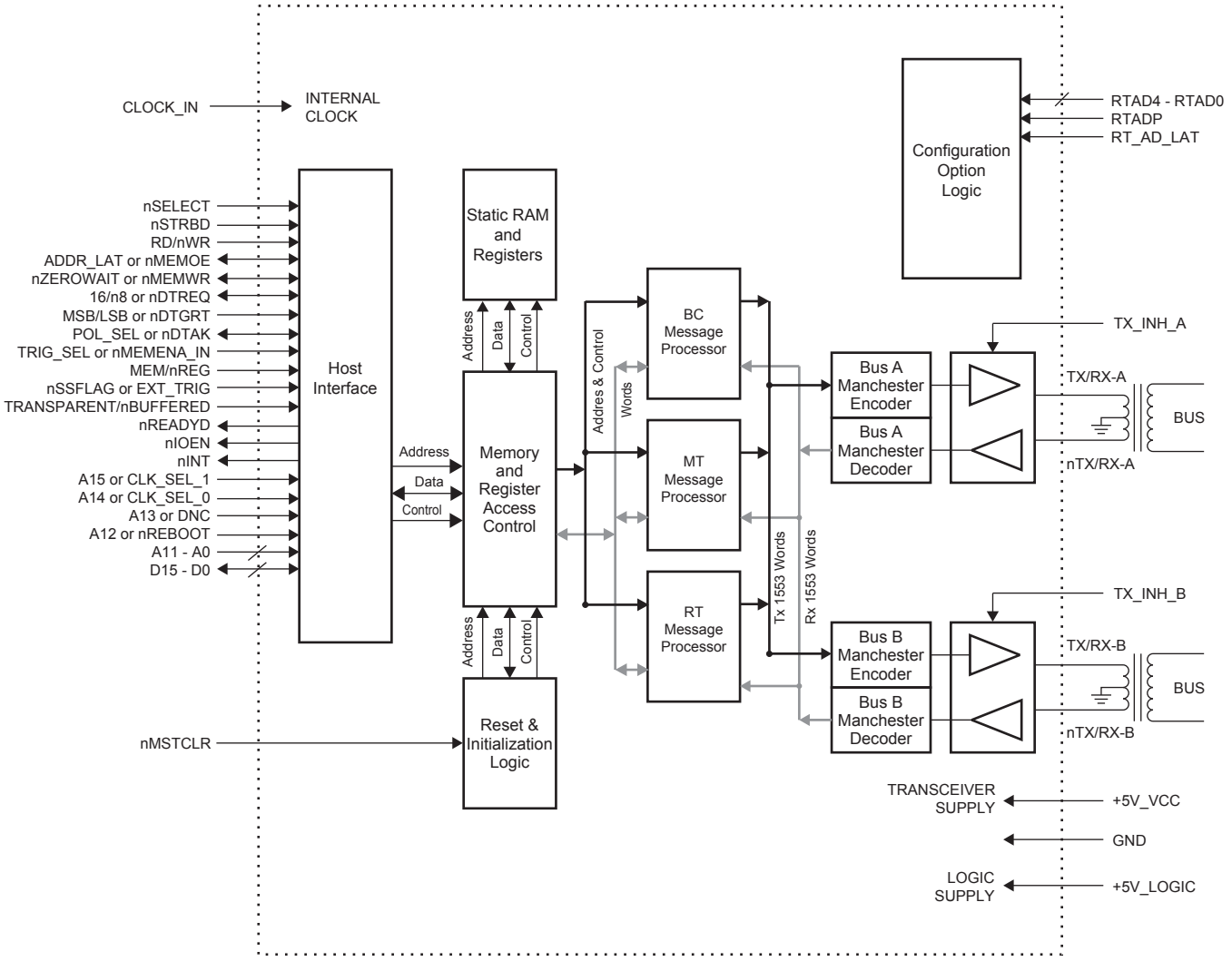
Holt P/N	DDC® P/N
HI-62805CPx	BU-61688P3 (1)
	BU-61689P3 (2)
HI-62815CPx	BU-61588P3 (1)
HI-62820CPx	BU-65178P0 (1)
HI-62825CPx	BU-65178P3 (1)
HI-62835CPx	BU-65179P3 (3)
HI-62805CQx	BU-61688G3 (1)
	BU-61689G3 (2)
HI-62815CQx	BU-61588G3 (1)
HI-62820CQx	BU-65178G0 (1)
HI-62825CQx	BU-65178G3 (1)
HI-62835CQx	BU-65179G3 (3)

Note (1): These device variants have a default clock input frequency (CLOCK_IN) of 16 MHz (same as Holt HI-628xx), but with an option to change the clock frequency to 12 MHz by setting bit 15 in “Configuration Register #5, Read/Write 0x0009”. This clock frequency must be programmed in HI-628xx using bits[1,0] of “Configuration Register #6, Read/Write 0x0018”.

Note (2): These device variants have a default clock input frequency (CLOCK_IN) of 20 MHz, but with an option to change the clock frequency to 10 MHz by setting bit 15 in “Configuration Register #5, Read/Write 0x0009”. Either of these clock frequencies **must** be programmed in HI-628xx (defaults to 16 MHz) using bits[1,0] of “Configuration Register #6, Read/Write 0x0018”.

Note (3): These devices have pin selectable clock input frequencies of 10, 12, 16 and 20 MHz (same as Holt HI-628xx).

1.8. Block Diagram



2. REGISTERS AND COMMAND/STATUS WORDS

Table 1 summarizes the device registers and corresponding addresses.

Table 1. Register Summary

Hex Address	Access	Register Name	Hard Reset Default
0x0000	RD/WR	“Interrupt Enable Register #1, Read/Write 0x0000”	0x0000
0x0001	RD/WR	“Configuration Register #1, Read/Write 0x0001”	0x0000
0x0002	RD/WR	“Configuration Register #2, Read/Write 0x0002”	0x0000
0x0003	RD	“Command Stack Pointer Register, Read Only 0x0003”	0x0000
0x0003	WR	“Start/Reset Register, Write Only 0x0003”	0x0000
0x0004	RD/WR	“BC Control Word Register, Read/Write 0x0004”	0x0000
0x0004	RD/WR	“RT Subaddress Control Word Register, Read/Write 0x0004”	0x0000
0x0005	RD/WR	“Time Tag Register, Read/Write 0x0005”	0x0000
0x0006	RD	“Interrupt Status Register #1, Read Only 0x0006”	0x0000
0x0007	RD/WR	“Configuration Register #3, Read/Write 0x0007”	0x0000
0x0008	RD/WR	“Configuration Register #4, Read/Write 0x0008”	0x0000
0x0009	RD/WR	“Configuration Register #5, Read/Write 0x0009”	0x0000
0x0018	RD/WR	“Configuration Register #6, Read/Write 0x0018”	0x0000
0x000A	RD/WR	“RT/Monitor Data Stack Address Register, Read/Write 0x000A”	0x0000
0x000B	RD	“BC Frame Time Remaining Register, Read Only 0x000B”	0x0000
0x000C	RD	“BC Message Time Remaining Register, Read Only 0x000C”	0x0000
0x000D	RD/WR	“BC Frame Time / RT Last Command / MT Trigger Register, Read/Write 0x000D”	0x0000
0x000E	RD	“RT Status Word Register, Read Only 0x000E”	0x0000
0x000F	RD	“RT BIT Word Register, Read Only 0x000F”	0x0000
0x0010	–	Reserved	0x0000
0x0011	–	Reserved	0x0000
0x0012	–	Reserved	0x0000
0x0013	–	Reserved	0x0000
0x0014	–	Reserved	0x0000
0x0015	–	Reserved	0x0000
0x0016	–	Reserved	0x0000
0x0017	–	Reserved	0x0000

Hex Address	Access	Register Name	Hard Reset Default
0x0019	–	Reserved	0x0000
0x001A	–	Reserved	0x0000
0x001B	–	Reserved	0x0000
0x001C	–	Reserved	0x0000
0x001D	–	Reserved	0x0000
0x001E	–	Reserved	0x0000
0x001F	–	Reserved	0x0000

2.1. Interrupt Enable Register #1, Read/Write 0x0000

Setting a respective bit below to logic “1” will cause an interrupt to be generated when the corresponding event occurs. In enhanced mode, with enhanced interrupts enabled (bit 15 of Configuration Register #2 is set to logic “1”), the equivalent bit in Interrupt Status Register #1 will also be set to logic “1” regardless of whether the enable bit is set or not. Setting a respective bit below to logic “0” will disable (mask) the interrupt.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)		–	0	Reserved
14	RAMPE	R/W	0	Set RAMPE to logic “1” to generate an interrupt when a RAM parity error occurs. Note: RAM PARITY ERROR must be set to logic “0” for 4K RAM device options, since there is no 17-bit RAM for these devices.
13	TXTO	R/W	0	Set TXTO to logic “1” to generate an interrupt when a transmitter timeout occurs.
12	STKRO	R/W	0	Set STKRO to logic “1” to generate an interrupt when a command stack rollover occurs. When in BC Mode, this applies to the BC Command Stack. When in RT Mode, this applies to the RT Command Stack.
11	MTRO	R/W	0	Set MTRO to logic “1” to generate an interrupt when an MT command stack rollover occurs.
10	MTDRO	R/W	0	Set MTDRO to logic “1” to generate an interrupt when an MT data stack rollover occurs.
9	HSKF	R/W	0	Set HSKF to logic “1” to generate an interrupt when a handshake failure occurs between the device and external RAM in Transparent Mode.
8	BCRTY	R/W	0	Set BCRTY to logic “1” to generate an interrupt when the BC tries to re-send a message, regardless of whether the retry was successful or not.
7	RTAPF	R/W	0	Set RTAPF to logic “1” to generate an interrupt when the The Remote Terminal address and parity bits do not exhibit odd parity.
6	TTRO	R/W	0	Set TTRO to logic “1” to generate an interrupt when the time tag counter rolls over.
5	RTCIRO	R/W	0	Set RTCIRO to logic “1” to generate an interrupt when the RT circular buffer rolls over.
4	CWEOM	R/W	0	Set CWEOM to logic “1” to generate an interrupt at the end of the current message provided the EOM interrupt is enabled in the respective BC or RT subaddress control word.
3	BCEOF	R/W	0	Set BCEOF to logic “1” to generate an interrupt at the end of the current BC frame
2	ERR	R/W	0	Set ERR to logic “1” to generate an interrupt when a 1553 Message Error, loopback failure or response timeout is detected

Bit No.	Mnemonic	R/W	Reset	Bit Description	
1	BRMINT	R/W	0	The function of this bit depends on whether the device is operating in BC, RT or MT mode as follows: Set BRMINT to logic “1” to generate an interrupt when the conditions below are met:	
				BC Mode	A received RT Status Word contains the wrong RT address or an unexpected status bit value.
				Enhanced RT Mode	A valid Mode Command is received.
				Word Monitor Mode	A valid received command word matches the value programmed in the Monitor Trigger Register.
0 (LSB)	EOM	R/W	0	Set EOM to logic “1” to generate an interrupt at the end of every message.	

2.2. Configuration Register #1, Read/Write 0x0001

Configuration Register #1 is used to select the device’s mode of operation and for software control of operational features such as RT Status Word bits, Time-Tagging, etc. Specific bit functionality depends on the selected mode of operation as outlined in the Tables below.

Table 2. Configuration Register #1, BC Mode (Enhanced Mode Disabled).

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “0” for BC mode of operation.
14	MODE2	R/W	0	Initializes logic “0” in BC mode.
13	MEMAB	R/W	0	This bit indicates which fixed memory location is used. If MEMAB is logic “0”, Location A is used If MEMAB is logic “1”, Location B is used.
12	ABRTME	R/W	0	Set ABORTME to logic “1” to abort message processing at the end of the current message when the BC encounters a message error. BC Message processing will continue if an optional message retry is successful.
11 − 0	-	R/W	0	Used only in Enhanced BC Mode (see below)

Table 3. Configuration Register #1, BC Mode (Enhanced Mode Enabled).

To enable Enhanced Mode for BC operation, bit 15 of Configuration Register #1 should be set to logic “0” **AND** bit 15 of Configuration Register #3 should be set to logic “1”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “0” for BC mode of operation.
14	MODE2	R/W	0	Initializes logic “0” in BC mode.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	ABRTME	R/W	0	Abort at End of Message if Error. Set to logic “1” to abort message processing at the end of the current message when the BC encounters an error. BC Message processing will continue if the message retry feature is enabled and retry is successful.
11	ABRTFE	R/W	0	Abort at End of Frame if Error. Set to logic “1” to abort message processing at the end of the current frame when the BC encounters an error. BC Message processing will continue if the message retry feature is enabled and retry is successful.
10	ABRTMES	R/W	0	Abort at End of Message if Status Bits Set. Set to logic “1” to abort message processing at the end of the current message when non-masked Status Word bits are set unexpectedly. BC Message processing will continue if the message retry feature is enabled and retry is successful.
9	ABRTFES	R/W	0	Abort at End of Frame if Status Bits Set. Set to logic “1” to abort message processing at the end of the current frame (even if Auto Frame Repeat is enabled) when non-masked Status Word bits are set unexpectedly. BC Message processing will continue if the message retry feature is enabled and retry is successful.
8	AFR	R/W	0	Auto Frame Repeat. Logic “0”: The host manually starts each BC frame. Logic “1”: BC frame will repeat indefinitely provided none of the conditions outlined in bits 12:9 occur or the part is not reset. A fixed frame time may be set by setting bit 6, Internal Trigger below.
7	ETRIG	R/W	0	External Trigger. Set to logic “1” to start BC message processing via rising edge of EXT_TRIG signal.

Bit No.	Mnemonic	R/W	Reset	Bit Description
6	ITRIG	R/W	0	Internal Trigger. This bit is used in conjunction with bit 8, Auto Frame Repeat, to automatically repeat the BC frame with a fixed frame time. The time is set in increments of 100µs (up to 6.55 sec.) according to the value specified by the BC Frame Time Register. Logic “1”: Enable. Logic “0”: Disable. Stop after a single frame.
5	GAPTMR	R/W	0	Message Gap Timer. Logic “0”: Default message gap (~10µs). Logic “1”: The message gap is defined in steps of 1µs in the third word of the BC Message Block Descriptor (the defined value may be 10µs − 65.535 ms)
4	RTY	R/W	0	Message Retry. Logic “1”: Enable BC message retries by setting bit 8 in the respective BC control word. Logic “0”: Disable message retries.
3	RTY2X	R/W	0	If RTY2X is set to logic “1” and retries are enabled by setting bit 4 above, then the BC will retry again if the first attempt was unsuccessful. If RTY2X is set to logic “0”, then retry only once.
2	BCEN	R	0	BC Enabled. Logic “1” indicates the BC state machine is enabled, i.e. is active and processing messages. Logic “0” indicates the BC is in Idle mode.
1	BCFIP	R	0	This bit will read logic “1” for the start of the first message to the end of the last message in a BC frame.
0 (LSB)	BCMIP	R	0	This bit will read logic “1” for the duration of all BC messages.

Table 4. Configuration Register #1, RT Mode (without Alternate Status Word).

Configuration Register #3, bit 5 = logic "0". For Enhanced RT operation, bit 15 of Configuration Register #3 should be set to logic "1".

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic "1" for RT mode of operation.
14	MODE2	R/W	0	If bit 15 is logic "1" for RT operation, this bit should be logic "0". In this case, enable MT mode (i.e. RT/MT) by setting bit 12 of this register.
13	MEMAB	R/W	0	Current Memory Pointer. Logic "0" for Location A, logic "1" for Location B.
12	MTEN	R/W	0	Message Monitor Enable Logic "1": Enable Message Monitor. Logic "0": Disable Message Monitor.
11	DBAC	R/W	0	Dynamic Bus Control Acceptance, active low. Logic "0": The RT will respond to a Dynamic Bus Control Mode Code Command by setting the Dynamic Bus Control Acceptance bit in the RT Status Word. Logic "1": The Dynamic Bus Control Acceptance bit in the RT Status Word will always be zero.
10	BUSY	R/W	0	Busy Bit, active low. Logic "0" will result in "busy" status set. The RT will not respond to commands and will transmit the RT Status Word with the busy bit set. Logic "1" results in the busy bit not set in the RT Status Word and the RT will respond to commands in the normal way.
9	SVCREQ	R/W	0	Service Request Bit, active low. Logic "0" will result in the Service Request bit set in the RT Status Word. Logic "1" will result in the Service Request bit not set in the RT Status Word.
8	SSYS	R/W	0	Subsystem Flag Bit, active low. Logic "0" will result in the Subsystem Flag bit set in the RT Status Word. Logic "1" will result in the Subsystem Flag bit not set in the RT Status Word.
7	TF	R/W	0	Terminal Flag Bit, active low. Enhanced Mode only (Configuration Register #3, bit 15 = logic "1"). Logic "0" will result in the Terminal Flag bit set in the RT Status Word. Logic "1" will result in the Terminal Flag bit not set in the RT Status Word.

Bit No.	Mnemonic	R/W	Reset	Bit Description
6 − 1		-	-	Not used.
0 (LSB)	RTMIP	R	0	RT Message in Progress. Enhanced Mode only (Configuration Register #3, bit 15 = logic “1”). Logic “1” indicates the RT is processing a message. Set just before SOM and reset just after EOM.

Table 5. Configuration Register #1, RT Mode (with Alternate Status Word).

Configuration Register #3, bit 5 = logic “1”. Bits 11 − 1 of the RT status word are programmable directly by the host. For use of the RT Alternate Status word, Enhanced RT operation must be activated (bit 15 of Configuration Register #3 should be set to logic “1”).

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “1” for RT mode of operation.
14	MODE2	R/W	0	Set to logic “0” for RT mode of operation.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	MTEN	R/W	0	Message Monitor Enable Logic “1”: Enable Message Monitor. Logic “0”: Disable Message Monitor.
11	MERR	R/W	0	If this bit is logic “1”, the Message Error bit (bit 9) of the RT Status Word will be set.
10	INS	R/W	0	If this bit is logic “1”, the Instrumentation bit (bit 10) of the RT Status Word will be set.
9	SVCREQ	R/W	0	If this bit is logic “1”, the Service Request bit (bit 11) of the RT Status Word will be set.
8	RSRV1	R/W	0	If this bit is logic “1”, bit 12 of the RT Status Word will be set.
7	RSRV2	R/W	0	If this bit is logic “1”, bit 13 of the RT Status Word will be set.
6	RSRV3	R/W	0	If this bit is logic “1”, bit 14 of the RT Status Word will be set.
5	BCST	R/W	0	If this bit is logic “1”, Broadcast Command Received bit (bit 15) of the RT Status Word will be set.
4	BUSY	R/W	0	If this bit is written logic “1”, the Busy bit (bit 16) of the RT Status Word will be set.
3	SSYS	R/W	0	If this bit is written logic “1”, the Subsystem Flag bit (bit 17) of the RT Status Word will be set.
2	DBAC	R/W	0	If this bit is written logic “1”, bit 18 of the RT Status Word will be set.

Bit No.	Mnemonic	R/W	Reset	Bit Description
1	TF	R/W	0	If this bit is written logic “1”, the Terminal Flag bit (bit 19) of the RT Status Word will be set.
0 (LSB)	RTMIP	R	0	RT Message in Progress. Logic “1” indicates the RT is processing a message. Set just before SOM and reset just after EOM.

Table 6. Configuration Register #1, Enhanced Monitor Mode.

Enhanced mode is activated by setting bit 15 of Configuration Register #3 to logic “1”. Bits 15 − 13 apply to both Enhanced and non-Enhanced Modes. Bits 12 − 0 only apply in Enhanced Mode.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MODE1	R/W	1	Set to logic “0” for MT mode of operation.
14	MODE2	R/W	0	Set to logic “1” for MT mode of operation.
13	MEMAB	R/W	0	Current Memory Pointer. Logic “0” for Location A, logic “1” for Location B.
12	MTEN	R/W	0	Message Monitor Enable Logic “1”: Enable Message Monitor. Logic “0”: Disable Message Monitor.
11	TRIGEN	R/W	0	Word Monitor Trigger Enable. Enable with logic “1”. This bit must be set in Word Monitor Mode to enable a monitor start via EXT_TRIG (bit 7 below set to logic “1”) or via successful comparison between a received valid word and the word stored in the MT Trigger Resister (0x00D).
10	TRSTRT	R/W	0	Start Word Monitor on Trigger. Enable with logic “1”. The Word Monitor will start monitoring following successful comparison between a received valid word and the word stored in the MT Trigger Resister (0x00D).
9	TRSTOP	R/W	0	Stop Word Monitor on Trigger. Enable with logic “1”. The Word Monitor will stop monitoring following successful comparison between a received valid word and the word stored in the MT Trigger Resister (0x00D).
8	-	-	-	Not used.
7	EXTTRIG	R/W	0	External Trigger. Set to logic “1” to start MT via rising edge of EXT_TRIG signal. Monitor trigger must also be enabled by setting bit 11 of this register.
6 − 3	-	-	-	Not used.

Bit No.	Mnemonic	R/W	Reset	Bit Description
2	MEN	R	0	Monitor Enabled. A logic “1” indicates the Monitor is enabled.
1	MTR	R	0	Monitor Triggered. A logic “1” indicates the Monitor was triggered either by successful comparison with the word in the MT Trigger Resister (0x00D) or via rising edge of the EXT_TRIG signal..
0 (LSB)	MACT	R	0	Monitor Active. A logic “1” indicates the Word Monitor was started.

2.3. Configuration Register #2, Read/Write 0x0002

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td>15 (MSB)</td><td>EINTEN</td><td>R/W</td><td>0</td><td>Set EINTEN to logic “1” to enable Enhanced Interrupts.</td></tr>
<tr><td>14</td><td>RAMP</td><td>R/W</td><td>0</td><td>Set RAMP to logic “1” to enable parity checking in the internal RAM.</td></tr>
<tr><td>13</td><td>BUSYLU</td><td>R/W</td><td>0</td><td>Set BUSYLU to logic “1” to enable the Busy Lookup Table.</td></tr>
<tr><td>12</td><td>DBUF</td><td>R/W</td><td>0</td><td>Set DBUF to logic “1” to enable Double Buffering for Rx messages (see bit 1 below).</td></tr>
<tr><td>11</td><td>OVINV</td><td>R/W</td><td>0</td><td>Setting OVINV to logic “1” will cause invalid circular buffer data to be overwritten.</td></tr>
<tr><td>10</td><td>256RO</td><td>R/W</td><td>0</td><td>If 256RO is logic “0”, RAM buffers will rollover after 256 words.</td></tr>
<tr><td>9 − 7</td><td>TTRES</td><td>R/W</td><td>0</td><td>Time Tag Resolution bits. Bits 9 − 7 set the time tag resolution as follows:
<table>
<tr><th>Bit 9</th><th>Bit 8</th><th>Bit 7</th><th>Time Tag Resolution</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>64 µs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>32 µs</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16 µs</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>8 µs</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>4 µs</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>2 µs</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>The Time Tag is incremented by writing logic “1” to bit 4 of the Start/Reset Register.</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>The Time Tag is incremented by means of an external clock connected to TAG_CLK.</td></tr>
</table></td></tr>
<tr><td>6</td><td>TTSYNC</td><td>R/W</td><td>0</td><td>In RT Mode, setting this bit to logic “1” will clear the Time Tag counter when a Synchronize Without Data mode command is received.</td></tr>
<tr><td>5</td><td>SYNCDAT</td><td>R/W</td><td>0</td><td>In RT Mode, setting this bit to logic “1” will cause the data word in a received Synchronize With Data mode command to loaded into the Time Tag Register.
In BC Mode, setting this bit to logic “1” will allow the value of the Time Tag Register to be transmitted as the data word in a Synchronize With Data mode command.</td></tr>
<tr><td>4</td><td>CLRSTAT</td><td>R/W</td><td>0</td><td>Logic “1”: Clear Interrupt Status Registers #1 or #2 when read respectively.
Logic “0”: Clear both Interrupt Status Registers #1 and #2 by writing logic “1” to bit 2, Start/Reset Register 0x003.</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
3	LEVEL	R/W	0	This bit sets whether the interrupt output signal INT is a continuous level or a pulse. Logic “1”: The $\overline{\text{INT}}$ output signal will be a level that will remain low until Interrupt Status Registers #1 and #2 are cleared. Logic “0”: The $\overline{\text{INT}}$ output signal will be a 500ns pulse.
2	SRREQ	R/W	0	Logic “0”: The Service Request bit in the RT Status Word may **only** be controlled by the host. Logic “1”: The Service Request bit in the RT Status Word may be controlled by the host, but is cleared when the RT responds to a Transmit Vector Word mode code command
1	ENRTBUF	R/W	0	This bit is used to set the Enhanced RT buffering mode. ENRTBUF = logic “0”: If bit 12 of this register is logic “1”, double buffer mode will be set globally for all Rx commands. If bit 12 is logic “0”, single buffer mode will be set. ENRTBUF = logic “1”: Each Rx subaddress can have a different buffering mode, set by the individual subaddress control word.
0 (LSB)	NOTICE2	R/W	0	Notice 2 Broadcast Data Storage. If this bit is logic “1”, the terminal stores data associated with broadcast commands separately from data associated with non-broadcast commands to meet the requirements of MIL-STD-1553B Notice 2. If this bit is logic “0”, broadcast command data is stored in the same buffer with data from nonbroadcast commands.

2.4. Command Stack Pointer Register, Read Only 0x0003

When read, this register contains the current value of the Stack Pointer for RT, MT and BC modes.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	Command Stack Pointer, bits[15 − 0] respectively.

2.5. Start/Reset Register, Write Only 0x0003

When writing to this register, all reserved bits must be written logic “0”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB) − 7	−	W	0	Reserved.
6	STOPMSG	W	0	In BC Mode, setting this bit will stop operation at End-of-Message. In MT Mode, setting this bit will stop message monitoring.
5	BCSTOPFR	W	0	In BC Mode, setting this bit will stop operation at End-of-Frame.
4	TTINC	W	0	Setting this bit will increment the Time Tag Counter by “1” LSB when Time Tag Resolution bits 9-7 of Configuration Register #2 are set to “110”.
3	TTRST	W	0	Setting TTRST to logic “1” will reset the Time Tag Counter.
2	INTRST	W	0	Setting this bit will clear Interrupt Status Registers #1 and #2.
1	BCMTSTRT	W	0	In BC Mode, setting this bit will start the BC. In MT Mode, setting this bit will start the MT.
0 (LSB)	SFTRESET	W	0	Setting this bit will initiate a software reset.

2.6. BC Control Word Register, Read/Write 0x0004

The BC Control Word is the first word in each Message Control / Status Block. The BC Control Word is not transmitted on the MIL-STD-1553 bus. This word is initialized and maintained by the host to specify message attributes such as bit masks for the received RT Status Word, which bus to use, BC message format, etc.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	−	W	0	Reserved.
14	MEMASK	R/W	0	Message Error Bit Mask. If MEMASK bit is logic “0” and the Message Error bit is logic 1 in the received RT Status Word, the BC will recognise the Message Error status. If MEMASK bit is logic “1”, the Message Error bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
13	SRQMASK	R/W	0	Service Request Bit Mask. If SRQMASK bit is logic “0” and the Service Request bit is logic 1 in the received RT Status Word, the BC will recognise the Service Request status. If SRQMASK bit is logic “1”, the Service Request bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
12	BSYMASK	R/W	0	Busy Bit Mask. If BSYMASK bit is logic “0” and the Busy bit is logic 1 in the received RT Status Word, the BC will recognise the Busy status. If BSYMASK bit is logic “1”, the Busy bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
11	SSYSMASK	R/W	0	Subsystem Flag Bit Mask. If SSYSMASK bit is logic “0” and the Subsystem Flag bit is logic 1 in the received RT Status Word, the BC will recognise the Subsystem Flag status. If SSYSMASK bit is logic “1”, the Subsystem Flag bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
10	TFMASK	R/W	0	Terminal Flag Bit Mask. If TFMASK bit is logic “0” and the Terminal Flag bit is logic 1 in the received RT Status Word, the BC will recognise the Terminal Flag status. If TFMASK bit is logic “1”, the Terminal Flag bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.

Bit No.	Mnemonic	R/W	Reset	Bit Description
9	RSVMASK	R/W	0	Reserved Bits Mask. If RSVMASK bit is logic “0” and one or more of the three Reserved bits is logic “1” in the received RT Status Word, the BC will recognise the Reserved status. If RSVMASK bit is logic “1”, the Reserved bits in the received RT Status Word are masked and are treated by the BC as “Don’t Care”.
8	RTRYENA	R/W	0	Retry Enabled. If RTRYENA is set to logic “1”, failed messages will be retried according to Configuration Register settings.
7	USEBUSA	R/W	0	Use Bus A/$\overline{B}$. If this Control Word bit is logic “1”, the BC transmits the command on Bus A. If this Control Word bit is logic “0”, the BC transmits the command on Bus B.
6	SELFTST	R/W	0	Self-Test Message Off-Line. If SELFTST is logic “1”, an internal loopback test (bus transmission disabled) is performed.
5	MASKBCR	R/W	0	Mask Broadcast Command Received Bit. If MASKBCR bit is logic “0” and the Broadcast Command Received bit is logic “1” in the received RT Status Word, the BC will recognise the Broadcast status. If MASKBCR bit is logic “1”, the Broadcast Command Received bit in the received RT Status Word is masked and is treated by the BC as “Don’t Care”.
4	EOMINT	R/W	0	End of Message Interrupt. If EOMINT is logic “1”, an interrupt request will be generated (if not masked in Interrupt Enable Register #1) upon message completion.
3	1553AB	R/W	0	1553A/B Select. If 1553AB is Logic “1”, RT response will comply with MIL-STD-1553A. If 1553AB is Logic “0”, RT response will comply with MIL-STD-1553B.

Bit No.	Mnemonic	R/W	Reset	Bit Description			
2 − 0 (LSB)	BCMSGFT	R/W	0	BC Message Format. The BC Message format is defined by these three bits as follows:			
				Bit 2	**Bit 1**	**Bit 0**	**BC Message Format**
				0	0	0	BC-to-RT
				0	0	1	RT-to-RT
				0	1	0	Broadcast
				0	1	1	Broadcast RT-to-RTs
				1	0	0	Mode Code
				1	0	1	Not Used
				1	1	0	Broadcast Mode Code
				1	1	1	Not Used

2.7. RT Subaddress Control Word Register, Read/Write 0x0004

This register enables the buffering mechanism for transmit, receive and broadcast subaddresses, either globally or for individual subaddresses (via the subaddress control word lookup table). It is Read-Only when the RT is active and reads back the value of the last received control word. It may be written for test purposes when the RT is Idle.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	DBGB	R/W	0	If this bit is logic “0” then circular or single message buffering will be enabled for individual subaddresses (see MEMx bits below). If this bit is logic “1”, then double buffering will be enabled for individual subaddresses. Note, DBUF bit 12 of Configuration Register #2 should be also be set. For individual subaddress buffering, enhanced RT buffering must be enabled (set ENRTBUF bit 1 of Configuration Register #2). Combinations of the MEMx bits below set the size of the buffer. To enable double buffering, DBUF bit 12 of Configuration Register #2 should be set. To enable circular buffering, CIRCEN bit 12 of Configuration Register #6 should be set. **Note:** This bit is ignored for Tx subaddresses.
14	TXEOM	R/W	0	TXEOM = logic “1” enables an interrupt to be generated when the end of a message occurs for a transmit subaddress.
13	TXCIR	R/W	0	TXCIR = logic “1” enables an interrupt to be generated when a transmit subaddress circular buffer rolls over.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td rowspan="10">12 − 10</td><td rowspan="10">TXMEM[2:0]</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td>These bits set the buffer type and size for transmit subaddress buffering as follows:
<table>
<tr><th>TXMEM2 bit 12</th><th>TXMEM1 bit 11</th><th>TXMEM0 bit 10</th><th>Buffering Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Individual Tx subaddress single message buffering</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Individual Tx subaddress circular buffering, 128 Words</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Individual Tx subaddress circular buffering, 256 Words</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Individual Tx subaddress circular buffering, 512 Words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Individual TX subaddress circular buffering, 1024 Words</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Individual TX subaddress circular buffering, 2048 Words</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Individual Tx subaddress circular buffering, 4096 Words</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Individual Tx subaddress circular buffering, 8192 Words</td></tr>
</table></td></tr>
<tr><td>9</td><td>RXEOM</td><td>R/W</td><td>0</td><td>RXEOM = logic “1” enables an interrupt to be generated when the end of a message occurs for a receive subaddress.</td></tr>
<tr><td>8</td><td>RXCIR</td><td>R/W</td><td>0</td><td>RXCIR = logic “1” enables an interrupt to be generated when a receive subaddress circular buffer rolls over.</td></tr>
</table>

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="5">Bit Description</th></tr>
<tr><td rowspan="11">7 – 5</td><td rowspan="11">RXMEM[2:0]</td><td rowspan="11">R/W</td><td rowspan="11">0</td><td colspan="5">These bits set the buffer type and size for receive subaddress buffering as follows:</td></tr>
<tr><td>DBGB bit 15</td><td>RXMEM2 bit 7</td><td>RXMEM1 bit 6</td><td>RXMEM0 bit 5</td><td>Buffering Mode</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Individual Rx subaddress single message buffering</td></tr>
<tr><td>X</td><td>0</td><td>0</td><td>1</td><td>Individual Rx subaddress circular buffering, 128 Words</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>0</td><td>Individual Rx subaddress circular buffering, 256 Words</td></tr>
<tr><td>X</td><td>0</td><td>1</td><td>1</td><td>Individual Rx subaddress circular buffering, 512 Words</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>0</td><td>Individual RX subaddress circular buffering, 1024 Words</td></tr>
<tr><td>X</td><td>1</td><td>0</td><td>1</td><td>Individual RX subaddress circular buffering, 2048 Words</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>0</td><td>Individual Rx subaddress circular buffering, 4096 Words</td></tr>
<tr><td>X</td><td>1</td><td>1</td><td>1</td><td>Individual Rx subaddress circular buffering, 8192 Words</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Double buffering for individual Rx subaddresses.</td></tr>
<tr><td>4</td><td>BCSTEOM</td><td>R/W</td><td>0</td><td colspan="5">BCSTEOM = logic “1” enables an interrupt to be generated when the end of a message occurs for a broadcast subaddress.</td></tr>
<tr><td>3</td><td>BCSTCIR</td><td>R/W</td><td>0</td><td colspan="5">BCSTCIR = logic “1” enables an interrupt to be generated when a broadcast subaddress circular buffer rolls over.</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description				
2 − 0	BCSTMEM[2:0]	R/W	0	These bits set the buffer type and size for broadcast subaddress buffering as follows:				
				DBGB bit 15	**BCSTMEM2 bit 2**	**BCSTMEM1 bit 1**	**BCSTMEM0 bit 0**	**Buffering Mode**
				0	0	0	0	Individual BCST subaddress single message buffering
				X	0	0	1	Individual BCST subaddress circular buffering, 128 Words
				X	0	1	0	Individual BCST subaddress circular buffering, 256 Words
				X	0	1	1	Individual BCST subaddress circular buffering, 512 Words
				X	1	0	0	Individual BCST subaddress circular buffering, 1024 Words
				X	1	0	1	Individual BCST subaddress circular buffering, 2048 Words
				X	1	1	0	Individual BCST subaddress circular buffering, 4096 Words
				X	1	1	1	Individual BCST subaddress circular buffering, 8192 Words
				1	0	0	0	Double buffering for individual BCST subaddresses.

2.8. Time Tag Register, Read/Write 0x0005

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	This register contains the current value of the time tag counter. The resolution of the Time Tag (in µs/LSB) is programmable through bits 9 − 7 of Configuration Register #2.

2.9. Interrupt Status Register #1, Read Only 0x0006

When enhanced interrupts are enabled (bit 15 of Configuration Register #2 set to logic “1”), the bits in this register will be set when the respective event occurs, regardless of whether the interrupt is enabled (equivalent bit set in the Interrupt Enable Register #1) or not.

If enhanced interrupts are not enabled (bit 15 of Configuration Register #2 is logic “0”), the bits in this register will only be set if the interrupt is enabled (equivalent bit set in the Interrupt Enable Register #1).

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	MINT	R	0	This bit only applies when Enhanced Interrupts are enabled by setting bit 15 of Configuration Register #2. MINT will be set to logic “1” if an interrupt request has been generated on the $\overline{\text{INT}}$ output signal.
14	RAMPE	R	0	RAMPE will be set to logic “1” when a RAM parity error occurs.
13	TXTO	R	0	TXTO will be set to logic “1” when a transmitter timeout occurs.
12	STKRO	R	0	STKRO will be set to logic “1” when a command stack rollover occurs. When in BC Mode, this applies to the BC Command Stack. When in RT Mode, this applies to the RT Command Stack.
11	MTRO	R	0	MTRO will be set to logic “1” when an MT command stack rollover occurs.
10	MTDRO	R	0	MTDRO will be set to logic “1” when an MT data stack rollover occurs.
9	HSKF	R	0	HSKF will be set to logic “1” when a handshake failure occurs between the device and external RAM in Transparent Mode.
8	BCRTY	R	0	BCRTY will be set to logic “1” when the BC tries to re-send a message, regardless of whether the retry was successful or not.
7	RTAPF	R	0	RTAPF will be set to logic “1” when the RT address and parity bits do not exhibit odd parity.
6	TTRO	R	0	TTRO will be set to logic “1” when the time tag counter rolls over.
5	RTCIRRO	R	0	RTCIRRO will be set to logic “1” when the RT circular buffer rolls over.
4	CWEOM	R	0	CWEOM will be set to logic “1” at the end of the current message provided the EOM interrupt is enabled in the respective BC or RT subaddress control word.
3	BCEOF	R	0	BCEOF will be set to logic “1” at the end of the current BC frame

Bit No.	Mnemonic	R/W	Reset	Bit Description	
2	ERR	R	0	ERR will be set to logic “1” when a 1553 Message Error, loopback failure or response timeout is detected	
1	BRMINT	R/W	0	The function of this bit depends on whether the device is operating in BC, RT or MT mode as follows: BRMINT will be set to logic “1” when the conditions below are met:	
				BC Mode	A received RT Status Word contains the wrong RT address or an unexpected status bit value.
				Enhanced RT Mode	A valid Mode Command is received.
				Word Monitor Mode	A valid received command word matches the value programmed in the Monitor Trigger Register.
0 (LSB)	EOM	R/W	0	EOM will be set to logic “1” at the end of every message.	

2.10. Configuration Register #3, Read/Write 0x0007

Bit No.	Mnemonic	R/W	Reset	Bit Description		
15 (MSB)	ENHANC	R/W	0	Set ENHANC to logic “1”, to enable Enhanced Mode operation.		
14 − 13	BCRTSTK[1:0]	R/W	0	The BCRTSTK[1:0] bits set the size of the BC (BC Mode) or RT (RT Mode) command stack size as follows:		
				BCRTSTK 1	**BCRTSTK 0**	**BC OR RT Command Stack Size**
				0	0	256 words (64 messages)
				0	1	512 words (128 messages)
				1	0	1024 words (256 messages)
				1	1	2048 words (512 messages)
12 − 11	MTSTK[1:0]	R/W	0	The MTSTK[1:0] bits set the size of the MT command stack size as follows:		
				MTSTK 1	**MTSTK 0**	**MT Command Stack Size**
				0	0	256 words (64 messages)
				0	1	1024 words (256 messages)
				1	0	4096 words (1024 messages)
				1	1	16384 words (4096 messages)

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td rowspan="10">10 − 8</td><td rowspan="10">MTDATA[2:0]</td><td rowspan="10">R/W</td><td rowspan="10">0</td><td>The MTDATA[2:0] bits set the size of the MT data stack size as follows:
<table><tr><th>MTSTK 2</th><th>MTSTK 1</th><th>MTSTK 0</th><th>MT Data Stack Size</th></tr><tr><td>0</td><td>0</td><td>0</td><td>65,536 words</td></tr><tr><td>0</td><td>0</td><td>1</td><td>32,768 words</td></tr><tr><td>0</td><td>1</td><td>0</td><td>16,384 words</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8,192 words</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4,096 words</td></tr><tr><td>1</td><td>0</td><td>1</td><td>2,048 words</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1,024 words</td></tr><tr><td>1</td><td>1</td><td>1</td><td>512 words</td></tr></table></td></tr>
<tr><td>7</td><td>ILLOFF</td><td>R/W</td><td>0</td><td>If ILLOFF bit is logic “0”, Command Illegalization is enabled.
If ILLOFF bit is logic “1”, Command Illegalization is disabled and the Illegalizaton Table memory space may be used for data storage. .</td></tr>
<tr><td>6</td><td>MCRSVME</td><td>R/W</td><td>0</td><td>The MCRSVME decides how the RT responds to a received reserved mode command:
Logic “0”: RT doesn’t respond to reserved mode commands. Message Error bit is set.
Logic “1”: RT will respond to reserved mode commands. Message Error bit is not set.</td></tr>
<tr><td>5</td><td>ALTSTAT</td><td>R/W</td><td>0</td><td>Setting ALTSTAT to logic “1” enables the Alternate RT Status Word as follows:
Logic “1”: All RT Status Word response bits may be controlled directly by the Host by setting their respective bits 11 − 1 in Configuration Register #1.
Logic “0”: The Alternate RT Status Word is disabled and only the Dynamic Bus Control Acceptance bit, Busy bit, Service Request bit, Subsystem Flag bit and Terminal Flag bits are programmable by the Host by setting their respective bits 11 − 7 in Configuration Register #1.</td></tr>
<tr><td>4</td><td>NOILLRX</td><td>R/W</td><td>0</td><td>If NOILLRX is set to logic “1”, illegal command data words received by the RT are not stored in RAM.
If NOILLRX is set to logic “0”, illegal command data words received by the RT are stored in RAM.</td></tr>
<tr><td>3</td><td>NOBUSYRX</td><td>R/W</td><td>0</td><td>If NOBUSYRX is set to logic “1”, the RT responds “Busy status” with the BUSY bit set, but does not store the received data words in RAM.
If NOBUSYRX is set to logic “0”, the RT responds “Busy status” with the BUSY bit set and stores the received data words in RAM.</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
2	RTTFF	R/W	0	Active low. If RTTFF is logic “1” the Terminal Flag bit in the RT status word will be automatically set following a transmitter timeout or loopback failure and control of the Terminal Flag bit is not accessable to the host. If RTTFF is logic “0” the Terminal Flag bit in the RT status word will be automatically set following a transmitter timeout or loopback failure **and** the Terminal Flag bit is also programmable by the host.
1	1553A	R/W	0	If 1553A is set to logic “1”, Mode Codes are processed according to MIL-STD-1553A. If 1553A is set to logic “0”, Mode Codes are processed according to MIL-STD-1553B.
0 (LSB)	ENHMC	R/W	0	If ENHMC is set to logic “1”, enhanced features are enabled for mode command processing. Mode code data words may be stored separately according to whether they are receive, transmit or broadcast and interrupts may be enables for individual mode codes. If ENHMC is set to logic “0”, all mode code data is stored in the same location in RAM.

2.11. Configuration Register #4, Read/Write 0x0008

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	BITW	R/W	0	If BITW is set to logic “0” the RT will respond to a Transmit BIT word mode command with the data word stored in the internal BIT Word Register. If BITW is set to logic “1” the RT will respond to a Transmit BIT word mode command with the data word stored by the host in RAM location 0x0123.
14	INBITW	R/W	0	Setting INBITW to logic “1” will inhibit transmission of the BIT word (in response to a Transmit BIT word mode command) if the Busy bit is set. The RT will respond with the Busy bit set in the RT Status word but no BIT word will be transmitted. If INBITW is logic “0”, the BIT word will be transmitted (in response to a Transmit BIT word mode command), following transmission of the RT Status word with the Busy bit set.
13	MCBUSY	R/W	0	This bit affects RT response to Transmit Vector Word or the Reserved Mode Commands 22 to 31 (decimal) when the busy bit is set. If MCBUSY is logic “1” the RT will respond to the above mode commands with the busy bit set in the RT Status Word, followed by a data word. If MCBUSY is logic “0”, no data word will be transmitted,

Bit No.	Mnemonic	R/W	Reset	Bit Description
12	EBCCW	R/W	0	In BC Mode, setting EBCCW to logic “1” enables all bits of the Expanded BC Control Word. In BC Mode, if EBCCW is logic “0” or if ENHANC bit 15 in Configuration Register #3 is logic “0”, then only bits 7, 6, 5, 2, 1, and 0 in the BC Control Word are enabled.
11	BCSTMEN	R/W	0	In BC Mode, if BCSTMEN is logic “1”, the function of the MASKBCR bit in the BC Control Word is enabled, i.e. if BCSTMEN is logic “1” and MASKBCR bit is logic “0”, the BC will recognise Broadcast status if the Broadcast Command Received bit is logic “1” in the received RT Status Word. If MASKBCR bit is logic “1”, the Broadcast Bit in the received RT Status Word is “Don’t Care”. In BC Mode, if BCSTMEN is logic “0”, the value of the MASKBCR bit in the BC Control Word is XORed with the Broadcast bit in the received RT Status Word.
10	RTY1553A	R/W	0	Setting this bit to logic “1” will cause the BC to try to resend a message in 1553A mode when the Message Error bit in the received RT Status word is set. This is in addition to the normal criteria for retrying failed messages, provided retries are enabled (e.g. response timeout, etc.).
9	RTYSTAT	R/W	0	If RTYSTAT is logic “0”, the BC will not retry to send a message in response to a received RT Status Word bit being set. If RTYSTAT is logic “1”, the BC will retry to send a message in response to a received RT Status Word bit being set, provided retries are enabled.
8	RTY1ALT	R/W	0	If this bit is set to logic “0”, the first retry will be on the same bus as the original failed message. If this bit is set to logic “1”, the first retry will be on the opposite bus from the original failed message.
7	RTY2ALT	R/W	0	If this bit is set to logic “0”, the second retry will be on the same bus as the original failed message. If this bit is set to logic “1”, the second retry will be on the opposite bus from the original failed message. Note that the second retry option must be enabled by setting RTY2X, bit 3 of Configuration Register #1.
6	MERVAL	R/W	0	When an RT responds to a valid message with the Message Error bit set in the status word, the requested number of data words must follow the status word in order for the response to be valid. Setting MERVAL to logic “1” allows the message to be also valid if the status word is followed by no data words (e.g. illegal command).
5	BUSYVAL	R/W	0	When an RT responds to a valid message with the Busy bit set in the status word, the requested number of data words must follow the status word in order for the response to be valid. Setting BUSYVAL to logic “1” allows the message to be also valid if the status word is followed with no data words.

Bit No.	Mnemonic	R/W	Reset	Bit Description
4	MTGAP	R/W	0	When in MT mode, this bit allows an additional 20µs to be added to the gap time of consecutive messages when the second message is received on the alternate bus. Logic “0”: Add 20µs to gap time, even if messages overlap. Logic “1”: Gap time will remain unchanged.
3	RTLATEN	R/W	0	When set to logic “1”, RTLATEN enables latching of the RT address and parity, provided the input signal RT_AD_LAT is also logic “1”. When RTLATEN is logic “0”, the RT address and parity will not be latched.
2 − 0 (LSB)	Reserved	R/W	0	These bits are reserved and must all remain logic “0”.

2.12. Configuration Register #5, Read/Write 0x0009

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td>15 (MSB)</td><td>CLKSEL</td><td>R</td><td>0</td><td>This Read-Only bit simply returns the value of bit 0, Configuration Register #6 (CLKSEL0).</td></tr>
<tr><td>14</td><td>SNGLEND</td><td>R</td><td>0</td><td>This bit will always return logic “0” when read.</td></tr>
<tr><td>13</td><td>TXINHA</td><td>R</td><td>0</td><td>TXINHA will be logic “1” when the TX_INH_A input signal is logic “1”, indicating that transmission on Bus A has been inhibited.</td></tr>
<tr><td>12</td><td>TXINHB</td><td>R</td><td>0</td><td>TXINHB will be logic “1” when the TX_INH_B input signal is logic “1”, indicating that transmission on Bus B has been inhibited.</td></tr>
<tr><td>11</td><td>ZEROXEN</td><td>R/W</td><td>0</td><td>Setting ZEROXEN to logic “0” will cause the decoder to sample both edges of the clock input.</td></tr>
<tr><td>10 − 9</td><td>RTRTTO[1:0]</td><td>R/W</td><td>0</td><td>These two bits set the device RT-to-RT response timeout as follows:
<table>
<tr><th>RTRTTO1</th><th>RTRTTO0</th><th>RT-to-RT Response Timeout</th></tr>
<tr><td>0</td><td>0</td><td>18.5 µs</td></tr>
<tr><td>0</td><td>1</td><td>22.5 µs</td></tr>
<tr><td>1</td><td>0</td><td>50.5 µs</td></tr>
<tr><td>1</td><td>1</td><td>130 µs</td></tr>
</table></td></tr>
<tr><td>8</td><td>GTEN</td><td>R/W</td><td>0</td><td>If GTEN is set to logic “0”, the device will not check for a minimum gap time between messages.
If GTEN is set to logic “1”, the device will check for a minimum gap time between messages of 2µs. Violating this minimum time will result in the message being invalid.</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
7	BCSTDIS	R/W	0	If BCSTDIS is set to logic “1”, the device will not recognise sub-address 31 as a Broadcast Command. If BCSTDIS is set to logic “0”, the device will recognise subad-dress 31 as a Broadcast Command.
6	RTADLAT	R	0	This bit reflects the state of the RT_AD_LAT input signal. See the section Signal Descriptions.
5 − 0 (LSB)	RTAD[4:0] RTADP (LSB)	R/W	0	Writing these lower 6 bits provides a mechanism to set the RT Address and Parity bit (LSB) via software. See RT_AD_LAT input signal description in section Signal Descriptions.

2.13. Configuration Register #6, Read/Write 0x0018

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th colspan="3">Bit Description</th></tr>
<tr><td>15 (MSB) − 2</td><td>-</td><td>R/W</td><td>0</td><td colspan="3">Reserved.</td></tr>
<tr><td rowspan="5">1 − 0 (LSB)</td><td rowspan="5">CLKSEL[1:0]</td><td rowspan="5">R/W</td><td rowspan="5">0</td><td colspan="3">These two bits select the Clock Frequency according to the table below.</td></tr>
<tr><th>CLKSEL1</th><th>CLKSEL0</th><th>Clock Frequency (MHz)</th></tr>
<tr><td>0</td><td>0</td><td>16</td></tr>
<tr><td>0</td><td>1</td><td>12</td></tr>
<tr><td>1</td><td>0</td><td>20</td></tr>
<tr><td>1</td><td>1</td><td>10</td></tr>
</table>

2.14. RT/Monitor Data Stack Address Register, Read/Write 0x000A

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	This register contains the current value of the Data Stack pointer, either RT Data stack or Word Monitor Data Stack, depending on the mode of operation.

2.15. BC Frame Time Remaining Register, Read Only 0x000B

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	In BC Mode, this register contains the value of the time remaining in the BC frame. The resolution is 100ms/LSB, with a maximum value of 6.55ms.

2.16. BC Message Time Remaining Register, Read Only 0x000C

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	In BC Mode, this register contains the current value of the time-to-next message timer. The resolution is 1µs/LSB, with a maximum value of 65.535ms.

2.17. BC Frame Time / RT Last Command / MT Trigger Register, Read/Write 0x000D

<table>
<tr><th>Bit No.</th><th>R/W</th><th>Reset</th><th colspan="2">Bit Description</th></tr>
<tr><td rowspan="5">15 (MSB) − 0 (LSB)</td><td rowspan="5">R/W</td><td rowspan="5">0</td><td colspan="2">The value of this register depends of the mode of operation as follows:</td></tr>
<tr><td>Mode of Operation</td><td>Register Function</td></tr>
<tr><td>BC</td><td>Used to program the BC frame time</td></tr>
<tr><td>RT</td><td>Used to store the last command processed by the RT.</td></tr>
<tr><td>Word Monitor</td><td>Used to store the value of the word which will initiate a monitor start if a valid received word matches it.</td></tr>
</table>

2.18. RT Status Word Register, Read Only 0x000E

This register contains the current value of the device RT Status Word. This includes the Alternate RT Status Word, where all lower 11 bits are all programmable by the host.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 11	R	0	Logic “0”
10	R	0	Message Error Status Bit
9	R	0	Instrumentation Status Bit
8	R	0	Service Request Status Bit
7 − 5	R	0	Reserved bits
4	R	0	Broadcast Command Received Status Bit
3	R	0	Busy Status Bit
2	R	0	Subsystem Flag Status Bit
1	R	0	Dynamic Bus Control Acceptance Status Bit
0 (LSB)	R	0	Terminal Flag Status Bit

2.19. RT BIT Word Register, Read Only 0x000F

This register’s bits will read logic “1” to reflect errors flagged by the device. The content of this register will be transmitted to the BC following a “Transmit BIT Word” mode command. It may also be read by the host.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	TXTO	R	0	Transmitter Timed Out. The transmitter timeout of 668µs was exceeded.
14	LBFB	R	0	Loopback Test Failure B. A loopback failure occurred on Bus B.
13	LBFA	R	0	Loopback Test Failure A. A loopback failure occurred on Bus A.
12	HSF	R	0	Transparent Mode Handshake Failure.
11	TXSDB	R	0	Transmitter Shutdown B. A Transmitter Shutdown mode command was received on Bus A. This mode command shuts down the transmitter of the inactive bus.
10	TXSDA	R	0	Transmitter Shutdown A. A Transmitter Shutdown mode command was received on Bus B. This mode command shuts down the transmitter of the inactive bus.
9	TFINH	R	0	Terminal Flag Inhibited. An Inhibit Terminal Flag mode command was received.

Bit No.	Mnemonic	R/W	Reset	Bit Description
8	BUSAB	R	0	If BUSAB = logic “0”, the previous message was received on Bus A. If BUSAB = logic “1”, the previous message was received on Bus B.
7	DWCH	R	0	Data Word Count High. The number of data words received in the last message was higher than expected.
6	DWCL	R	0	Data Word Count Low. The number of data words received in the last message was lower than expected.
5	SNYCF	R	0	Incorrect Sync Received. A command sync bit was detected in a data word.
4	INVW	R	0	Invalid Word Received
3	RTRTE	R	0	RT−to−RT Gap / Sync / Address Error. If the device is the receiving RT in an RT-to-RT transfer, this bit will be set if there is a gap time error (gap less than 2µs), incorrect sync or format error, or incorrect RT address.
2	RTRTTO	R	0	RT−to−RT Timeout Error. This bit will be set if the allowed RT-to-RT response time is exceeded. The RT-to-RT response timeout is programmed by setting the RTRT-TO[1:0] bits [10:9] in Configuration Register #5.
1	RTRTCWE	R	0	RT−to−RT Command Word Error . If the device is the receiving RT in an RT-to-RT transfer, this bit will be set if there is an error in the Transmit Command Word, e.g. T/$\overline{R}$ bit is not logic “1”.
0 (LSB)	RXCWE	R	0	Received Command Word Error. This bit will be set if there is an error in a received Command Word

2.20. BC Block Status Word

The Block Status Word in the Message Control / Status Block provides information regarding message status (in process or completed), the bus it was transmitted on, whether errors occurred during the message, and the type of occurring errors. This word is written into RAM by the device after message completion. Because it resides in RAM, the host has read-write access, although this word is usually treated as read-only by the host.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	EOM	R/W	0	End of Message. This bit is set upon completion of a BC message, whether or not errors occurred.
14	SOM	R/W	0	Start of Message. This bit is set at the start of a BC message and cleared at the end of the message.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). This bit is logic “1” if the BC message was transacted on Bus B. This bit is logic “0” if the BC message was transacted on Bus A.
12	EF	R/W	0	This bit acts as an Error Flag. If EF is logic “1” and some/all of bits 10, 9 or 8 are also set, it is an indication that one or more of those respective errors occurred in the current message. If EF is logic “1” and all of bits 10, 9 and 8 are zero, then a handshake failure has occurred (applies only to transparent mode).
11	STATSET	R/W	0	Status Set. This bit is not affected by the values of mask bits 14-9 in the BC Control Word for the message. This bit is logic “1” when the received RT Status Word contains an unexpected bit value in the bit range 10 − 0. The expected value is usually logic “0”, except when broadcast is enabled.
10	FE	R/W	0	Format Error. This bit is logic “1” when a received RT response violates MIL-STD-1553 message protocol. This includes sync, word count, encoding, bit count or parity errors.
9	TOER	R/W	0	No Response Timeout Error. This bit is logic “1” when a receiving RT responded later than the RT-to-RT Response Timeout interval specified by bits RTRTTO[10 − 9] in Configuration Register #5.

<table>
<tr><th>Bit No.</th><th>Mnemonic</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td>8</td><td>LBE</td><td>R/W</td><td>0</td><td>Loopback Error.
Each word transmitted by the BC is looped back to the receiver and checked for 1553 validity (sync, encoding, bit count and/or parity error). In addition, for each message transacted, the received image for the last word transmitted by the BC is evaluated for data match.
This bit is logic “1” when the received version for one or more words transmitted by the BC fails 1553 “word validity” criteria, and/or the received version for the last word transmitted by the BC does not match the transmitted Manchester II word.</td></tr>
<tr><td>7</td><td>MSTATSET</td><td>R/W</td><td>0</td><td>Masked Status Set.
This bit is logic “1” when one or more of the mask bits 14-9 in the BC Control Word is logic “0” and the corresponding bit is logic “1” in the received RT Status Word.</td></tr>
<tr><td>6 − 5</td><td>RETRY[1:0]</td><td>R/W</td><td>0</td><td>These two bits indicate the number of times a message was retried:
<table>
<tr><th>RETRY1</th><th>RETRY0</th><th>Number of Retries</th></tr>
<tr><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>2</td></tr>
<tr><td>1</td><td>1</td><td>2</td></tr>
</table></td></tr>
<tr><td>4</td><td>GDB</td><td>R/W</td><td>0</td><td>Good Transmit Data Block Transfer.
This bit is set to logic “1” upon successful completion of an error-free RT-to-BC message, RT-to-RT message, or transmit mode code message with data. This bit always resets to logic 0 for any BC-to-RT message, mode code message without data, or any incomplete or invalid message.</td></tr>
<tr><td>3</td><td>WAG</td><td>R/W</td><td>0</td><td>Wrong RT Address and/or No Gap.
This bit is logic 1 when one or both of the following conditions occur:
• the RT address field within a received RT Status Word does not match the RT address field in the Command Word transmitted by the BC or
• the GTEN Gap Check Enable bit 8 of Configuration Register #5 is set and the RT responds with response time less than 4 µs per MIL-STD-1553B, mid-parity bit to mid-sync, (2 µs bus “dead time”).</td></tr>
</table>

Bit No.	Mnemonic	R/W	Reset	Bit Description
2	LE	R/W	0	Word Count (Length) Error. This bit is logic 1 when an RT-to-BC message, RT-to-RT message, or transmit mode code message with data is transacted with the wrong number of data words. This bit always resets to logic 0 for BC-to-RT messages, receive mode code messages, or transmit mode code messages without data.
1	SE	R/W	0	Sync Error. This bit is logic 1 when an RT responds with Data Sync in its Status Word, or with Command/Status Sync in a Data Word.
0 (LSB)	IWE	R/W	0	Invalid Word Error. This bit is logic 1 when an RT response in one or more words having at least one of the following errors: sync encoding error, Manchester II encoding error, bit count error, parity error.

2.21. RT and MT Block Status Word

The following block status word applies to both RT and Message Monitor Modes.

Bit No.	Mnemonic	R/W	Reset	Bit Description
15 (MSB)	EOM	R/W	0	End of Message. This bit is set upon completion of an RT message, whether or not errors occurred.
14	SOM	R/W	0	Start of Message. This bit is set at the start of an RT message and cleared at the end of the message.
13	BID	R/W	0	Bus ID (Bus B / $\overline{\text{Bus A}}$). This bit is logic “1” if the RT message was transacted on Bus B. This bIt is logic “0” if the RT message was transacted on Bus A.
12	EF	R/W	0	This bit acts as an Error Flag. If EF is logic “1” and some/all of bits 10, 9 or 8 (10 and 9 in Message Monitor Mode) are also set, it is an indication that one or more of those respective errors occurred in the current message. If EF is logic “1” and all of bits 10, 9 and 8 (10 and 9 in Message Monitor Mode) are zero, then a handshake failure has occurred (applies only to transparent mode).
11	RTRTRX	R/W	0	This bit will be set in the RT Block Status Word if the device is the receiving RT in an RT-to-RT transfer. In Message Monitor Mode, this bit will be set to indicate the message was an RT-to-RT transfer.
10	FE	R/W	0	Format Error. This bit is logic “1” when a received RT response violates MIL-STD-1553 message protocol. This includes sync, word count, encoding, bit count or parity errors.
9	TOER	R/W	0	No Response Timeout Error. This bit is logic “1” when the device is the receiving RT in an RT-to-RT transfer and the transmitting RT failed to respond, or responded later than the RT-to-RT Response Timeout interval specified by bits RTRTTO[10 − 9] in Configuration Register #5.
8	LBE	R/W	0	Loopback Error. In RT Mode, this bit will be logic “1” following a loopback error, i.e. when the received version of a transmitted word fails 1553 “word validity” criteria, and/or the received version of the last word transmitted does not match the transmitted Manchester II word. In Message Monitor Mode, this bit will be logic “1” following receipt of a valid message. It will be logic “0” if the message was invalid.

Bit No.	Mnemonic	R/W	Reset	Bit Description
7	CIRRO	R/W	0	CIRRO will be set to logic “1” if the enabled global circular buffer rolls over. This will happen if the upper boundary of the circular buffer is exceeded. If OVINV bit 11 of Configuration register #2 is set to logic “1”, the roll over will only occur following receipt of a valid message. Invalid messages will be overwritten and roll over will not occur until the next valid message. In Message Monitor Mode, the size of the circular buffer is set by bits MTDATA[10 − 8] in Configuration Register #3.
6	ILLCMD	R/W	0	In RT Mode, ILLCMD will be set to logic “1” when an illegal command is received.
5	LE	R/W	0	Word Count (Length) Error. This bit is logic 1 when an RT-to-BC message, RT-to-RT message, or transmit mode code message with data is transacted with the wrong number of data words.
4	SE	R/W	0	Sync Error. This bit is logic 1 when an RT responds with Data Sync in its Status Word, or with Command/Status Sync in a Data Word.
3	IWE	R/W	0	Invalid Word Error. This bit is logic 1 when an RT response in one or more words having at least one of the following errors: sync encoding error, Manchester II encoding error, bit count error, parity error.
2	RTRTERR	R/W	0	This bit is set if one of the following occurs during an RT-to-RT transfer: • the RT address of the responding RT does not match the RT address field in the Command Word • the GTEN Gap Check Enable bit 8 of Configuration Register #5 is set and the RT responds with response time less than 4 µs per MIL-STD-1553B, mid-parity bit to mid-sync, (2 µs bus “dead time”) • the responding RT had an invalid status word or wrong sync bit.
1	RTRTERR2	R/W	0	This bit is set if the second command word in an RT-to-RT transfer had an error (e.g. wrong T/$\overline{R}$ bit).
0 (LSB)	CWERR	R/W	0	This bit is set if a received Command Word is undefined (violates MIL-STD-1553 rules), e.g. if broadcast is enabled (BCSTDIS bit 7 in Configuration Register #5 is set to logic “0”) and a mode command not allowed to be broadcast under 1553 rules (e.g. Transmit Last Command) is sent to subaddress 31.

2.22. Word Monitor Identification Word

The Word Monitor Information Word gives information about the received words stored during Word Monitor Mode operation.

Bit No.	Mnemonic	Bit Description
15 (MSB) − 8	GT[7:0]	Gap Time, bits 7 − 0. If CTDATA, bit 1 is logic “0”, then these bits will show the gap time between the start of the current word and the end of the previous word. The resolution is 0.5 µs/LSB, up to a max of 127.5 µs.
7	WF	Word Flag, always set to logic “1”.
6	RTCMD	If RTCMD is logic “0”, then the received word was a valid RT command (correct sync, RT Address and Parity). Otherwise, RTCMD will be logic “1”.
5	BCST	If BCST is logic “0”, then the received word was a valid broadcast command with RT address = 31.
4	ERR	This bit will be set to logic “1” if the received word contained an error.
3	SYNC	If SYNC = logic “1”, then the received word contained a command sync. If SYNC = logic “0”, then the received word contained a data sync.
2	BUSAB	If BUSAB = logic “0”, then the word was received on Bus A. If BUSAB = logic “1”, then the word was received on Bus B.
1	CTDATA	If CTDATA is logic “1”, then previous and next message is contiguous and the gap time bits GT[7:0] above are not used. If CTDATA is logic “0”, then the gap time is stored in bits 15 − 8 above.
0 (LSB)	MCODE	If MCODE is logic “0”, then the received word was a valid mode code command.

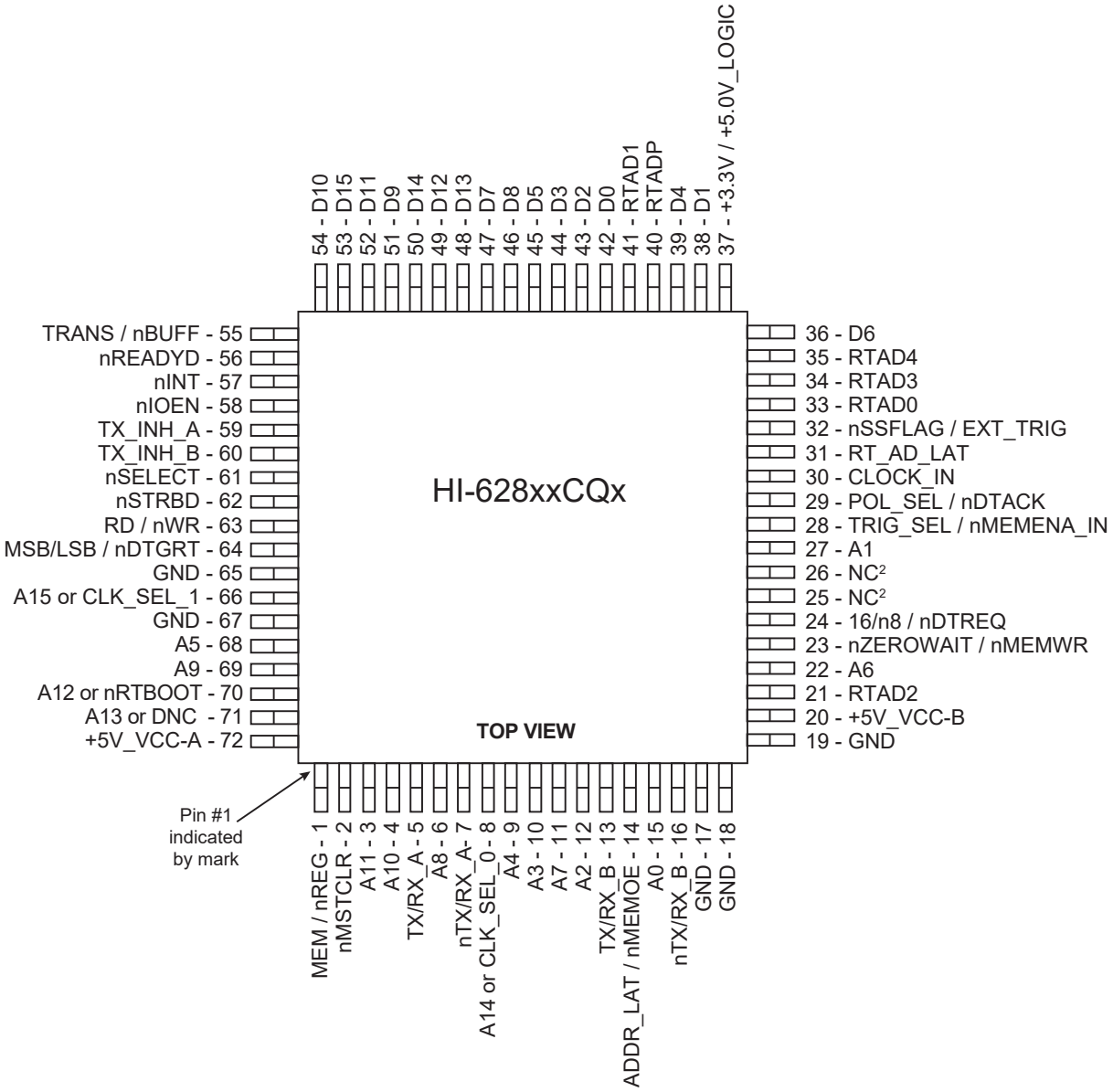
3. PIN DIAGRAMS

Bottom View

RTAD1	D0	RTADP	D2	D7	D14	TRANS / nBUFF	D9	+5V_ VCC-B	9
GND	RTAD4	RTAD3	D1	D6	D15	nINT	nREADYD	GND	8
RTAD2	RTAD0	RT_AD_ LAT	D3	D8	D13	TX_ INH_B	TX_ INH_A	GND	7
POL_SEL / nDTACK	CLOCK _IN	D4	NC	NC	NC	nSELECT	NC	nSTRBD	6
TRIG_SEL / n MEM-ENA_IN	16/n8 / nDTREQ	D5	NC	NC	NC	A15 / CLK_ SEL_1	nMSTCLR	RD / nWR	5
A9	NC	ADDR_LAT / nMEMOE	NC	NC	NC	A14 / CLK_ SEL_0	MEM / nREG	NC	4
+5V_ VCC-A	NC	A0	A2	A4	+5V_ LOGIC	A10	A12 / nRT-BOOT	nIOEN	3
nZERO-WAIT / nMEMWR	nSSFLAG / EXT_TRIG	A1	A3	A5	A8	A11	D12	D11	2
MSB/LSB / nDTGRT	nTX / RX-B	TX / RX-B	A6	A7	nTX / RX-A	TX / RX-A	A13 / DNC	D10	1
J	H	G	F	E	D	C	B	A	

Notes:
1. Prefix “n” denotes an inverted or negative signal, e.g. nIOEN = $\overline{\text{IOEN}}$, etc.
2. “NC” = Not Connected Internally.

Figure 1. 628xxCPx, PGA Package Pinout



Notes:
1. Prefix “n” denotes an inverted or negative signal, e.g. nMSTCLR = $\overline{\text{MSTCLR}}$, etc.
2. Not connected internally.

Figure 2. HI-628xxCQx Gull Wing Package Pinout

4. SIGNAL DESCRIPTIONS

Table 7. Power and Ground

Ball Name	Function	Description
NC	-	Not Connected Internally.
+5V_VCC-A	Power Supply	+5.0V DC power supply for Bus A transceiver.
+5V_VCC-B	Power Supply	+5.0V DC power supply for Bus B transceiver.
+5.0V_LOGIC	Power Supply	+5.0V DC power supply for digital logic.
GND	Power Supply	Power supply ground.

Table 8. MIL-STD-1553 Bus Interface

Signal Name	Function	Description
TX/RX-A	Analog I/O	Bi-directional Bus A interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
$\overline{\text{TX/RX-A}}$	Analog I/O	
TX/RX-B	Analog I/O	Bi-directional Bus B interface to external MIL-STD-1553 isolation transformer. Observe positive / negative polarity.
$\overline{\text{TX/RX-B}}$	Analog I/O	

Table 9. Host Address and Data Buses

<table>
<tr><th>Signal Name</th><th>Function</th><th>Description</th></tr>
<tr><td>D15 (MSB) − D0 (LSB)</td><td>Data inputs or Data outputs</td><td>Bi-directional data bus for host read/write operations on registers and RAM.</td></tr>
<tr><td>A15 (MSB) − A0 (LSB)</td><td>Digital inputs</td><td>These signals function as the address bus for host read/write operations on registers and RAM.</td></tr>
<tr><td rowspan="7">A15 / CLK_SEL_1
and
A14 / CLK_SEL_0</td><td rowspan="7">Digital Input</td><td>For HI-62835Cxx devices (MIL-STD-1760 boot option, 4K RAM), these signals function as CLK_SEL_1 and CLK_SEL_0 and set the clock frequency as follows:</td></tr>
<tr><td>CLK_SEL_1 | CLK_SEL_0 | Clock Frequency</td></tr>
<tr><td>0 | 0 | 10 MHz</td></tr>
<tr><td>0 | 1 | 20 MHz</td></tr>
<tr><td>1 | 0 | 12 MHz</td></tr>
<tr><td>1 | 1 | 16 MHz</td></tr>
<tr><td>For all other devices, these signals function as address lines A15 and A14.</td></tr>
<tr><td>A13 / DNC</td><td>Digital Input</td><td>For HI-62835Cxx devices (MIL-STD-1760 boot option, 4K RAM), this signal has no function and should be left unconnected.
For all other devices, this signal functions as address line A13.</td></tr>
<tr><td rowspan="4">A12 / $\overline{\text{RTBOOT}}$</td><td rowspan="4">Digital Input</td><td>For HI-62835Cxx devices (MIL-STD-1760 boot option, 4K RAM), this signal functions as $\overline{\text{RTBOOT}}$. as follows:</td></tr>
<tr><td>$\overline{\text{RTBOOT}}$ = Logic "1"</td><td>$\overline{\text{RTBOOT}}$ = Logic "0"</td></tr>
<tr><td>The RT will initialize in Idle mode.</td><td>Enable MIL-STD-1760 operation (the RT will initialize with the busy bit set in the RT Status Word).</td></tr>
<tr><td colspan="2">For all other devices, this signal functions as address line A12.</td></tr>
<tr><td>A11 − A0 (LSB)</td><td>Digital Input</td><td>Lower 12 bits of 16-bit bi-directional address bus.</td></tr>
</table>

Table 10. Host Interface

Signal Name	Function	Description
$\overline{\text{SELECT}}$	Digital Input	The Host sets this signal to logic "0" to select the device for a transfer to / from RAM (or registers).
$\overline{\text{STRBD}}$	Digital Input	This signal is used by the host with the $\overline{\text{SELECT}}$ signal to initiate data transfers to / from the device. $\overline{\text{STRBD}}$ must remain low during the data transfer cycle.
RD / $\overline{\text{WR}}$	Digital Input	Read/$\overline{\text{Write}}$. RD/$\overline{\text{WR}}$ specifies reading or writing between the host. The polarity depends on the state of the POL_SEL signal (see below).
ADDR_LAT or $\overline{\text{MEMOE}}$	Digital Input or Digital Output	When in buffered mode, this signal is an input and functions as ADDR_LAT. When ADDR_LAT transitions low, it latches the values on A15 − A0, $\overline{\text{SELECT}}$, MEM / $\overline{\text{REG}}$, and MSB / LSB. When ADDR_LAT is high, the values of these signals track the respective inputs. When in transparent mode, this signal is an output and functions as $\overline{\text{MEMOE}}$. It is used to enable external RAM reads and should be connected to the $\overline{\text{OE}}$ input signal on an external RAM.
$\overline{\text{ZEROWAIT}}$ or $\overline{\text{MEMWR}}$	Digital Input or Digital Output	When in buffered mode, this signal is an input and functions as $\overline{\text{ZEROWAIT}}$ as follows; $\overline{\text{ZEROWAIT}}$ = “0” specifies zero wait mode, $\overline{\text{ZEROWAIT}}$ = “1” specifies non-zero wait mode. When in transparent mode, this signal is an output and functions as $\overline{\text{MEMWR}}$. It is used in transparent mode for external RAM data transfers and should be connected to the $\overline{\text{WR}}$ input signal on the external RAM.
16 / $\overline{8}$ or $\overline{\text{DTREQ}}$	Digital Input or Digital Output	When in buffered mode, this signal is an input and functions as 16 / $\overline{8}$. It is used to specify 16 bit data mode (16 / $\overline{8}$ = “1”) or 8-bit data mode (16 / $\overline{8}$ = “0”). When in transparent mode, this signal is an output and functions as $\overline{\text{DTREQ}}$ (Data Transfer Request). It is used by the device to request access to the host address and data buses. The handshake is complete when the $\overline{\text{DTGRT}}$ (Data Transfer Grant) signal is asserted in response.
MSB / LSB or $\overline{\text{DTGRT}}$	Digital Input or Digital Input	When in buffered mode (8-bit only), this signal is an input and functions as (MSB / LSB). It is used to indicate whether the MSB or LSB is currently being transferred. The polarity of MSB / LSB is controlled by the POL_SEL input (see below). When in transparent mode, this signal is an input and functions as the $\overline{\text{DTGRT}}$ signal. It completes the handshake following a $\overline{\text{DTREQ}}$ request and is asserted to indicate that control of the host address and data buses have been released to the device.

<table>
<tr><th>Signal Name</th><th>Function</th><th colspan="3">Description</th></tr>
<tr><td rowspan="4">POL_SEL

or

$\overline{\text{DTACK}}$</td><td rowspan="4">Digital Input

or

Digital Output</td><td colspan="3">Polarity Select or Data Transfer Bus Acknowledge.
When in buffered mode, this signal is an input and functions as POL_SEL. In 16-bit mode, it controls the polarity of the RD / $\overline{\text{WR}}$ signal and in 8-bit mode it controls the polarity of the MSB / LSB signal as follows:</td></tr>
<tr><td>POL_SEL</td><td>16-bit buffered mode</td><td>8-bit-buffered mode</td></tr>
<tr><td>1</td><td>Assert RD / $\overline{\text{WR}}$ = 1 for RD.
Assert RD / $\overline{\text{WR}}$ = 0 for WR.</td><td>Assert MSB / LSB = 1 for LSB.
Assert MSB / LSB = 0 for MSB.</td></tr>
<tr><td>0</td><td>Assert RD / $\overline{\text{WR}}$ = 0 for RD.
Assert RD / $\overline{\text{WR}}$ = 1 for WR.</td><td>Assert MSB / LSB = 0 for LSB.
Assert MSB / LSB = 1 for MSB.</td></tr>
<tr><td>$\overline{\text{DTACK}}$</td><td>Digital Output</td><td colspan="3">When in transparent mode, this signal is an output and functions as $\overline{\text{DTACK}}$. It is asserted to acknowledge a data transfer grant ($\overline{\text{DTGRT}}$) and indicates that the device has accepted control of the host address and data buses.</td></tr>
<tr><td rowspan="4">TRIG_SEL

or

$\overline{\text{MEMENA\_IN}}$</td><td rowspan="4">Digital Input

or

Digital Input</td><td colspan="3">In 8-bit buffered mode, this signal is an input and functions as TRIG-SEL. It is used to select the "endianness" (byte order) of 16-bit word transfers to or from the device as follows:</td></tr>
<tr><td>TRIG_SEL</td><td>8-bit buffered mode</td><td>16-bit buffered mode</td></tr>
<tr><td>1</td><td>MSB followed by LSB.</td><td>No function. May be left unconnected.</td></tr>
<tr><td>0</td><td>LSB followed by MSB.</td><td>No function. May be left unconnected.</td></tr>
<tr><td>$\overline{\text{MEMENA\_IN}}$</td><td>Digital Input</td><td colspan="3">When in transparent mode, this signal is an input and functions as $\overline{\text{MEMENA\_IN}}$. It is used as a Chip Select input to the internal RAM.
NOTE: If only internal RAM is used, $\overline{\text{MEMENA\_IN}}$ should be connected directly to the output of a OR Gate which has $\overline{\text{DTACK}}$ and $\overline{\text{IOEN}}$ as inputs.</td></tr>
<tr><td>MEM/ $\overline{\text{REG}}$</td><td>Digital Input</td><td colspan="3">This input is used by the host to notify the device of memory or register access.
MEM / $\overline{\text{REG}}$ = "1" for memory access or
MEM / $\overline{\text{REG}}$ = "0" for register access.</td></tr>
</table>

Signal Name	Function	Description	
$\overline{\text{SSFLAG}}$ or EXT_TRIG	Digital Input or Digital Input	Subsystem Flag (RT) or External Trigger input. In RT mode, this signal functions as $\overline{\text{SSFLAG}}$. If asserted (logic "0"), the Subsystem Flag bit will be set in the transmitted RT Status Word. In BC or MT modes, this signal functions as an External Trigger as follows.	
		BC Mode	
		Non-Enhanced Mode (Legacy)	No function.
		Enhanced Mode (Legacy)	If the external trigger is enabled by setting bit 7 in Configuration Register #1, a low-to-high transition on EXT_TRIG will initiate a BC Start.
		Enhanced Mode	When a Wait for External Trigger (WTG) instruction is executed, the BC will wait for a low-to-high transition on EXT_TRIG before executing the next instruction.
		MT Mode	
		Word Monitor	If the external trigger is enabled by setting bit 7 in Configuration Register #1, a low-to-high transition on EXT_TRIG will start monitor operation.
		Message Monitor	No effect.
TRANSPARENT / $\overline{\text{BUFFERED}}$	Digital Input	Transparent or Buffered Mode Selection TRANSPARENT / $\overline{\text{BUFFERED}}$ = "0" for Buffered Mode or TRANSPARENT / $\overline{\text{BUFFERED}}$ = "1" for Transparent Mode	
$\overline{\text{READYD}}$	Digital Output	This output indicates to the host processor the status or availability of data transferred to or from the device respectively. The host will initiate a transfer cycle by asserting $\overline{\text{STRBD}}$ low. When the data is ready the device will assert $\overline{\text{READYD}}$ low, indicating to the host that the transfer is complete. The host will then assert $\overline{\text{STRBD}}$ high, following which $\overline{\text{READYD}}$ will return to logic "1", indicating that the device is ready for the next transfer.	
$\overline{\text{IOEN}}$	Digital Output	I/O Enable. This output allows tri-state control for external addresses and data buffers. It is asserted low during data transfer cycles and remains low until $\overline{\text{STRBD}}$ is asserted high ending the current transfer.	

Table 11. RT Address

Signal Name	Function	Description
RTAD4 (MSB)	Digital Input	RT Address Input signals.
RTAD3	Digital Input	
RTAD2	Digital Input	
RTAD1	Digital Input	
RTAD0 (LSB)	Digital Input	
RTADP	Digital Input	Remote Terminal Address Parity. Used to provide odd parity for the RT address on RTAD[4:0].
RT_AD_LAT	Digital Input	RT Address Latch. This input signal is used to control how the RT address is latched internally. If RT_AD_LAT is logic "0", then the RT address and parity will simply track RTAD4:0 and RTADP inputs. If RT_AD_LAT transitions from logic "0" to logic "1", the values on RTAD4:0 and RTADP will then be latched on the rising edge of RT_AD_LAT. If RT_AD_LAT is connected to logic "1", then the RT address may be latched under software control as follows: a. The RT Address Input signals RTAD4 through RTAD0 **must** be connected to the data bus inputs D5 − D1 respectively and the RTADP parity input signal **must** be connected to data bus input D0. b. The device must be operating in Enhanced mode (Configuration Register #3, bit 15 = logic "1"). c. Bit 3 of Configuration Register #4 (RTLATEN) should be written logic "1". d. The RT address and parity are programmed by writing the lower 6 bits of Configuration Register #5 (RTAD[4:0] and RTADP (LSB) respectively).

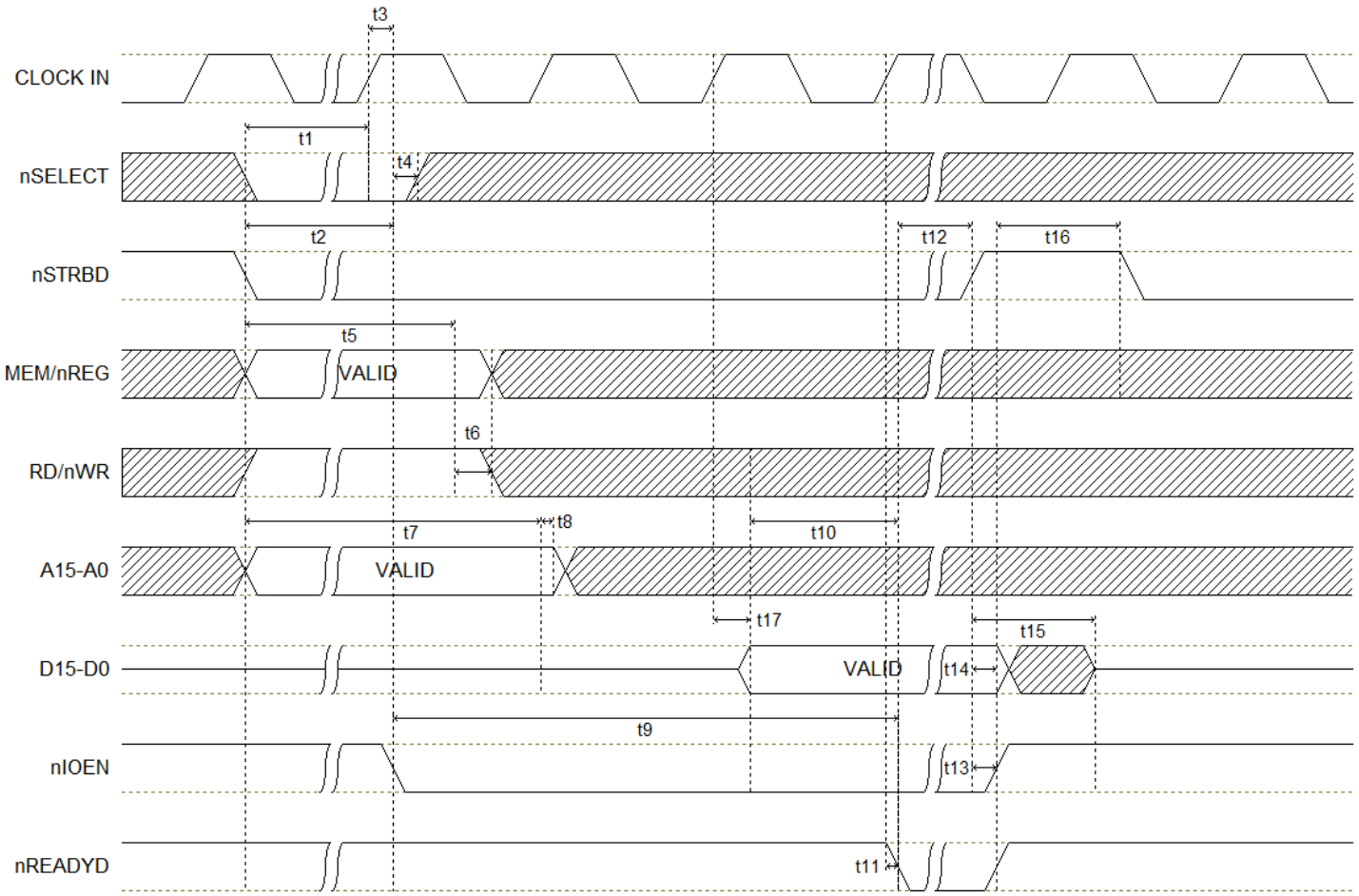
Table 12. Other Signals

Signal Name	Function	Description
$\overline{INT}$	Digital Output	Interrupt Request. If Configuration Register #2, bit 3 LEVEL is logic "0", the interrupt request output on $\overline{INT}$ will be a negative pulse of about 500 ns. If LEVEL is logic "1", the interrupt request output on $\overline{INT}$ will be a LOW continuous level. To clear the interrupt, one of following events should occur: 1. Logic "1" should be written to bit 2 of the Start/Reset Register (INTRST); or 2. If bit 4 of Configuration Register #2 (CLRSTAT) is logic "1", then reading the Interrupt Status Register will clear $\overline{INT}$. **NOTE:** In cases where both Interrupt Status Registers #1 and #2 have bits set, **both** registers must be read in order to clear $\overline{INT}$.
CLOCK_IN	Digital Input	20 MHz, 16 MHz, 12 MHz, or 10 MHz clock input.
TX_INH_A	Digital Input	Transmit inhibit inputs for Bus A and Bus B, active high. These two inputs enable (logic "0") or inhibit (logic "1") transmit on Bus A or Bus B, affecting behavior for all enabled 1553 devices.
TX_INH_B	Digital Input	
$\overline{MSTCLR}$	Digital Input	Master Reset, active low.

5. HOST INTERFACE

The most commonly used host interface is the 16-bit buffered, non-zero wait mode. This configuration may be used to interface the device with a 16 or 32-bit microprocessor. In this mode the device does not access external memory and uses the internal 4K or 64K words of RAM for storing MIL-STD-1553 data and related buffering. Figure 3 and Table 13 illustrate host read timing and Figure 4 and Table 14 illustrate host write timing respectively.

5.1. Host RAM/Register Read (16-BIT Buffered, Nonzero Wait)



Note: Timing intervals not to scale. For illustration purposes only.

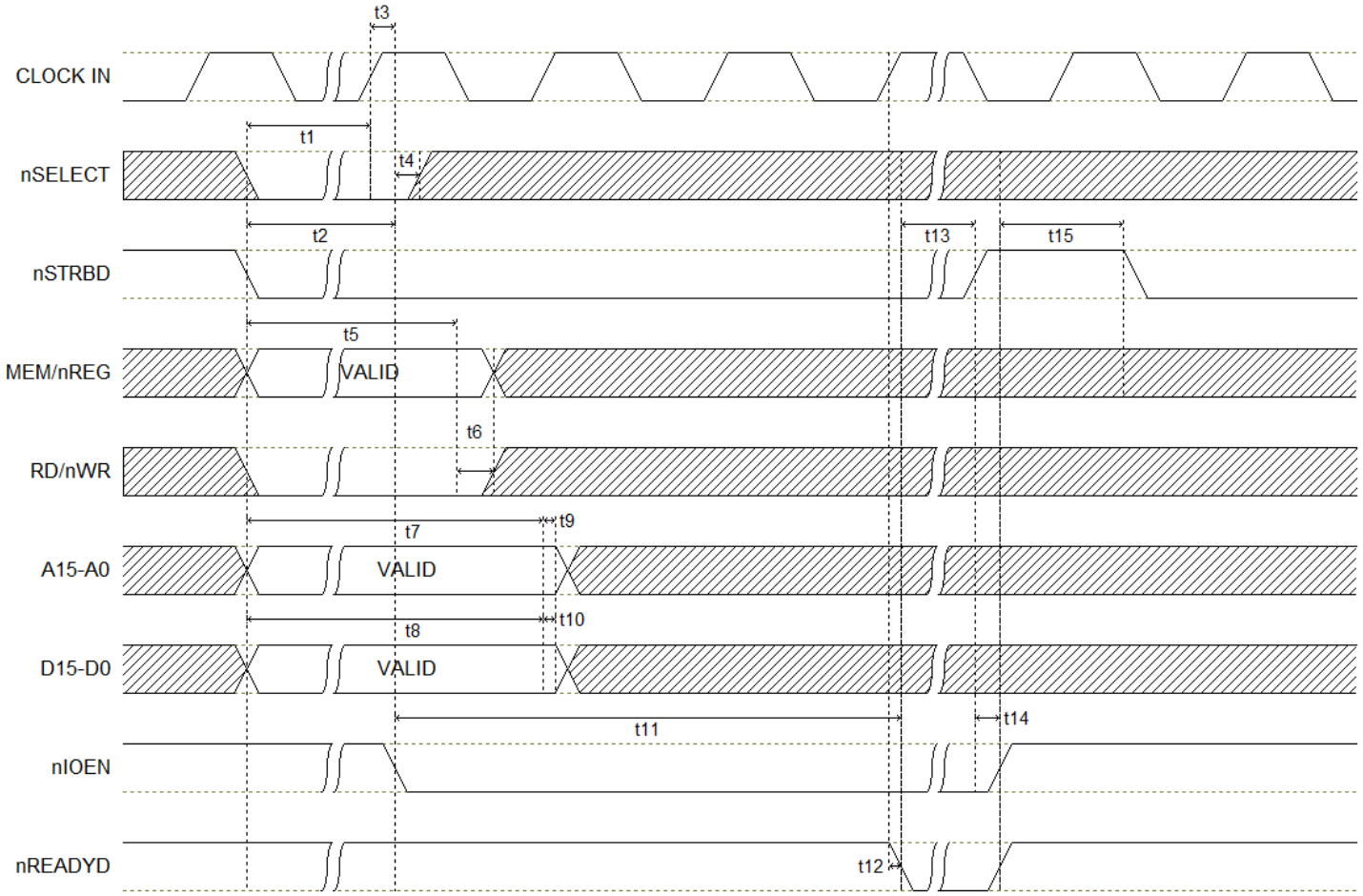
Figure 3. Host RAM/Register Read Timing Diagram (16-BIT Buffered, Nonzero Wait)

Table 13. Host RAM/Register Read Timing (16-BIT Buffered, Nonzero Wait)

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time to clock rising edge	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ falling edge (No contention @ 20 MHz)			100			105	ns
	(Contention, with Bit 14, Config. Reg #6, ENHCPU = “0” @ 20 MHz)			3.6			3.6	µs
	(Contention, with ENHCPU = “1” @ 20 MHz)			515			520	ns
	(No contention @ 16 MHz)			112			117	ns
	(Contention, with ENHCPU = “0” @ 16 MHz)			4.6			4.6	µs
	(Contention, with ENHCPU = “1” @ 16 MHz)			630			635	ns
	(No contention @ 12 MHz)			133			138	ns
	(Contention, with ENHCPU = “0” @ 12 MHz)			6.0			6.0	µs
	(Contention, with ENHCPU = “1” @ 12 MHz)			815			820	ns
	(No contention @ 10 MHz)			150			155	ns
	(Contention, with ENHCPU = “0” @ 10 MHz)			7.2			7.2	µs
	(Contention, with ENHCPU = “1” @ 10 MHz)			965			970	ns
t3	$\overline{\text{IOEN}}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t4	$\overline{\text{SELECT}}$ hold time from $\overline{\text{IOEN}}$ falling edge	0			0			ns
t5	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ setup time to CLOCK IN falling edge	10			15			ns
t6	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ hold time from CLOCK IN falling edge	30			30			ns
t7	Address valid setup time to CLOCK IN rising edge	30			35			ns
t8	Address valid hold time from CLOCK IN rising edge	30			30			ns

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t9	$\overline{IOEN}$ falling edge delay to $\overline{READYD}$ falling edge (@ 20 MHz)	135	150	165	135	150	165	ns
	(@ 16 MHz)	170	187.5	205	170	187.5	205	ns
	(@ 12 MHz)	235	250	265	235	250	265	ns
	(@ 10 MHz)	285	300	315	285	300	315	ns
t10	Output Data valid to $\overline{READYD}$ falling edge (@ 20 MHz)	21			11			ns
	(@ 16 MHz)	33			23			ns
	(@ 12 MHz)	54			44			ns
	(@ 10 MHz)	71			61			ns
t11	$\overline{READYD}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t12	$\overline{READYD}$ falling edge to $\overline{STRBD}$ rising edge			∞			∞	ns
t13	$\overline{STRBD}$ rising edge delay to $\overline{IOEN}$ and $\overline{READYD}$ rising edge			30			40	ns
t14	Output Data hold time from $\overline{STRBD}$ rising edge	0			0			ns
t15	$\overline{STRBD}$ rising edge delay to output data tri-state			40			40	ns
t16	$\overline{STRBD}$ high hold time from $\overline{READYD}$ rising edge	0			0			ns
t17	CLOCK IN rising edge delay to output data valid			40			40	ns

5.2. Host RAM/Register Write (16-BIT Buffered, Nonzero Wait)



Note: Timing intervals not to scale. For illustration purposes only.

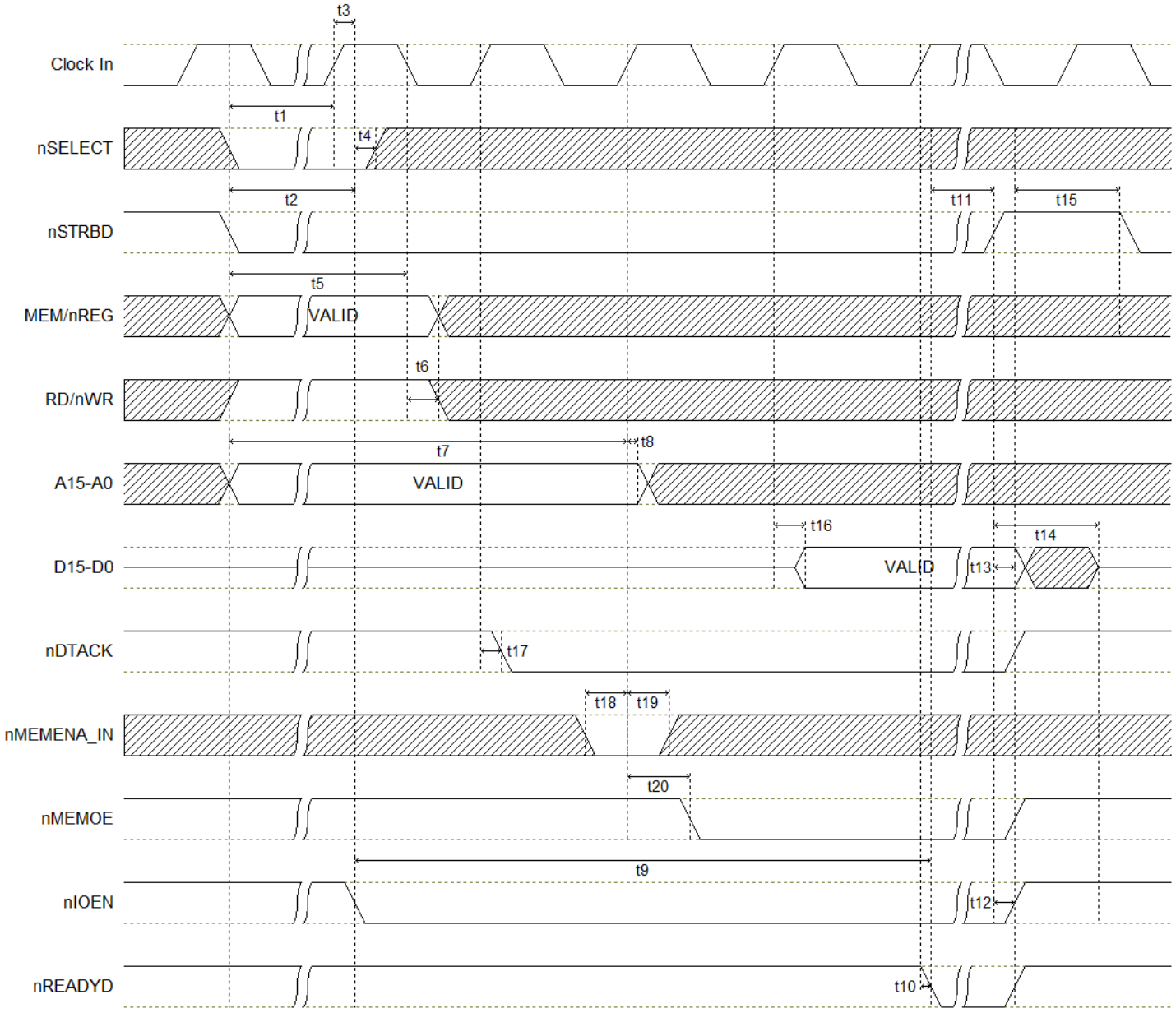
Figure 4. Host RAM/Register Write Timing Diagram (16-BIT Buffered, Nonzero Wait)

Table 14. Host RAM/Register Write Timing (16-BIT Buffered, Nonzero Wait)

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time to clock rising edge	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ falling edge (No contention @ 20 MHz)			100			105	ns
	(Contention, with Bit 14, Config. Reg #6, ENHCPU = “0” @ 20 MHz)			3.6			3.6	µs
	(Contention, with ENHCPU = “1” @ 20 MHz)			465			470	ns
	(No contention @ 16 MHz)			112			117	ns
	(Contention, with ENHCPU = “0” @ 16 MHz)			4.6			4.6	µs
	(Contention, with ENHCPU = “1” @ 16 MHz)			565			570	ns
	(No contention @ 12 MHz)			133			138	ns
	(Contention, with ENHCPU = “0” @ 12 MHz)			6.0			6.0	µs
	(Contention, with ENHCPU = “1” @ 12 MHz)			732			737	ns
	(No contention @ 10 MHz)			150			155	ns
	(Contention, with ENHCPU = “0” @ 10 MHz)			7.2			7.2	µs
	(Contention, with ENHCPU = “1” @ 10 MHz)			865			870	ns
t3	$\overline{\text{IOEN}}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t4	$\overline{\text{SELECT}}$ hold time from $\overline{\text{IOEN}}$ falling edge	0			0			ns
t5	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ setup time to CLOCK IN falling edge	10			15			ns
t6	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ hold time from CLOCK IN falling edge	30			35			ns
t7	Address valid setup time to CLOCK IN rising edge	30			35			ns
t8	Data valid setup time to CLOCK IN rising edge	10			15			ns
t9	Address valid hold time from CLOCK IN rising edge	30			30			ns
t10	Data valid hold time from CLOCK IN rising edge	10			15			ns

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t11	$\overline{\text{IOEN}}$ falling edge delay to $\overline{\text{READYD}}$ falling edge (@ 20 MHz)	85	100	115	85	100	115	ns
	(@ 16 MHz)	110	125	140	110	125	140	ns
	(@ 12 MHz)	152	167	182	152	167	182	ns
	(@ 10 MHz)	185	200	215	185	200	215	ns
t12	$\overline{\text{READYD}}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t13	$\overline{\text{READYD}}$ falling edge to $\overline{\text{STRBD}}$ rising edge			∞			∞	ns
t14	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ rising edge			30			40	ns
t15	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising edge	10			10			ns

5.3. Host RAM/Register Read (Transparent Mode)



Note: Timing intervals not to scale. For illustration purposes only.

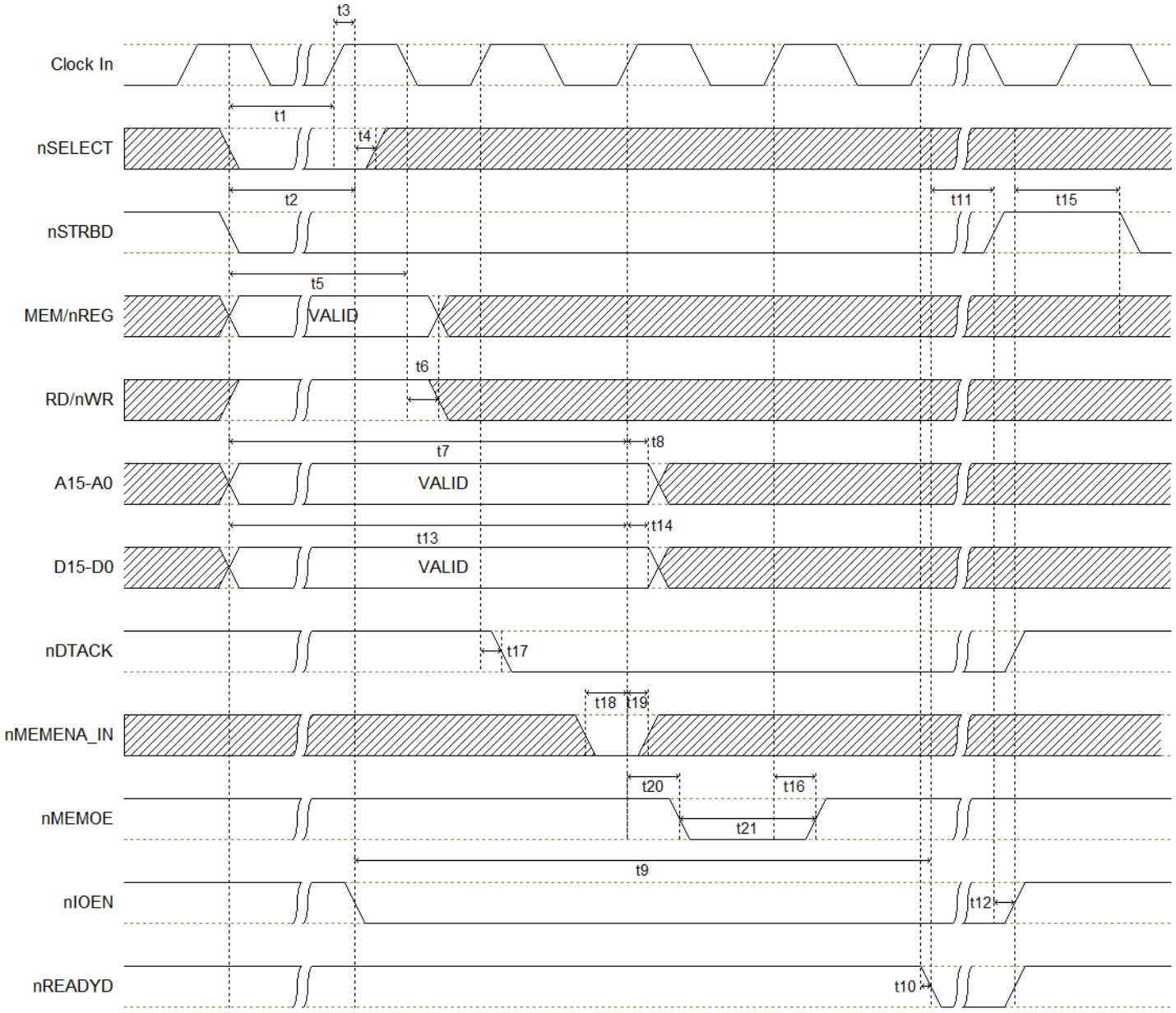
Figure 5. Host RAM/Register Read Timing Diagram (Transparent Mode)

Table 15. Host RAM/Register Read Timing (Transparent Mode)

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time to clock rising edge	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ falling edge (No contention @ 20 MHz)			100			105	ns
	(Contention @ 20 MHz)			3.6			3.6	µs
	(No contention @ 16 MHz)			112			117	ns
	(Contention @ 16 MHz)			4.6			4.6	µs
	(No contention @ 12 MHz)			133			138	ns
	(Contention @ 12 MHz)			6.0			6.0	µs
	(No contention @ 10 MHz)			150			155	ns
	(Contention @ 10 MHz)			7.2			7.2	µs
t3	$\overline{\text{IOEN}}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t4	$\overline{\text{SELECT}}$ hold time from $\overline{\text{IOEN}}$ falling edge	0			0			ns
t5	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ setup time to CLOCK IN falling edge	10			15			ns
t6	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ hold time from CLOCK IN falling edge	30			30			ns
t7	Address valid setup time to CLOCK IN rising edge	30			35			ns
t8	Address valid hold time from CLOCK IN rising edge	30			30			ns
t9	$\overline{\text{IOEN}}$ falling edge delay to $\overline{\text{READYD}}$ falling edge (@ 20 MHz)	185	200	215	185	200	215	ns
	(@ 16 MHz)	235	250	265	235	250	265	ns
	(@ 12 MHz)	315	333	350	315	333	350	ns
	(@ 10 MHz)	385	400	415	385	400	415	ns
t10	$\overline{\text{READYD}}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t11	$\overline{\text{READYD}}$ falling edge to $\overline{\text{STRBD}}$ rising edge			5.0			5.0	µs
t12	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ rising edge			30			40	ns
t13	Output Data hold time from $\overline{\text{STRBD}}$ rising edge	0			0			ns

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t14	$\overline{\text{STRBD}}$ rising edge delay to output data tri-state			40			40	ns
t15	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising edge	0			0			ns
t16	CLOCK IN rising edge delay to output data valid			40			40	ns
t17	CLOCK IN rising edge delay to $\overline{\text{DTACK}}$ falling edge			40			40	ns
t18	$\overline{\text{MEMENA\_IN}}$ setup time to CLOCK IN rising edge	10			10			ns
t19	$\overline{\text{MEMENA\_IN}}$ hold time from CLOCK IN rising edge	30			30			ns
t20	CLOCK IN rising edge delay to $\overline{\text{MEMOE}}$ falling edge			40			40	ns

5.4. Host RAM/Register Write (Transparent Mode)



Note: Timing intervals not to scale. For illustration purposes only.

Figure 6. Host RAM/Register Write Timing Diagram (Transparent Mode)

Table 16. Host RAM/Register Write Timing (Transparent Mode)

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t1	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low setup time to clock rising edge	10			15			ns
t2	$\overline{\text{SELECT}}$ and $\overline{\text{STRBD}}$ low to $\overline{\text{IOEN}}$ falling edge (No contention @ 20 MHz)			100			105	ns
	(Contention @ 20 MHz)			3.6			3.6	µs
	(No contention @ 16 MHz)			112			117	ns
	(Contention @ 16 MHz)			4.6			4.6	µs
	(No contention @ 12 MHz)			133			138	ns
	(Contention @ 12 MHz)			6.0			6.0	µs
	(No contention @ 10 MHz)			150			155	ns
	(Contention @ 10 MHz)			7.2			7.2	µs
t3	$\overline{\text{IOEN}}$ falling edge delay from CLOCK IN rising edge.			40			40	ns
t4	$\overline{\text{SELECT}}$ hold time from $\overline{\text{IOEN}}$ falling edge	0			0			ns
t5	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ setup time to CLOCK IN falling edge	10			15			ns
t6	MEM / $\overline{\text{REG}}$ and RD / $\overline{\text{WR}}$ hold time from CLOCK IN falling edge	30			30			ns
t7	Address valid setup time to CLOCK IN rising edge	30			10			ns
t8	Address valid hold time from CLOCK IN rising edge	30			25			ns
t9	$\overline{\text{IOEN}}$ falling edge delay to $\overline{\text{READYD}}$ falling (@ 20 MHz)	185	200	215	185	200	215	ns
	(@ 16 MHz)	235	250	265	235	250	265	ns
	(@ 12 MHz)	315	333	350	315	333	350	ns
	(@ 10 MHz)	385	400	415	385	400	415	ns
t10	$\overline{\text{READYD}}$ falling edge delay from CLOCK IN rising edge.			35			30	ns
t11	$\overline{\text{READYD}}$ edge falling to $\overline{\text{STRBD}}$ rising edge			5.0			5.0	µs
t12	$\overline{\text{STRBD}}$ rising edge delay to $\overline{\text{IOEN}}$ and $\overline{\text{READYD}}$ rising edge			30			35	ns
t13	Data setup time to CLOCK IN rising edge	10			10			ns

Time	Description	Response Time						Units
		5V Logic			3.3V Logic			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
t14	Data hold time from CLOCK IN rising edge	30			25			ns
t15	$\overline{\text{STRBD}}$ high hold time from $\overline{\text{READYD}}$ rising edge	0			0			ns
t16	CLOCK IN rising edge delay to $\overline{\text{MEMOE}}$ rising edge			30			30	ns
t17	CLOCK IN rising edge delay to $\overline{\text{DTACK}}$ falling edge			35			30	ns
t18	$\overline{\text{MEMENA\_IN}}$ setup time to CLOCK IN rising edge	5			10			ns
t19	$\overline{\text{MEMENA\_IN}}$ hold time from CLOCK IN rising edge	30			25			ns
t20	CLOCK IN rising edge delay to $\overline{\text{MEMOE}}$ falling edge			40			30	ns
t21	$\overline{\text{MEMOE}}$ low pulse width (@ 20 MHz)	37		62	37		62	ns
	(@ 16 MHz)	50		75	50		75	ns
	(@ 12 MHz)	70		95	70		95	ns
	(@ 10 MHz)	87		112	87		112	ns

6. ELECTRICAL CHARACTERISTICS

6.1. Absolute Maximum Ratings

Supply voltages	Logic +5V	-0.3 V to +6.0 V
	Transceivers +5V	-0.3 V to +7.0 V
Logic input voltage range		-0.3 V to +6.0 V
Receiver differential voltage		10 Vp-p
Solder Temperature (reflow)		260°C
Junction Temperature		175°C
Storage Temperature		-65°C to +150°C

6.2. Recommended Operating Conditions

Parameters		Limits			Unit
		Min	Typ	Max	
Supply Voltages	Logic	4.5	5.0	5.5	V
	5.0V Transceivers	4.75	5.0	5.25	V
Temperature Range	Industrial	-40		85	°C
	Extended	-55		125	°C

6.3. DC Electrical Characteristics

T_A = Operating Temperature Range

Parameters		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Power Supply							
Operating Supply Voltages	5.0V Logic	V_{DD}		4.5	5.0	5.5	V
	5.0V Transceivers	V_{DD}		4.75	5.0	5.25	V
Power Supply Current See Note 1	V_{LOGIC} = 5.0V = V_{DD}	I_{CC1}	Not Transmitting	-	10	15	mA
		I_{CC2}	Continuous supply current while one bus transmits @ 50% duty cycle, 70Ω resistive load	-	340	410	mA
		I_{CC23}	Continuous supply current while one bus transmits @ 100% duty cycle, 70Ω resistive load	-	560	645	mA
Power Dissipation See Note 2	V_{LOGIC} = 5.0V = V_{DD}	PD_1	Not Transmitting	-	-	60	mW
		PD_2	Transmit one bus @ 50% duty cycle, 70Ω resistive load	-	1.20	1.45	W
		PD_3	Transmit one bus @ 100% duty cycle, 70Ω resistive load	-	1.80	1.90	W
Logic							
Input Voltage (High)		V_{IH}	All digital inputs	2.1	-	-	V
Input Voltage (Low)		V_{IL}	All digital inputs	-	-	0.7	V
Schmidt Trigger Hysteresis		V_{HYST}	All digital inputs	0.2			V
Input Current (High)		I_{IH}	All digital inputs V_{LOGIC} = 5.25V = V_{IH} V_{LOGIC} = 5.25V, V_{IH} = 2.7V	 -10 -350	 - -	 -10 -50	 µA µA
Input Current (Low)		I_{IL}	All digital inputs V_{LOGIC} = 5.25V, V_{IL} = 0.4V	 -350	 -	 -50	 µA
Output Voltage (High)		V_{OH}	V_{LOGIC} = 4.5V, V_{IH} = 2.7V, V_{IL} = 0.2V, I_{OH} = max	2.4	-	-	V
Output Voltage (Low)		V_{OL}	V_{LOGIC} = 4.5V, V_{IH} = 2.7V, V_{IL} = 0.2V, I_{OL} = max	-	-	0.4	V
Output Current (High)		I_{OH}	V_{LOGIC} = 4.5V	-	-	-3.4	mA
Output Current (Low)		I_{OL}	V_{LOGIC} = 4.5V	3.4	-	-	mA
RECEIVER (Measured at Point "AD" in Table 1 unless otherwise specified)							
Input Resistance		R_{IN}	Differential	20	-	-	kΩ
Input Capacitance		C_{IN}	Differential	-	-	5	pF
Common Mode Rejection Ratio		CMRR		40	-	-	dB

Parameters		Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Input Level		V_{IN}	Differential	-	-	9	Vp-p
Input Common Mode Voltage		V_{ICM}		-10	-	+10	V-pk
Threshold Voltage (Direct-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point “AD“ in Table 1)	1.2	-	20.0	Vp-p
	No Detect	V_{THND}		-	-	0.28	Vp-p
Threshold Voltage (Transformer-Coupled)	Detect	V_{THD}	1 MHz Sine Wave (Measured at Point “AT“ in Table 13)	0.86	-	14.0	Vp-p
	No Detect	V_{THND}		-	-	0.2	Vp-p
TRANSMITTER (Measured at Point “AD” in Table 1 unless otherwise specified)							
Output Voltage	Direct Coupled	V_{OUT}	35Ω Load	6.0	7.0	9.0	Vp-p
	Transformer Coupled	V_{OUT}	70Ω Load (Measured at Point “AT“ in Table 13)	20.0	22	27.0	Vp-p
Output Noise		V_{ON}	Differential, Direct Coupled	-	-	10.0	mVp-p
Output Dynamic Offset Voltage	Direct Coupled	V_{DYN}	35Ω Load	-90	-	90	mV
	Transformer Coupled	V_{DYN}	70Ω Load (Measured at Point “AT“ in Table 13)	-250	-	250	mVp
Rise/Fall Time	HI-623x5xxxx	$t_{r/f}$	MIL-STD-1553B compliant	100	150	300	ns
	HI-623x6Cxxx	$t_{r/f}$	McAir compliant	200	250	300	ns
Output Resistance		R_{OUT}	Differential, not transmitting	10	-	-	kΩ
Output Capacitance		C_{OUT}	1 MHz sine wave	-	-	15	pF
Clock Input							
Frequency	(Default)	CLK_{IN}			16.0		MHz
	(option)				12.0		MHz
	(option)				10.0		MHz
	(option)				20.0		MHz
Master Reset ($\overline{\text{MSTCLR}}$) Timing							
Minimum $\overline{\text{MSTCLR}}$ pulsewidth for Master Reset		t_{MR}		100			ns
MIL-STD-1553 Message Timing							
Completion of CPU write (BC Start) to Start of First Message for non-Enhanced BC Mode					2.5		µs
BC intermessage gap time (typical value; may be lengthened under software control to 65.535 ms)			non-Enhanced BC Mode		9.5		µs
			Enhanced BC Mode		10.5		µs
BC/RT/MT Response Timeout (Software programmable, 4 options)			18.5 nominal	17.5	18.0	19.5	µs
			22.5 nominal	21.5	22.5	23.5	µs
			50.5 nominal	49.5	50.5	51.5	µs
			128.0 nominal	127.0	129.5	131.0	µs
RT Response Time (mid-parity to mid-sync)				4		7	µs
Transmitter Watchdog Timeout					660.5		µs

Note 1: In actual use, the highest practical transmit duty cycle is 96%, occurring when a Remote Terminal responds to a series of 32 data word transmit commands (RT to BC) repeating with minimum intermessage gap of 4µs (2µs dead time) and typical RT response delay of 5µs.

Note 2: While one bus continuously transmits, the power delivered by the power supply is 5.0V × 560mA typical = 2.8W. Of this, 1.80W is dissipated in the device, the remainder in the load.

6.4. MIL-STD-1553 Bus Interface

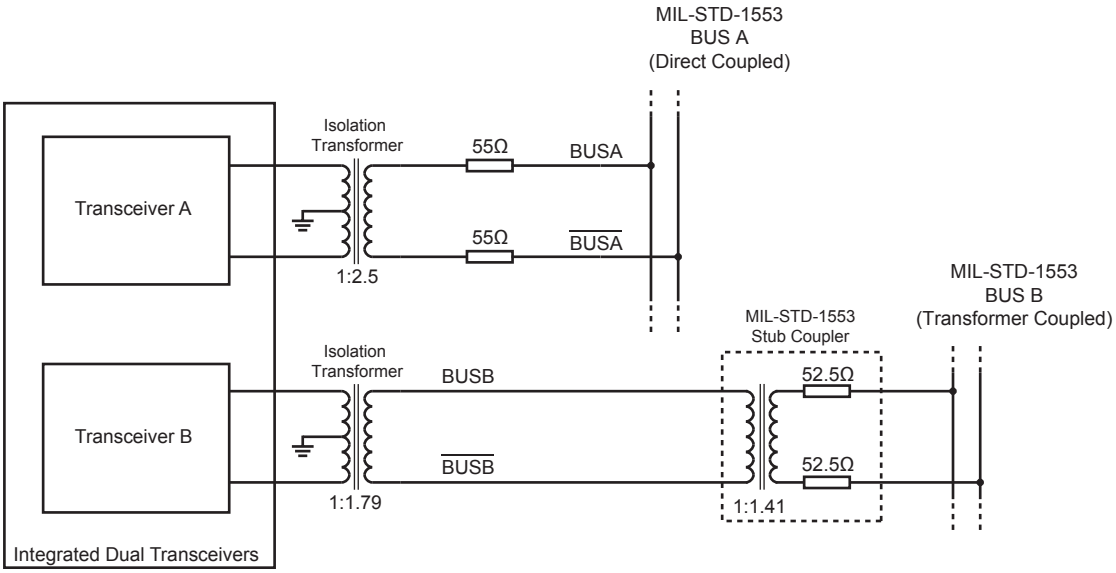


Figure 7. Bus Connection Example

6.5. MIL-STD-1553 Test Circuits

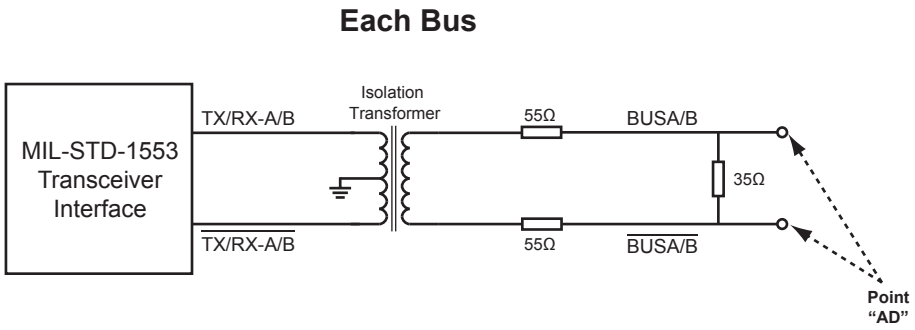


Figure 8. MIL-STD-1553 Direct Coupled Test Circuits

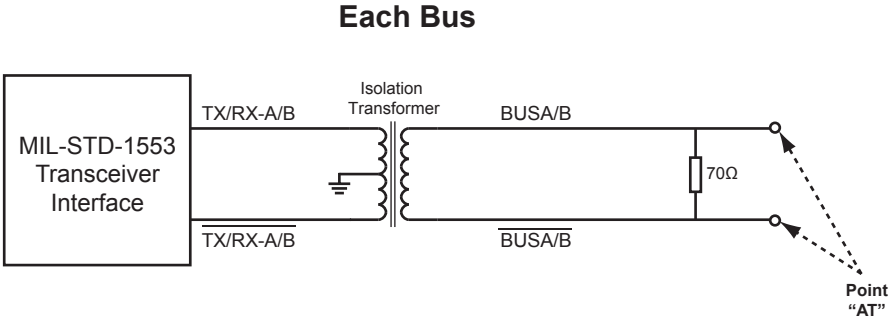


Figure 9. MIL-STD-1553 Transformer Coupled Test Circuits

7. PACKAGE DIMENSIONS

Bottom View

Dimensions: inches (mm)

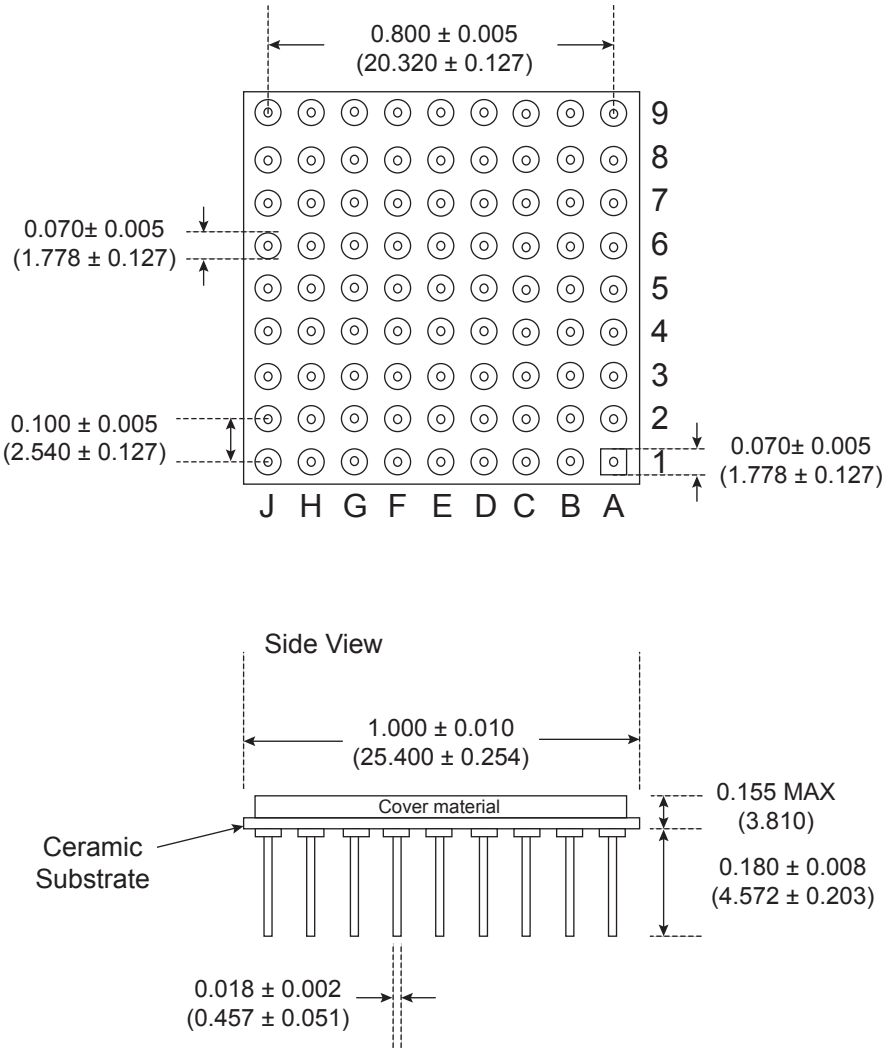


Figure 10. Pin Grid Array Package Dimensions (PGA-81)

Dimensions: inches (mm)

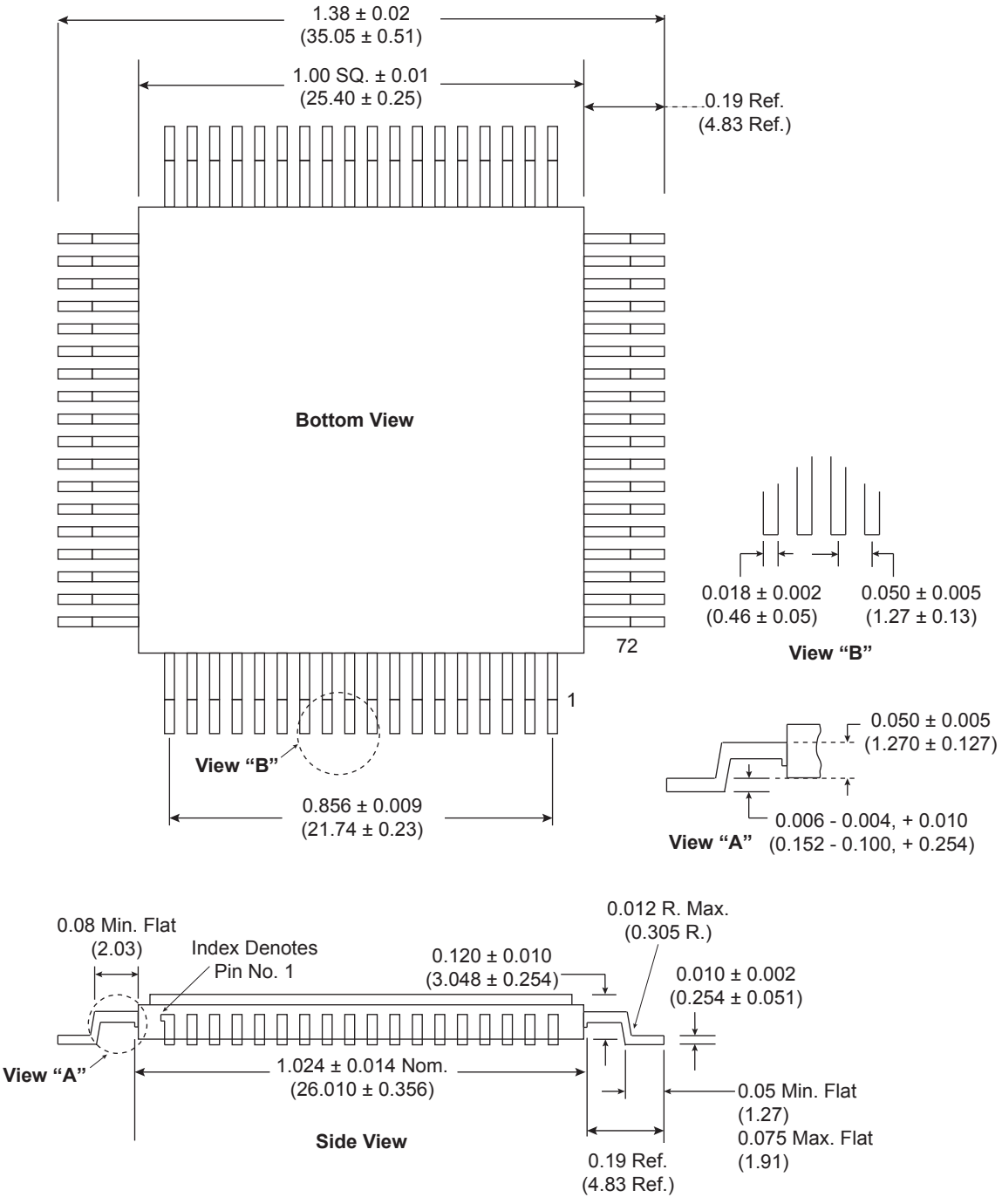


Figure 11. 72-Pin Gull Wing Package Dimensions

8. ORDERING INFORMATION

HI - 628 x x CP x x

- Blank = Leaded Pins (Solder dipped)
- F = RoHS compliant

- I = −40°C to +85°C
- T = −55°C to +125°C
- M = −55°C to +125°C with burn-in
- R = Same as M, MIL-PRF compliant
- D = Same as R, with PIND testing

- CP = Ceramic PGA-81

- 0 = No transceivers, digital-only[1]
- 5 = 5.0V Transceiver supply voltage

- 0 = BC/MT/RT, 64K x 17 bit word RAM capacity
- 1 = BC/MT/RT, 4K x 16 bit word RAM capacity
- 2 = RT only, 4K x 16 bit word RAM capacity
- 3 = RT only with MIL-STD-1760 Boot mode , 4K x 16 bit word RAM capacity

[1] Contact factory for availability.

HI - 628 x x CQ x x

- Blank = Leaded Pins (Solder dipped)
- F = RoHS compliant

- I = −40°C to +85°C
- T = −55°C to +125°C
- M = −55°C to +125°C with burn-in
- R = Same as M, MIL-PRF compliant
- D = Same as R, with PIND testing

- CQ = Ceramic 72-pin gull wing package

- 0 = No transceivers, digital-only[1]
- 5 = 5.0V Transceiver supply voltage

- 0 = BC/MT/RT, 64K x 17 bit word RAM capacity
- 1 = BC/MT/RT, 4K x 16 bit word RAM capacity
- 2 = RT only, 4K x 16 bit word RAM capacity
- 3 = RT only with MIL-STD-1760 Boot mode , 4K x 16 bit word RAM capacity

[1] Contact factory for availability.

9. REVISION HISTORY

Revision	Date	Description of Change
DS6280, Rev. New.	08/22/2023	Initial Release.