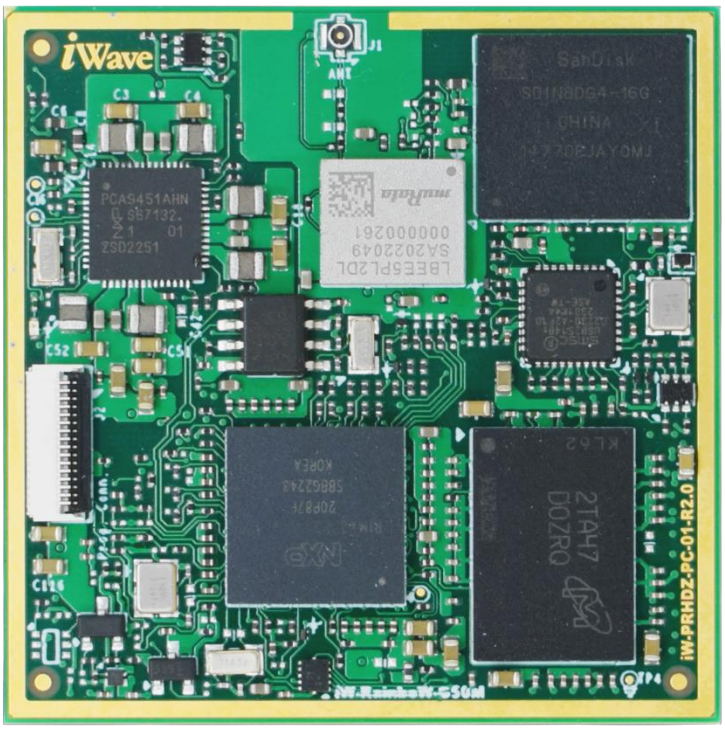
iW-RainboW-G50M
i.MX 93 or i.MX 91
OSM-LF LGA Module
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the NXP's i.MX 93 or i.MX 91 Application processor based OSM V1.1 specification compatible LGA module. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 93 or i.MX 91 OSM Module from a Hardware Systems perspective.

1.2 OSM LGA Module Overview

The OSM V1.1 ("Open Standard Modules™") is a future proof and versatile standard for small size, low-cost embedded computer modules. Combining the following key characteristics like completely machine processible during soldering, assembly and testing, Pre-tinned LGA package for direct PCB soldering without connector.

The OSM Module definition targeting application that requires low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 93 or i.MX 91 SoC based OSM LGA Module is rich with i.MX 93 or i.MX 91 features along with on SOM LPDDR4/4X, eMMC, Wi-Fi/BT module and comes in compact 45mm x 45mm form factor (Size L). The Module PCB has 662 contacts which can be mounted as LGA/BGA on OSM carrier card.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card

Acronyms	Abbreviations
EMS	Electronics manufacturing services
ESAI	Enhanced Serial Audio Interface
FLEXCAN	Flexible Control Area Network
FlexSPI	Flexible Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LVDS	Low Voltage Differential Signal
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface differential pair signals
OSM	Open Standard Module
OTG	On-The-Go
PCB	Printed Circuit Board
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SoC	System on Chip
SOM	System On Module
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
USB	Universal Serial Bus
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-OSM.

1.5 References

- IMX93IEC_Rev_x.pdf
- IMX91PEC_Revx
- i.MX93RM Rev_x.pdf
- OSM Specification V1.1

1.6 Important Note

In this document, wherever i.MX 93 or i.MX 91 SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.
- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 93 or i.MX 91 OSM LGA Module features and Hardware architecture with high level block diagram.

2.1 i.MX 93 or i.MX 91 OSM LGA Module Block Diagram

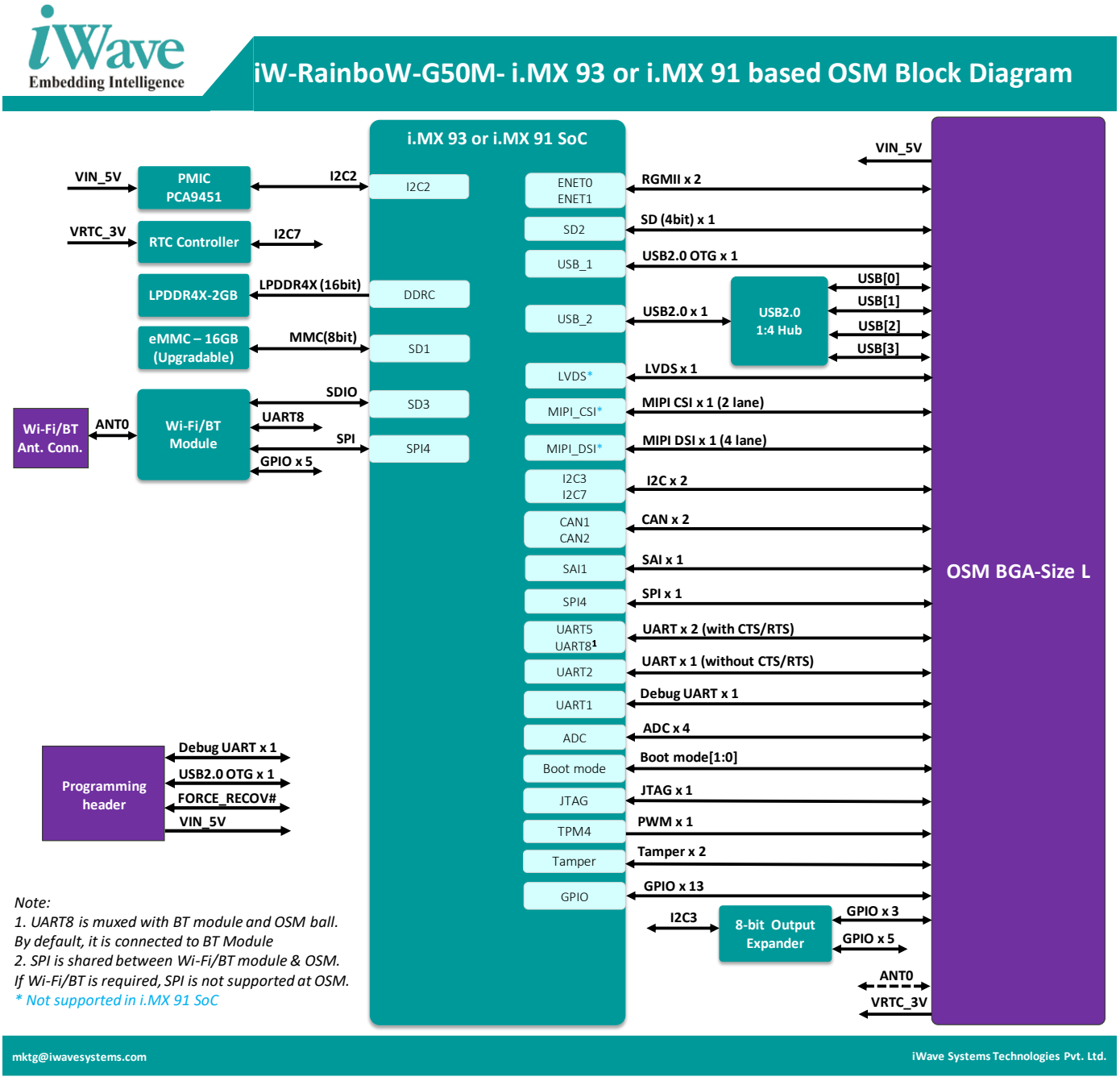

Figure 1: i.MX 93 or i.MX 91 OSM LGA MODULE Block Diagram

2.2 i.MX 93 or i.MX 91 SOM Features

i.MX 93 or i.MX 91 OSM LGA Module supports the following features.

SoC

- i.MX 93 Processor[1]
  - i.MX 9352: 2x Cortex®-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
  - i.MX 9351: 1 x Cortex-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
  - i.MX 9332: 2x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
  - i.MX 9331: 1x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 91 Processor
  - i.MX 91: 1x Cortex®-A55, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0

Power

- PCA9451 PMIC

Memory

- LPDDR4/4X - 2GB[2,3]
- eMMC Flash - 16GB (Expandable)[2]

Other On-SOM Features

- IEEE 802.11a/b/g/n/ac/ax+ Bluetooth 5.3+ IEEE802.15.4[4]
- USB2.0 1:4 Hub
- Programming Header

OSM LGA Interfaces

- RGMII x 2
- USB2.0 OTG x 1
- USB2.0 Host x 4
- SAI/I2S (Audio Interface) x 1
- SPI x 1[4]
- Data UART with flow control x 2 (1 is optional)[5]
- Data UART without flow control x 1
- Debug UART x 1
- GPIOs x 16

- MIPI_DSI(4lane) x 1*
- MIPI_CSI(2lane) x 1*
- SD (4 bit) x 1
- LVDS x 1*
- I2C x 2
- PWM x 1
- ADC x 4 (2 through Vendor defined pins)
- Tamper x 2 (through Vendor defined pins)

General Specification

- Power Supply : 5V, 2.5A
- Form Factor : 45mm X 45mm (OSM V1.1 Specification)

1. *There are four configurations of i.MX 93 Processor, hence this document is used to represent either of one based on SOM Part Number.*
2. *Memory Size will differ based on iWave's SOM Product Part Number.*
3. *i.MX 93 OSM supports LPDDR4X by default and i.MX 91 OSM supports LPDDR4.*
4. *SPI4 is shared between Wi-Fi/BT module to support IEEE802.15.4 and OSM. If Wi-Fi/BT is required, SPI is not supported at the OSM. If SPI is required at the OSM, Wi-Fi/BT module will be made DNP in the OSM.*
5. *UART8 is muxed with BT module and OSM. By default, it is connected to BT Module.*

** Not supported in i.MX 91 SoC.*

2.3 CPU

iW-RainboW-G50M i.MX 93 and i.MX 91 OSM LGA Module can support different i.MX 93 or i.MX 91 SoCs from NXP.

2.3.1 i.MX 93 CPU

The i.MX 93 (11 x 11 mm) Family consists of four processors.

- i.MX 9352: 2x Cortex®-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9351: 1 x Cortex-A55, NPU, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9332: 2x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM
- i.MX 9331: 1x Cortex®-A55, MIPI DSI, LVDS, MIPI CSI, Parallel camera, Parallel display, 2x Ethernet, 2x USB 2.0, 7x I2S TDM

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Memory interfaces supporting 16-bit LPDDR4 and LPDDR4X, eMMC 5.1, SD 3.0 and a wide range of peripheral IOs providing wide flexibility.

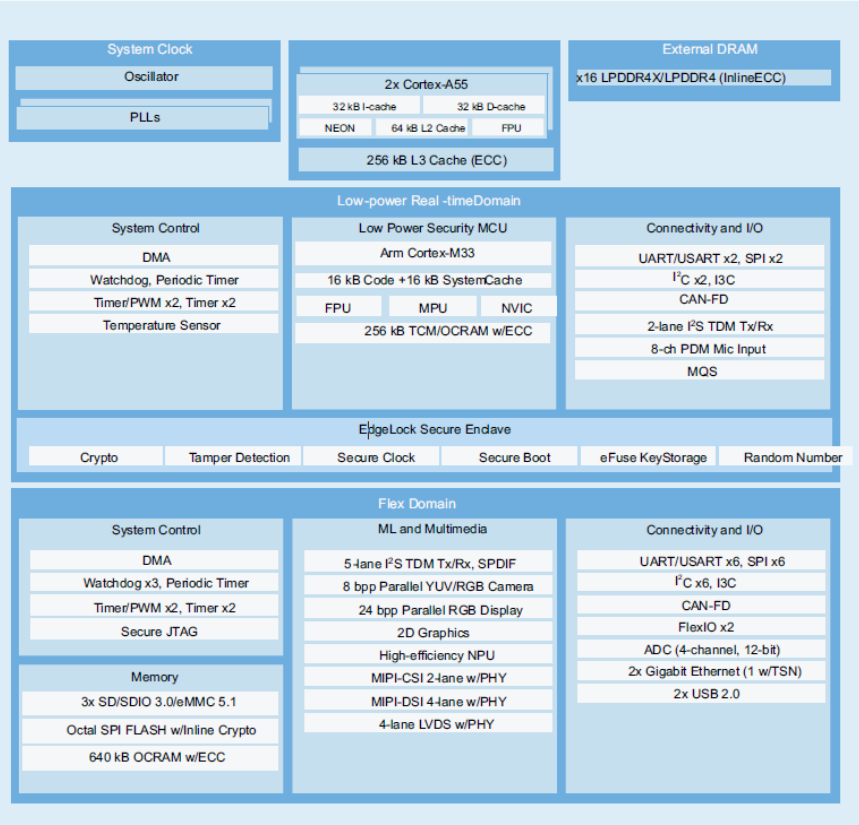

Figure 2: i.MX 93 SoC Block Diagram

2.3.2 i.MX 91 CPU

The i.MX 91 (11 x 11 mm) Family consists of two processors.

- i.MX 91P1C: Industrial Grade
- i.MX 91P1D: Consumer Grade

The i.MX 91 includes powerful single Arm® Cortex®-A55 processor with speeds up to 1.4 GHz. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, drive gateway applications with low latency. Memory interfaces supporting 16-bit LPDDR4, eMMC 5.1, SD 3.0 and a wide range of peripheral IOs providing wide flexibility.

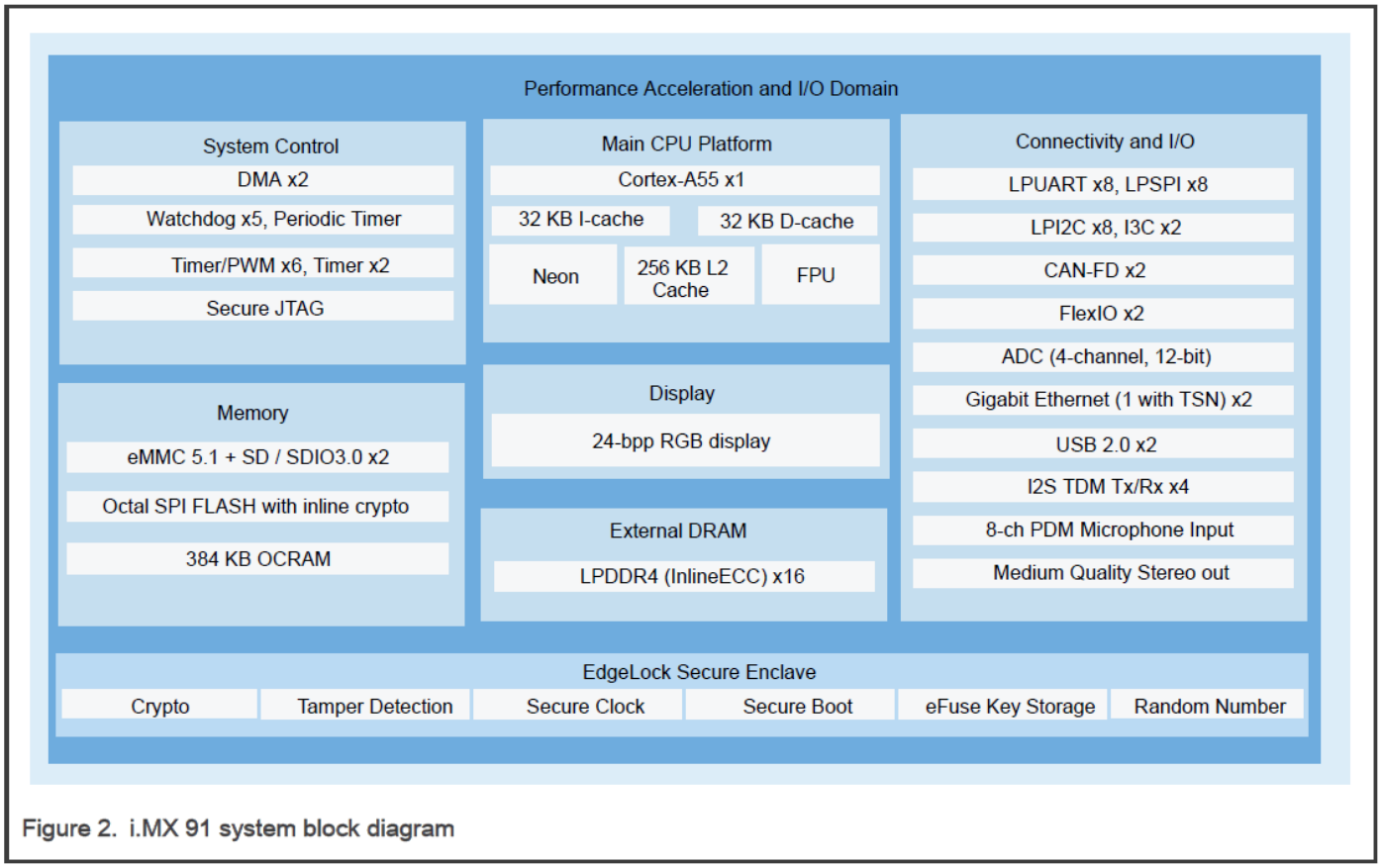

Figure 2. i.MX 91 system block diagram

Figure 3: i.MX 91 SoC Block Diagram

Note: The i.MX 93 and i.MX 91 processor offers numerous advanced features, please refer the latest i.MX 93 or i.MX 91 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PCA9451 PMIC

The i.MX 93 or i.MX 91 OSM LGA Module uses one PCA9451 PMIC (U4) for module power management. The PCA9451 features six high efficiency step-down regulators and three linear regulators. The PCA9451 is a single chip Power Management IC (PMIC) specifically designed to support i.MX 93x family processor in both 1 cell Li-Ion and Li-polymer battery portable application and 5V adapter non-portable applications. Regulator parameters are adjustable through high-speed I2C after start up offering flexibility for different system states. The PCA9451 PMIC comes in 56-pin HVQFN package.

2.5 Memory

2.5.1 LPDDR4X/LPDDR4

The i.MX 93 or i.MX 91 OSM LGA Module supports 2GB LPDDR4X/LPDDR4 memory by using 16bit DDR_CH0 channel of the SoC. By default, LPDDR4X is supported in i.MX 93 OSM. The i.MX 91 SoC supports only LPDDR4. To customize the LPDDR4X/LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX 93 or i.MX 91 OSM LGA Module supports 16GB eMMC as default boot and storage device. This is directly connected to eMMC controller of the i.MX 93 or i.MX 91 SoC and operates at 1.8V (IO supply) and 3.3V (NAND core supply) Voltage levels. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.6 Network & Communications features

2.6.1 Wi-Fi and Bluetooth Interface

The i.MX 93 or i.MX 91 OSM LGA Module is integrated with Murata's "LBES5PL2EL-SMP" based Wi-Fi+Bluetooth module. LBES5PL2EL-SMP module is complaint with IEEE802.11a/b/g/n/ac/ax, SISO, Bluetooth specification v5.3 and IEEE802.15.4. It supports standard SDIO3.0 interface for WLAN, UART interfaces support for Bluetooth is Host Controller Interface (HCI) and SPI interface to optionally support IEEE802.15.4. Connection to a host processor is through SDIO, High-Speed UART interfaces and SPI. The i.MX 93 OSM LGA Module uses processor's UART8 interface for Bluetooth and SD3 interface for Wi-Fi in a default configuration. In the OSM LGA module, antenna pins of LBES5PL2EL-SMP Bluetooth and Wi-Fi is connected to J1 connector and optionally connected to A16th pin of OSM.

Note: SPI4 is shared between Wi-Fi/BT module to support IEEE802.15.4 and OSM. If Wi-Fi/BT is required, SPI is not supported at the OSM. If SPI is required at the OSM, Wi-Fi/BT module will be made DNP in the OSM.

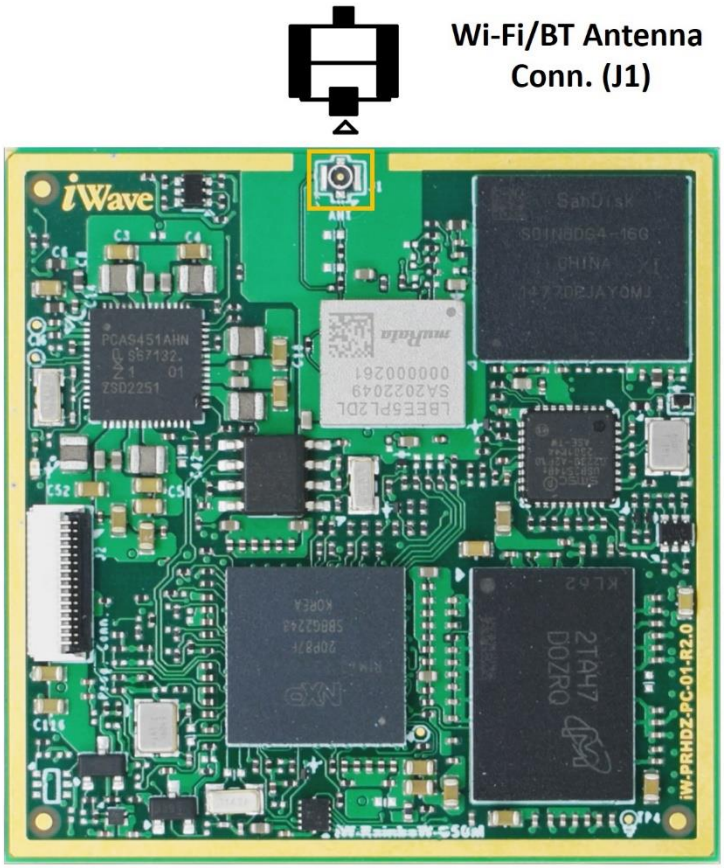

Figure 4: Wi-Fi+Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata.

Antenna Part Number - : 2042811100 from Molex

2.6.2 RTC Controller

The i.MX 93 and i.MX 91 OSM LGA Module by supports external RTC Controller “PCF85263” On-SOM for Real time clock support. This external RTC Controller IC (U6) is connected to i.MX 93 SoC through I2C7 Interface and operates at 1.8V voltage level. In SOM power off condition, this device will take power from OSM pin No. W17 (RTC_PWR) coin cell power input and continues to keep the current time.

Note: RTC cannot be used as wake-up source, as a result RTC alarm won't work.

2.7 OSM LGA/BGA

OSM LGA/BGA (J3) has standard pinout as per OSM Specification V1.1 The interfaces which are available at 662 contacts are explained in the following sections.

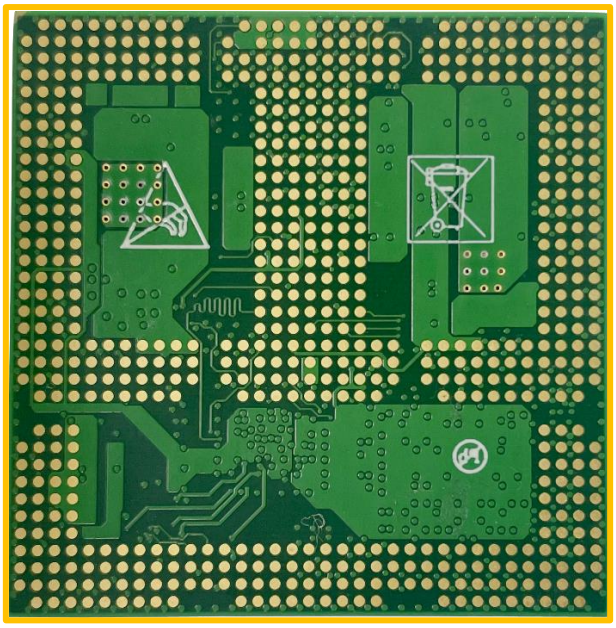

Figure 5: OSM LGA/BGA

Number of contacts - : 662

Table 3: OSM Pinouts

OSM Pins	Signal
SIZE 0	
M18	ADC_IN0
N18	ADC_IN1
U19	BOOT_SEL0#
R18	UART2_TXD(BOOT_MODE1)
AB17	CAN1_RX(PDM_BIT0)
AC17	CAN1_TX(PDM_CLK)
AB19	CAN2_RX(GPIO_IO27)
AC19	CAN2_TX(GPIO_IO25)
V17	CARRIER_PWR_ON
A15	GND
A16	OSM_ANT0
A17	GND
A18	GND
A19	GND
A20	NC
A21	GND
B15	GND
B16	GND
B17	GND
B18	GND
B19	GND
B20	GND
B21	GND
C15	NC
C17	NC
C19	NC
C21	NC
AC18	NC
F15	NC
E16	NC
R15	ENET1_QOS_RGMII_RXC
M15	ENET1_QOS_RGMII_RX_CTL
L16	NC
N15	ENET1_QOS_RGMII_RD2
P15	ENET1_QOS_RGMII_RD3
J15	ENET1_QOS_RGMII_TXC
K16	ENET1_QOS_RGMII_TX_CTL
K15	ENET1_QOS_RGMII_RD0
L15	ENET1_QOS_RGMII_RD1

OSM Pins	Signal
H15	ENET1_QOS_RGMII_TD0
G15	ENET1_QOS_RGMII_TD1
H16	ENET1_QOS_RGMII_TD2
G16	ENET1_QOS_RGMII_TD3
N16	NC
M17	VDD_1V8
T16	ENET1_QOS_MDC
T15	ENET1_QOS_MDIO
T17	FORCE_RECOV#
F16	GND
J16	GND
J20	GND
E21	GND
E15	GND
M16	GND
M20	GND
P18	GND
R16	GND
R20	GND
V16	GND
V20	GND
Y18	GND
AA14	GND
AA17	GND
AA19	GND
AA22	GND
AB15	GND
AB21	GND
D18	GND
L18	GND
F20	GND
D17	OSM_GPIO_A0(GPIO1_IO01_I3C1_SDA)
E17	OSM_GPIO_A1(SPI3_MISO_GPIO_IO09)
F17	OSM_GPIO_A2(SPI3_MOSI_GPIO_IO10)
G17	OSM_GPIO_A3(SPI3_SS0_GPIO_IO08)
H17	OSM_GPIO_A4(SPI3_SCLK_GPIO_IO11)
J17	OSM_GPIO_A5(GPIO1_IO00_I3C1_SCL)
K17	OSM_GPIO_A6(IO_5)
L17	OSM_GPIO_A7(GPIO4_IO29_CCM_CLKO4)
D19	OSM_GPIO_B0(GPIO4_IO28_CCM_CLKO3)
E19	OSM_GPIO_B1(GPIO_IO16)

OSM Pins	Signal
F19	OSM_GPIO_B2(GPIO_IO17)
G19	NC
H19	NC
J19	OSM_GPIO_B5(GPIO_IO26)
K19	NC
L19	NC
AA15	I2C7_SCL(GPIO_IO07)
AA16	I2C7_SDA(GPIO_IO06)
AA20	I2C3_SCL(GPIO_IO29)
AA21	I2C3_SDA(GPIO_IO28)
V21	SAI1_RX_DATA0
W21	SAI1_TXD0(BOOT_MODE3)
V19	NC
W19	NC
W20	SAI1_TXCLK
W18	SAI1_TXFS(BOOT_MODE2)
V18	NC
R19	JTAG_NTRST
P19	NC
N17	GPIO3_IO30(JTAG_TCK)
P17	GPIO3_IO28(JTAG_TDI)
R17	GPIO3_IO31(JTAG_TDO)
N19	GPIO3_IO29(JTAG_TMS)
E18	NC
F18	NC
G18	NC
H18	NC
J18	NC
K18	NC
T18	NC
T19	NC
Y13	NC
Y14	NC
AA13	NC
W17	VRTC_3V0
J21	SD2_CD_B
F21	SD2_CLK
E20	SD2_CMD
G20	SD2_DATA0
G21	SD2_DATA1
H20	SD2_DATA2

OSM Pins	Signal
H21	SD2_DATA3
C20	NVCC_SD2
D21	GPIO3_IO7(SD2_RESET_B)
D20	NC
T21	NC
K20	NC
K21	NC
L20	NC
L21	NC
M21	NC
N20	NC
N21	NC
P20	NC
P21	NC
R21	NC
T20	SDIO_B_IOPWR
U21	NC
U20	NC
W15	NC
W16	NC
Y15	SPI4_SSO(GPIO_IO18)
U16	SPI4_SCK(GPIO_IO21)
U15	SPI4_MISO(GPIO_IO19)
V15	SPI4_MOSI(GPIO_IO20)
AA23	NC
Y21	NC
Y22	NC
Y23	NC
U17	PMIC_RST_B
C18	NC
C14	UART5_CTS(GPIO_IO02)
C13	UART5_RTS(GPIO_IO03)
A14	UART5_RXD(GPIO_IO01)
B13	UART5_TXD(GPIO_IO00)
D16	UART8_CTS
D15	UART8_RTS
D14	UART8_RXD
D13	UART8_TXD
A22	UART2_RXD
B23	UART2_TXD(BOOT_MODE1)
D22	UART1_RXD

OSM Pins	Signal
D23	UART1_TXD(BOOT_MODE0)
C22	NC
C23	NC
AB13	USB_OTG1_DM
AC14	USB_OTG1_DP
AC16	NC
AB14	USB_OTG1_ID
AC15	NC
AB16	OTG1_VBUS
AB23	USB_HUB1OUT_DM
AC22	USB_HUB1OUT_DP
AC20	OSM_USB_B_PWR_EN
AB22	USB_B_ID
AC21	OSM_USB_B_OC
AB20	USB_B_VBUS
AB18	V_BAT
AA18	V_BAT
M19	VDD_3V3
Y16	NVCC_SD2
Y20	VDD_SOC_0V8
Y19	VCC_IN_3V3
Y17	VCC_IN_5V
U18	VCC_OUT_IO
B22	PMIC_ON_REQ
C16	ADC_IN2
P16	ADC_IN3
SIZE S	
C2	NC
G3	CAM_PWR_EN(GPIO_IO24)
G4	CAM_RST(GPIO_IO23)
B3	MIPI_CSI1_CLK_N*
B4	MIPI_CSI1_CLK_P*
C1	MIPI_CSI1_D0_N*
B1	MIPI_CSI1_D0_P*
A2	MIPI_CSI1_D1_N*
A3	MIPI_CSI1_D1_P*
A5	NC
A6	NC
B6	NC
B7	NC
AB8	MIPI_DSI1_CLK_N*

OSM Pins	Signal
AB7	MIPI_DSI1_CLK_P*
AB11	MIPI_DSI1_D0_N*
AB10	MIPI_DSI1_D0_P*
AC9	MIPI_DSI1_D1_N*
AC8	MIPI_DSI1_D1_P*
AC6	MIPI_DSI1_D2_N*
AC5	MIPI_DSI1_D2_P*
AB5	MIPI_DSI1_D3_N*
AB4	MIPI_DSI1_D3_P*
AA3	NC
E1	NC
D2	NC
P1	ENET2_RGMII_RXC
L1	ENET2_RGMII_RX_CTL
K2	NC
M1	ENET2_RGMII_RD2
N1	ENET2_RGMII_RD3
H1	ENET2_RGMII_TXC
J2	ENET2_RGMII_TX_CTL
J1	ENET2_RGMII_RD0
K1	ENET2_RGMII_RD1
G1	ENET2_RGMII_TD0
F1	ENET2_RGMII_TD1
G2	ENET2_RGMII_TD2
F2	ENET2_RGMII_TD3
C6	ENET2_MDC
C7	ENET2_MDIO
M2	NC
B5	GND
D8	GND
P4	GND
AC10	GND
AC7	GND
AC4	GND
AB9	GND
AB6	GND
AB3	GND
AA11	GND
AA10	GND
AA8	GND
A4	GND

OSM Pins	Signal
A7	GND
A10	GND
B2	GND
B8	GND
B9	GND
C11	GND
D1	GND
D5	GND
E2	GND
H2	GND
H4	GND
L2	GND
L4	GND
P2	GND
U2	GND
U4	GND
V1	GND
W3	GND
Y2	GND
AA1	GND
AA4	GND
AA7	GND
R1	GND
D3	NC
D4	NC
E3	NC
E4	NC
F3	OSM_GPIO_C4(GPIO_IO22)
F4	GPIO2_IO4(GPIO_IO04)
C4	I2C7_SCL(GPIO_IO07)
C3	I2C7_SDA(GPIO_IO06)
AB2	NC
AB1	NC
AC3	NC
AC2	NC
V2	NC
W2	NC
Y1	NC
W1	NC
R2	NC
T1	NC

OSM Pins	Signal
U1	NC
T2	NC
AA9	CPU_ON_OFF
M4	NC
R4	NC
R3	NC
P3	NC
N3	NC
N4	NC
M3	NC
H3	NC
J4	NC
K4	NC
W4	NC
V3	NC
V4	NC
U3	NC
T3	NC
T4	NC
K3	NC
Y7	NC
AA6	NC
Y6	NC
AA5	NC
Y5	NC
Y4	NC
J3	NC
L3	NC
AA2	NC
N2	NC
D11	USB_HUB2OUT_DM
D10	USB_HUB2OUT_DP
C10	OSM_USBC_PWR_EN
D9	USB_C_ID
C8	OSMC_USB_OC
B11	NC
B10	NC
A9	NC
A8	NC
C9	NC
Y3	VCC_5_TEST

OSM Pins	Signal
C5	VCC_6_TEST
Y11	VCC_IN_5V
Y10	VCC_IN_5V
Y9	VCC_IN_5V
Y8	VCC_IN_5V
D6	TAMPER0
D7	TAMPER1
SIZE M	
C34	NC
C33	NC
D32	NC
D31	NC
D33	NC
C31	NC
A31	NC
A30	NC
B32	NC
B31	NC
A34	NC
A33	NC
B35	NC
B34	NC
H33	NC
G33	NC
F32	NC
E32	NC
G32	NC
E33	NC
E35	NC
D35	NC
F34	NC
E34	NC
H35	NC
G35	NC
J34	NC
H34	NC
AB35	NC
AC34	NC
W35	NC
T35	NC
U34	NC

OSM Pins	Signal
R35	NC
P35	NC
N35	NC
V34	NC
V35	NC
U35	NC
Y35	NC
AA35	NC
Y34	NC
AA34	NC
R34	NC
N33	NC
P33	NC
A26	GND
J33	GND
AC30	GND
AC33	GND
H32	GND
G34	GND
F35	GND
F33	GND
D34	GND
D28	GND
C35	GND
C32	GND
AC27	GND
AB34	GND
AB31	GND
AB28	GND
AA32	GND
AA28	GND
AA27	GND
AA26	GND
AA25	GND
W34	GND
T34	GND
N34	GND
M35	GND
K34	GND
C25	GND
A29	GND

OSM Pins	Signal
A32	GND
B27	GND
B28	GND
B30	GND
B33	GND
J35	GND
U32	NC
U33	NC
V32	NC
V33	NC
W32	NC
W33	NC
Y32	NC
Y33	NC
M34	NC
L34	NC
L35	NC
K35	NC
L33	NC
K33	NC
J32	NC
K32	NC
L32	NC
M32	NC
M33	NC
N32	NC
P32	NC
P34	NC
R32	NC
R33	NC
T32	NC
T33	NC
AB25	NC
AB26	NC
C30	NC
D29	NC
C29	NC
D30	NC
AC26	NC
AB27	NC
AC32	NC

OSM Pins	Signal
AC31	NC
AB33	NC
AB32	NC
AC29	NC
AC28	NC
AB30	NC
AB29	NC
D26	USB_HUB3OUT_DM
D25	USB_HUB3OUT_DP
C26	OSM_USBD_PWR_EN
D27	USB_D_ID
C28	OSM_USB_D_OC
B26	NC
B25	NC
A28	NC
A27	NC
C27	NC
AA33	NC
B29	NC
Y25	VCC_IN_5V
Y28	VCC_IN_5V
Y27	VCC_IN_5V
Y26	VCC_IN_5V
Y29	USB_HUB4OUT_DP
Y30	NC
Y31	NC
AA29	USB_HUB4OUT_DM
AA30	NC
AA31	NC
SIZE L	
AF3	NC
AE3	NC
AP1	NC
AL1	NC
AK2	NC
AM1	NC
AN1	NC
AH1	NC
AJ2	NC
AJ1	NC
AK1	NC

OSM Pins	Signal
AF1	NC
AG1	NC
AG2	NC
AF2	NC
AM2	NC
AR2	NC
AN4	NC
AN10	NC
AR8	NC
AP7	NC
AR9	NC
AR10	NC
AR5	NC
AP6	NC
AP3	NC
AP4	NC
AR6	NC
AR7	NC
AR3	NC
AR4	NC
AP9	NC
AP25	GND
AP28	GND
AP31	GND
AP34	GND
AR14	GND
AP19	GND
AR20	GND
AR26	GND
AR29	GND
AR32	GND
AP22	GND
AP16	GND
AE2	GND
AP13	GND
AP8	GND
AE34	GND
AP5	GND
AP2	GND
AN33	GND
AN21	GND

OSM Pins	Signal
AN18	GND
AR17	GND
AN15	GND
AF35	GND
AG3	GND
AH2	GND
AH34	GND
AJ35	GND
AK3	GND
AL2	GND
AL34	GND
AM13	GND
AM16	GND
AM19	GND
AM22	GND
AN11	GND
AN9	GND
AN6	GND
AN3	GND
AM35	GND
AF32	NC
AF33	NC
AG32	NC
AG33	NC
AH32	NC
AH33	NC
AJ32	NC
AJ33	NC
AN12	LVDS0_CLK_N*
AN13	LVDS0_CLK_P*
AP17	LVDS0_D0_N*
AP18	LVDS0_D0_P*
AR15	LVDS0_D1_N*
AR16	LVDS0_D1_P*
AP14	LVDS0_D2_N*
AP15	LVDS0_D2_P*
AP11	LVDS0_D3_N*
AP12	LVDS0_D3_P*
AN16	NC
AN17	NC
AM20	NC

OSM Pins	Signal
AM21	NC
AN19	NC
AN20	NC
AM17	NC
AM18	NC
AM14	NC
AM15	NC
AN23	LVDS_BL_EN(IO_07)
AN22	TPM4(GPIO_IO05)
AM11	I2C3_SCL(GPIO_IO29)
AM12	I2C3_SDA(GPIO_IO28)
AN14	NC
AP32	NC
AP33	NC
AP35	NC
AN35	NC
AL35	NC
AK35	NC
AH35	NC
AG35	NC
AR33	NC
AR34	NC
AN34	NC
AM34	NC
AK34	NC
AJ34	NC
AG34	NC
AF34	NC
AE33	NC
AR18	NC
AR19	NC
AR21	NC
AR22	NC
AP26	NC
AP27	NC
AP29	NC
AP30	NC
AP20	NC
AP21	NC
AP23	NC
AP24	NC

OSM Pins	Signal
AR27	NC
AR28	NC
AR30	NC
AR31	NC
AN32	NC
AL3	NC
AL4	NC
AM3	NC
AM4	NC
AM5	NC
AM6	NC
AM7	NC
AM8	NC
AM9	NC
AM10	NC
AM23	NC
AM24	NC
AM25	NC
AM26	NC
AM27	NC
AM28	NC
AM29	NC
AM30	NC
AM31	NC
AN2	NC
AN5	NC
AN7	NC
AN8	NC
AN24	NC
AN25	NC
AN26	NC
AN27	NC
AN28	NC
AN29	NC
AN30	NC
AP10	NC
AN31	NC
AE32	NC
AE4	VCC_IN_5V
AF4	VCC_IN_5V
AG4	VCC_IN_5V

OSM Pins	Signal
AH3	VCC_IN_5V
AH4	VCC_IN_5V
AJ3	VCC_IN_5V
AJ4	VCC_IN_5V
AK4	VCC_IN_5V
AK32	NC
AK33	NC
AL32	NC
AL33	NC
AM32	NC
AM33	NC

** Not supported in i.MX 91 SoC.*

2.7.1 RGMII Interface

The i.MX 93 and i.MX 91 OSM LGA Module supports 2 RGMII interface and are connected OSM LGA. i.MX 93 and i.MX 91 provides two Ethernet Interfaces ENET1 with TSN in addition to AVB and ENET2 with AVB support. Connection of the i.MX 93 to the world wide web or a local area network (LAN) is possible using the GbE PHY which is off the module. The PHY can be selected which operates with a data transmission speed of 10 Mbit/s, 100 Mbit/s, or 1000 Mbit/s.

For more details on ENET1 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
H15	ETH_A_(S)(R)(G)MII_TXD0	ENET1_QOS_RGMII_TD0	ENET1_TD0/ W11	O, 1.8V CMOS/0E	Transmit data bit 0 (transmitted first) port A
G15	ETH_A_(S)(R)(G)MII_TXD1	ENET1_QOS_RGMII_TD1	ENET1_TD1/T12	O, 1.8V CMOS/0E	Transmit data bit 1 port A
H16	ETH_A_(S)(R)(G)MII_TXD2	ENET1_QOS_RGMII_TD2	ENET1_TD2/ U12	O, 1.8V CMOS/0E	Transmit data bit 2 port A
G16	ETH_A_(S)(R)(G)MII_TXD3	ENET1_QOS_RGMII_TD3	ENET1_TD3/V12	O, 1.8V CMOS/0E	Transmit data bit 3 port A
K16	ETH_A_(R)(G)MII_TX_EN(_ER)	ENET1_QOS_RGMII_TX_CTL	ENET1_TX_CTL/V10	O, 1.8V CMOS/0E	Transmit enable (Error) port A
J15	ETH_A_(R)(G)MII_TX_CLK	ENET1_QOS_RGMII_TXC	ENET1_TXC/ U10	O, 1.8V CMOS/0E	Transmit clock port A
K15	ETH_A_(S)(R)(G)MII_RXD0	ENET1_QOS_RGMII_RD0	ENET1_RD0/AA8	I, 1.8V CMOS	Receive data bit 0 (received first) port A
L15	ETH_A_(S)(R)(G)MII_RXD1	ENET1_QOS_RGMII_RD1	ENET1_RD1/ Y9	I, 1.8V CMOS	Receive data bit 1 port A
N15	ETH_A_(R)(G)MII_RXD2	ENET1_QOS_RGMII_RD2	ENET1_RD2/ AA9	I, 1.8V CMOS	Receive data bit 2 port A
P15	ETH_A_(R)(G)MII_RXD3	ENET1_QOS_RGMII_RD3	ENET1_RD3/ Y10	I, 1.8V CMOS	Receive data bit 3 port A
M15	ETH_A_(R)(G)MII_RX_DV(_ER)	ENET1_QOS_RGMII_RX_CTL	ENET1_RX_CTL/Y8	I, 1.8V CMOS	Receive data valid port A
R15	ETH_A_(R)(G)MII_RX_CLK	ENET1_QOS_RGMII_RXC	ENET1_RXC/AA7	I,1.8V CMOS	Receive clock port A

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
T15	ETH_MDIO	ENET1_QOS_MDIO	ENET1_MDIO/AA10	IO, 1.8V CMOS	Management data IO for Port A
T16	ETH_MDC	ENET1_QOS_MDC	ENET1_MDC/AA11	O, 1.8V CMOS/0E	Management data clock for Port A
M17	ETH_IOPWR	-	-	P, 1V8	ETH voltage. It is used to provide the IO Voltage Level for all Ethernet interfaces.

For more details on ENET2 pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G1	ETH_B_(S)(R)(G)MII_TXD0	ENET2_RGMII_TD0	ENET2_TD0/T8	O, 1.8V CMOS/0E	Transmit data bit 0 port B
F1	ETH_B_(S)(R)(G)MII_TXD1	ENET2_RGMII_TD1	ENET2_TD1/U8	O, 1.8V CMOS/0E	Transmit data bit 1 port B
G2	ETH_B_(S)(R)(G)MII_TXD2	ENET2_RGMII_TD2	ENET2_TD2/V8	O, 1.8V CMOS/0E	Transmit data bit 2 port B
F2	ETH_B_(S)(R)(G)MII_TXD3	ENET2_RGMII_TD3	ENET2_TD3/T10	O, 1.8V CMOS/0E	Transmit data bit 3 port B
J2	ETH_B_(R)(G)MII_TX_EN(_ER)	ENET2_RGMII_TX_CTL	ENET2_TX_CTL/V6	O, 1.8V CMOS/0E	Transmit enable (Error) port B
H1	ETH_B_(R)(G)MII_TX_CLK	ENET2_RGMII_TXC	ENET2_TXC/U6	O,1V8 CMOS/0E	Transmit clock port B
J1	ETH_B_(S)(R)(G)MII_RXD0	ENET2_RGMII_RD0	ENET2_RX0/AA4	I, 1.8V CMOS	Receive data bit 0 (received first) port B
K1	ETH_B_(S)(R)(G)MII_RXD1	ENET2_RGMII_RD1	ENET2_RX1/Y5	I, 1.8V CMOS	Receive data bit 1 port B
M1	ETH_B_(R)(G)MII_RXD2	ENET2_RGMII_RD2	ENET2_RX2/AA5	I, 1.8V CMOS	Receive data bit 2 port B
N1	ETH_B_(R)(G)MII_RXD3	ENET2_RGMII_RD3	ENET2_RX3/Y6	I, 1.8V CMOS	Receive data bit 3 port B

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
L1	ETH_B_(R)(G)MII_RX_DV(_ER)	ENET2_RGMII_RX_CTL	ENET2_RX_CTL/Y4	I, 1.8V CMOS	Receive data valid port B
P1	ETH_B_(R)(G)MII_RX_CLK	ENET2_RGMII_RXC	ENET2_RXC/AA3	I 1.8V CMOS	Receive clock port B
C7	ETH_B_MDIO	ENET2_MDIO	ENET2_MDIO/AA6	IO, 1.8V CMOS	Management data IO for Port B
C6	ETH_B_MDC	ENET2_MDC	ENET2_MDC/Y7	O, 1.8V CMOS/0E	Management data clock for Port B

2.7.2 USB 2.0 OTG Interface

The i.MX 93 or i.MX 91 OSM LGA Module supports one USB2.0 OTG interface and one USB2.0 Host. The SoC's USB OTG controller supports two independent USB core and includes the PHY and IO interfaces to support this operation. It supports High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps). It is fully compatible with the USB On-The-Go supplement to the USB 2.0 specification.

For more details on USB 2.0 OTG pinouts on OSM LGA, refer the below table:

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB13	USB_A_D_N	OSM_USBA_OTG1_DM	USB1_D_N/A14	IO, USB	USB2.0 PortA Data Negative.
AC14	USB_A_D_P	OSM_USBA_OTG1_DP	USB1_D_P/B14	IO, USB	USB2.0 PortA Data Positive.
AB14	USB_A_ID	USB_OTG1_ID	USB1_ID/C11	I, 1.8V CMOS	USB OTG ID.
AC15	USB_A_OC#	OSMA_USB_OC	-	I, 1.8V CMOS/ 10K PU	USB2.0 PortA Over Current Indicator.
AB16	USB_A_VBUS	OTG1_VBUS	USB1_VBUS/F12	I USB VBUS 5V	USB PortA power detection. *Note: Same power is also connected to 1Othpin of Programming Header*

2.7.3 USB 2.0 Host Interface

For more details on USB 2.0 Host pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB23	USB_B_D_N	USB_HUB1OUT_DM	-	IO, USB	USB2.0 PortB Data Negative. *Note: This pin is connected to USB Hub.*
AC22	USB_B_D_P	USB_HUB1OUT_DP	-	IO, USB	USB2.0 PortB Data Positive. *Note: This pin is connected to USB Hub.*
AB22	USB_B_ID	USB_B_ID	-	I, 1.8V CMOS/ 10K PU	USB OTG ID.
AC21	USB_B_OC#	OSM_USB_B_OC	-	I, 1.8V CMOS/ 10K PU	USB2.0 PortB Over Current Indicator.
AC20	USB_B_EN	OSM_USB_B_PWR_EN	-	O, 1.8V CMOS	USB Power Enable. *Note: This pin is connected to USB Hub.*
D11	USB_C_D_N	OSM_USBC_OTG1_DM	-	IO USB	USB2.0 PortC Data Negative *Note: This pin is connected to USB Hub.*
D10	USB_C_D_P	OSM_USBC_OTG1_DP	-	IO USB	USB2.0 PortC Data Positive *Note: This pin is connected to USB Hub.*
D9	USB_C_ID	OSM_USB_OTG1_ID	-	I, 1.8V CMOS/ 10K PU	USB OTG ID.
C8	USB_C_OC#	OSMC_USB_OC	-	I, 1.8V CMOS/ 10K PU	USB2.0 PortC Over Current Indicator.
C10	USB_C_EN	OSM_USBC_PWR_EN	-	O, 1.8V CMOS	USB Power Enable. *Note: This pin is connected to USB Hub.*
Y29	Vendor Defined8	USB_HUB4OUT_DP	-	IO USB	USB2.0 Data Negative *Note: This pin is connected to USB Hub.*
AA29	Vendor Defined11	USB_HUB4OUT_DM	-	IO USB	USB2.0 Data Positive

Pin No.	OSM Pin Name	OSM Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: This pin is connected to USB Hub.
D26	USB_D_D_N	USB_HUB3OUT_DM	-	IO USB	USB2.0 PortD Data Negative *Note: This pin is connected to USB Hub.*
D25	USB_D_D_P	USB_HUB3OUT_DP	-	IO USB	USB2.0 PortD Data Positive *Note: This pin is connected to USB Hub.*
D27	USB_D_ID	USB_D_ID	-	I, 1.8V CMOS/ 10K PU	USB OTG ID.
C28	USB_D_OC#	OSM_USB_D_OC	-	I, 1.8V CMOS/ 10K PU	USB2.0 PortD Over Current Indicator.
C26	USB_D_EN	OSM_USBD_PWR_EN	-	O, 1.8V CMOS	USB Power Enable. *Note: This pin is connected to USB Hub.*

2.7.4 Audio Interface

The i.MX 93 or i.MX 91 OSM LGA Module supports I2S_A of OSM LGA ball from SoC's SAI1 channel. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97, TDM and other audio codec/DSP interfaces. The SAI general feature includes Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits.

In i.MX 93 or i.MX 91 OSM LGA Module the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
W18	I2S_LRCLK	SAI1_TXFS(BOOT_MODE2)	SAI1_TXFS/ G21	IO, 1.8V CMOS, 100K PD	Serial Audio Interface Frame Sync. *Note: This signal is also used as BOOT_MODE2.*
W20	I2S_BITCLK	SAI1_TXCLK	SAI1_TXC/ G20	O, 1.8V CMOS/33E	Digital audio clock
V21	I2S_A_DATA_IN	SAI1_RX_DATA0	SAI1_RXD0/ H20	O, 1.8V CMOS	Digital audio Input

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
W21	I2S_A_DATA_OUT	SAI1_TXD0(BOOT_ MODE3)	SAI1_TXD0/ H21	O, 1.8V CMOS, 100K PD	Digital audio Output *Note: This signal is also used as BOOT_MODE3*

2.7.5 SPI Interface

The i.MX 93 or i.MX 91 SoC supports Low Power Serial Peripheral Interface (LPSPI) module which provides an efficient interface to a SPI bus, either as a master or slave. The i.MX 93 or i.MX 91 SoC's SPI4 supports SPI_A channels of the OSM.

For more details on SPI pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y15	SPI_A_CS0#	SPI4_SSO(GPIO_IO18)	GPIO_IO18/ R18	O, 1.8V CMOS	SPI4 Chip Select 0
U16	SPI_A_SCK	SPI4_SCK(GPIO_IO21)	GPIO_IO21/ T21	O, 1.8V CMOS/33E	SPI4 Clock
U15	SPI_A_SDI_(IO0)	SPI4_MISO(GPIO_IO 19)	GPIO_IO19/ R17	I, 1.8V CMOS	SPI4 Master IN Slave Out
V15	SPI_A_SDO_(IO1)	SPI4_MOSI(GPIO_IO 20)	GPIO_IO20/ T20	O, 1.8V CMOS	SPI4 Master Out Slave In

Note: SPI4 is shared between Wi-Fi/BT module to support IEEE802.15.4 and OSM. If Wi-Fi/BT is required, SPI is not supported at the OSM. If SPI is required at the OSM, Wi-Fi/BT module will be made DNP in the OSM.

2.7.6 Data UART

The i.MX 93 or i.MX 91 OSM supports four UART channels where one is optional. The i.MX 93 or i.MX 91 SoC's UART1, UART2, UART5 are connected to the LGA whereas UART8 is by default connected to Bluetooth module and optionally connected to the LGA. UART5 and UART2 can be used for any data communication. UART1 of the SoC is connected to LGA and used as Debug UART.

For more details on UART pinouts, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
A14	UART_A_RX	UART5_RXD	GPIO_IO01/J20	I, 1.8V CMOS	UART5 Receiver.
B13	UART_A_TX	UART5_TXD	GPIO_IO00/J21	O, 1.8V CMOS	UART5 Transmitter.
C13	UART_A_RTS	UART5_RTS	GPIO_IO03/K21	O, 1.8V CMOS	"Request to Send" handshake signal for UART5
C14	UART_A_CTS	UART5_CTS	GPIO_IO02/K20	I, 1.8V CMOS	"Clear to Send" handshake signal for UART5
D14	UART_B_RX	UART8_RXD	GPIO_IO13/N21	I, 1.8V CMOS	NC.

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Optional. By default, connected to BT
D13	UART_B_TX	UART8_TXD	GPIO_IO12/N20	O, 1.8V CMOS	NC. Note: Optional. By default, connected to BT
D16	UART_B_CTS	UART8_CTS	GPIO_IO14/P20	I, 1.8V CMOS	"Clear to Send" handshake signal for UART8
D15	UART_B_RTS	UART8_RTS	GPIO_IO15/P21	O, 1.8V CMOS	"Request to Send" handshake signal for UART8
A22	UART_C_RX	UART2_RXD	UART2_RXD/F20	I, 1.8V CMOS	UART2 Receiver.
B23	UART_C_TX	UART2_TXD(BOOT_MODE1)	UART2_TXD/F21	O, 1.8V CMOS, 4.7K PU	UART2 Transmitter. *Note: Signal is also used as BOOT_MODE1*
D22	UART_CON_RX	UART1_RXD	UART1_RXD/E20	I, 1.8V CMOS	Debug UART Receiver. *Note: Also connected to on-Module programming header.*
D23	UART_CON_TX	UART1_TXD(BOOT_MODE0)	UART1_TXD/E21	O, 1.8V CMOS, 4.7K PU	Debug UART Transmitter. *Note:Also connected to on-Module programming header.*

2.7.7 CAN Interface

The Flexible Controller Area Network (FlexCAN) module is a communication controller implementing the CAN protocol according ISO 11898-1:2015 standard and CAN 2.0 B protocol specifications. The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol, and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads. The i.MX 93 or i.MX 91 SoC Supports two CAN interface and are connected to OSM LGA.

For more details of CAN pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AC17	CAN_A_TX	CAN1_TX(PDM_CLK)	PDM_CLK/G17	O, 1.8V CMOS	CAN 1 Transmitter.
AB17	CAN_A_RX	CAN1_RX(PDM_BIT0)	PDM_BIT_STREAM0/J17	I, 1.8V CMOS	CAN 1 Receiver.

AC19	CAN_B_TX	CAN2_TX(GPIO_IO25)	GPIO_IO25/V21	O, 1.8V CMOS	CAN 2 Transmitter.
AB19	CAN_B_RX	CAN2_RX(GPIO_IO27)	GPIO_IO27/W21	I, 1.8V CMOS	CAN 2 Receiver.

2.7.8 JTAG Interface (Optional)

The i.MX 93 or i.MX 91 OSM supports JTAG interface for SoC debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG).

For more details on JTAG pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
N17	JTAG_TCK(SWCLK)	GPIO3_IO30(JTAG_TCK)	DAP_TCLK_SWCLK/Y1	O CMOS ,1V8	JTAG test Clock. By default, 10K PD is mounted to read board configuration.
N19	JTAG_TMS(SWDIO)	GPIO3_IO29(JTAG_TMS)	DAP_TMS_SWDIO/W2	I CMOS ,1V8	JTAG test mode select. By default, 10K PD is mounted to read board configuration.
P17	JTAG_TDI	GPIO3_IO28(JTAG_TDI)	DAP_TDI/W1	I CMOS ,1V8	JTAG test data input. By default, 10K PU is mounted to read board configuration.
R17	JTAG_TDO(SWO)	GPIO3_IO31(JTAG_TDO)	DAP_TDO_TRACESWO/Y2	O CMOS ,1V8	JTAG test data output. By default, 10K PD is mounted to read board configuration.
R19	JTAG_NTRST	JTAG_NTRST	POR_B/A16	I CMOS ,1V8	Test Reset, Active Low

2.7.9 I2C Interface

The i.MX 93 or i.MX 91 OSM supports two I2C interface on OSM LGA. i.MX 93 or i.MX 91 SoC's I2C7 & I2C3 interfaces are connected to OSM LGA for I2C whereas the SoC's I2C2 is connected to On-SOM PMIC.

For more details of I2C pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AA15	I2C_A_SCL	I2C7_SCL(GPIO_IO07)	GPIO_IO07/ L21	O, 1.8V CMOS 4.7K PU	I2C7 Clock.
AA16	I2C_A_SDA	I2C7_SDA(GPIO_IO06)	GPIO_IO06/ L20	IO, 1.8V CMOS 4.7K PU	I2C7 Data.
AA20	I2C_B_SCL	I2C3_SCL(GPIO_IO29)	GPIO_IO29/ Y21	O, 1.8V CMOS	I2C3 Clock.

				4.7K PU	
AA21	I2C_B_SDA	I2C3_SDA(GPIO_IO28)	GPIO_IO28/ W20	IO, 1.8V CMOS 4.7K PU	I2C3 Data.

2.7.10 MIPI CSI Interface (Not available in i.MX 91)

The i.MX 93 OSM supports one 2-lane MIPI CSI-2 camera input complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2. It supports up to 2 Rx data lanes (plus 1 Rx clock lane) and 80 Mbps -1.5 Gbps per lane data rate in high-speed operation. It also supports 10 Mbps data rate in low power operation.

For more details of MIPI CSI pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
C1	CSI_DATA0_N	MIPI_CSI1_D0_N	MIPI_CSI1_D0_N /A11	I, MIPI	MIPI CSI differential data lane 0 negative.
B1	CSI_DATA0_P	MIPI_CSI1_D0_P	MIPI_CSI1_D0_P /B11	I, MIPI	MIPI CSI differential data lane 0 positive.
A2	CSI_DATA1_N	MIPI_CSI1_D1_N	MIPI_CSI1_D1_N /A10	I, MIPI	MIPI CSI differential data lane 1 negative.
A3	CSI_DATA1_P	MIPI_CSI1_D1_P	MIPI_CSI1_D1_P /B10	I, MIPI	MIPI CSI differential data lane 1 positive.
B3	CSI_CLOCK_N	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N /D10	I, MIPI	MIPI CSI differential Clock negative.
B4	CSI_CLOCK_P	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P /E10	I, MIPI	MIPI CSI differential Clock positive.
C3	I2C_CAM_SDA / CSI_TX_N	I2C7_SDA(GPIO_IO06)	GPIO_IO06/ L20	O, 1.8V CMOS 4.7K PU	MIPI CSI I2C Data.
C4	I2C_CAM_SCL / CSI_TX_P	I2C7_SCL(GPIO_IO07)	GPIO_IO07/ L21	IO, 1.8V CMOS 4.7K PU	MIPI CSI I2C Clock.

2.7.11 LVDS interface (Not available in i.MX 91)

The i.MX 93 SoC has LVDS Display Bridge which provides connectivity to relevant devices-Displays with LVDS receivers, arranging the data as required by the external display receiver and by LVDS display standards.

For more details of LVDS pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AP18	LVDS_A_LANE0_P	LVDS0_D0_P	LVDS_D0_P	O, LVDS	LVDS differential data lane 0 positive

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AP17	LVDS_A_LANE0_N	LVDS0_D0_N	LVDS_D0_N	O, LVDS	LVDS differential data Lane 0 negative
AR16	LVDS_A_LANE1_P	LVDS0_D1_P	LVDS_D1_P	O, LVDS	LVDS differential data lane 1 positive
AR15	LVDS_A_LANE1_N	LVDS0_D1_N	LVDS_D1_N	O, LVDS	LVDS differential data lane 1 negative
AP15	LVDS_A_LANE2_P	LVDS0_D2_P	LVDS_D2_P	O, LVDS	LVDS differential data lane 2 positive
AP14	LVDS_A_LANE2_N	LVDS0_D2_N	LVDS_D2_N	O, LVDS	LVDS differential data lane 2 negative
AP12	LVDS_A_LANE3_P	LVDS0_D3_P	LVDS_D3_P	O, LVDS	LVDS differential data lane 3 positive
AP11	LVDS_A_LANE3_N	LVDS0_D3_N	LVDS_D3_N	O, LVDS	LVDS differential data lane 3 negative
AN13	LVDS_A_CLK_P	LVDS0_CLK_P	LVDS_CLK_P	O, LVDS	LVDS differential Clock positive
AN12	LVDS_A_CLK_N	LVDS0_CLK_N	LVDS_CLK_N	O, LVDS	LVDS differential Clock negative
AM11	LVDS_I2C_CLK	I2C3_SCL(GPIO_IO29)	GPIO_IO29/ Y21	O,OD CMOS,1.8V	I2C CLK for Display and Touch
AM12	LVDS_I2C_DAT	I2C3_SDA(GPIO_IO28)	GPIO_IO28/ W20	IO,OD CMOS,1.8V	I2C DATA for Display and Touch
AN22	LVDS_BL_PWM	TPM4(GPIO_IO05)	GPIO_IO05/L18	O, 1.8V CMOS	LCD Back Light Brightness control PWM
AN23	LVDS_BL_EN	LVDS_BL_EN(IO_07)	-	O, 1.8V CMOS	LCD Backlight Enable

2.7.12 MIPI DSI interface (Not available in i.MX 91)

The i.MX 93 OSM supports one 4-lane MIPI DSI display with data supplied by the LCDIF Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2. It is capable of resolutions achievable with a 200 MHz pixel clock and active pixel rate of 140 Mpixel/s with 24-bit RGB. Support 80 Mbps—1.5 Gbps data rate per lane in high-speed operation.

For more details of MIPI DSI pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
AB11	DSI_DATA0_N	MIPI_DSI1_D0_N	MIPI_DSI1_D0_N/A6	O, MIPI	DSI differential output
AB10	DSI_DATA0_P	MIPI_DSI1_D0_P	MIPI_DSI1_D0_P/B6	O, MIPI	DSI differential output
AC9	DSI_DATA1_N	MIPI_DSI1_D1_N	MIPI_DSI1_D1_N/A7	O, MIPI	DSI differential output
AC8	DSI_DATA1_P	MIPI_DSI1_D1_P	MIPI_DSI1_D1_P/B7	O, MIPI	DSI differential output
AC6	DSI_DATA2_N	MIPI_DSI1_D2_N	MIPI_DSI1_D2_N/A8	O, MIPI	DSI differential output
AC5	DSI_DATA2_P	MIPI_DSI1_D2_P	MIPI_DSI1_D2_P/B8	O, MIPI	DSI differential output
AB5	DSI_DATA3_N	MIPI_DSI1_D3_N	MIPI_DSI1_D3_N/A9	O, MIPI	DSI differential output
AB4	DSI_DATA3_P	MIPI_DSI1_D3_P	MIPI_DSI1_D3_P/B9	O, MIPI	DSI differential output
AB8	DSI_CLOCK_N	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N/D6	O, MIPI	DSI differential output
AB7	DSI_CLOCK_P	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P/E6	O, MIPI	DSI differential output

2.7.13 SD Interface

The i.MX 93 or i.MX 91 OSM supports 4bit SD interface over OSM LGA which can be used to connect SD card as Mass storage or boot device. uSDHC2 controller of the i.MX 93 SoC is used to support OSM SD interface. It supports 4-bit transfer mode for SD 3.0. The I/O voltage level of uSDHC2 lines can be set to 1.8V or 3.3V based on PMIC configuration through SoC signal SD2_VSELECT. If SD2_VSELECT is set to low, then 3.3V IO level is selected for uSDHC2 lines. If SD2_VSELECT is set to high, then 1.8V IO level is selected for uSDHC2 lines. For more details on SD pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
F21	SDIO_A_CLK	SD2_CLK	SD2_CLK/AA19	O, 1.8/3.3V, 33E	SD Clock
E20	SDIO_A_CMD	SD2_CMD	SD2_CMD/Y19	IO, 1.8/3.3V CMOS	SD command

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
G20	SDIO_A_D0	SD2_DATA0	SD2_DATA0/Y18	IO, 1.8/3.3V CMOS	SD data 0
G21	SDIO_A_D1	SD2_DATA1	SD2_DATA1/AA18	IO, 1.8/3.3V CMOS	SD data 1
H20	SDIO_A_D2	SD2_DATA2	SD2_DATA2/Y20	IO, 1.8/3.3V CMOS	SD data 2
H21	SDIO_A_D3	SD2_DATA3	SD2_DATA3/AA20	IO, 1.8/3.3V CMOS	SD data 3
J21	SDIO_A_CD#	SD2_CD_B	SD2_CD_B/Y17	I, 1.8V/3.3V CMOS 10K PU	SD Card Detect
D21	SDIO_A_PWR_EN	GPIO3_IO7(SD2_RESET_B)	SD2_RESET_B/AA17	O, 3.3V CMOS	SD Power enable

2.7.14 OSM GPIOs

The i.MX 93 or i.MX 91 OSM supports GPIOs on OSM LGA in i.MX 93 OSM Development platform's default configuration. Most of the SoC Pins which are connected to OSM LGA can be configured as GPIO with interrupt capable (if not used as other interface). The SoC's GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

For more details on GPIO Interface pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
D17	GPIO_A_0	OSM_GPIO_A0(GPIO1_IO01_I3C1_SDA)	I2C1_SDA/C21	IO, 1.8V CMOS	OSM General Purpose Input/output A0.
E17	GPIO_A_1	OSM_GPIO_A1(SPI3_MISO_GPIO_IO09)	GPIO_IO09/ M21	IO, 1.8V CMOS	OSM General Purpose Input/output A1.
F17	GPIO_A_2	OSM_GPIO_A2(SPI3_MOSI_GPIO_IO10)	GPIO_IO10/ N17	IO, 1.8V CMOS	OSM General Purpose Input/output A2.
G17	GPIO_A_3	OSM_GPIO_A3(SPI3_SS0_GPIO_IO08)	GPIO_IO08/M20	IO, 1.8V CMOS	OSM General Purpose Input/output A3.
H17	GPIO_A_4	OSM_GPIO_A4(SPI3_SCLK_GPIO_IO11)	GPIO_IO11/N18	IO, 1.8V CMOS	OSM General Purpose Input/output A4.
J17	GPIO_A_5	OSM_GPIO_A5(GPIO1_IO00_I3C1_SCL)	I2C1_SCL/ C20	IO, 1.8V CMOS	OSM General Purpose Input/output A5.
K17	GPIO_A_6 / SPI_A_CS1#	OSM_GPIO_A6(IO_5)	-	IO, 1.8V CMOS	OSM General Purpose Input/output A6.
L17	GPIO_A_7 / SPI_B_CS1#	OSM_GPIO_A7(GPIO4_IO29_CCM_CLKO4	CCM_CLKO4/V4	IO, 1.8V CMOS	OSM General Purpose Input/output A7.

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
		)			*Optionally connected to BT module*
D19	GPIO_B_0	OSM_GPIO_B07(GPIO3_IO28_CCM_CLKO3)	CCM_CLKO3/ U4	IO, 1.8V CMOS	OSM General Purpose Input/output B0. *Optionally connected to BT module*
E19	GPIO_B_1	OSM_GPIO_B1(GPIO_IO16)	GPIO_IO16/R21	IO, 1.8V CMOS	OSM General Purpose Input/output B1.
F19	GPIO_B_2	OSM_GPIO_B2(GPIO_IO17)	GPIO_IO17/R20	IO, 1.8V CMOS	OSM General Purpose Input/output B2.
J19	GPIO_B_5	OSM_GPIO_B5(GPIO_IO26)	GPIO_IO26/V20	IO, 1.8V CMOS	OSM General Purpose Input/output B5.
F3	GPIO_C_4 / DISP_VDD_EN	OSM_GPIO_C4(GPIO_IO22)	GPIO_IO22/U18	IO, 1.8V CMOS	OSM General Purpose Input/output C4.
F4	GPIO_C_5 / DISP_BL_EN	OSM_GPIO_C5(GPIO1_IO10_PDM_B1)	PDM_BIT_STREAM1/G18	IO, 1.8V CMOS	OSM General Purpose Input/output C5.
G3	CAM_PWR / GPIO_C_6	CAM_PWR_EN(GPIO_IO24)	GPIO_IO24/U21	O, 1.8V CMOS	Camera Power Enable, active high output *Optionally connected to BT WAKE_IN*
G4	CAM_RST# / GPIO_C_7	CAM_RST(GPIO_IO23)	GPIO_IO23/U20	O, 1.8V CMOS	Camera reset, active low output

2.7.15 Miscellaneous Pins

For more details of miscellaneous pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
M18	ADC_0	ADC_IN0	ADC_IN0/B19	Analog, 0V -1.8V	Analog Digital Converter 0
N18	ADC_1	ADC_IN1	ADC_IN1/A20	Analog, 0V -1.8V	Analog Digital Converter 1
B22	VENDOR DEFINED1	PMIC_ON_REQ	PMIC_ON_REQ/A17	O, 1.8V CMOS 100K PD	PMIC on request signal
C16	VENDOR DEFINED2	ADC_IN2	ADC_IN2/B20	Analog, 0V -1.8V	Analog Digital Converter 2
P16	VENDOR DEFINED3	ADC_IN3	ADC_IN3/B21	Analog, 0V -1.8V	Analog Digital Converter 3
D7	VENDOR DEFINED7	TAMPER1	TAMPER1/F14	-	Tamper Pin 1
D6	VENDOR DEFINED6	TAMPER0	TAMPER0/B16	-	Tamper Pin 0
A16	COM_AREA_02	OSM_ANT0	-	-	Main Antenna *Optional. By default, connected to Wi-Fi*

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
					Bluetooth antenna.

2.7.16 Control Signals

OSM V1.1 specification supports control Signals, for more details on OSM Control Signals pinouts on OSM LGA, refer below table:

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
U19	BOOT_SEL0#	BOOT_SEL0#	UART1_TXD/E21	I OD CMOS ,1.8V	**BOOT_MODE (3:0)** **0001**-USB Serial Download **0010**-eMMC boot **0011**-SD boot
R18	BOOT_SEL1#	UART2_TXD(BOOT_MODE1)	UART2_TXD/AR25	I OD CMOS ,1.8V, 4.7K PU	
U17	SYS_RST#	PMIC_RST_B	NA	I, 1.8V CMOS 10K PU	Hard RESET Input to SOM.
AA9	PWR_BTN#	CPU_ON_OFF	ON_OFF_BUTTON/ AR21	I, 1.8V CMOS 10K PU	Power ON /OFF Input to SOM.
V17	CARRIER_PWR_EN	CARRIER_PWR_ON	NA	O, 1.8V CMOS	Carrier Board power should be enabled only after CARRIER_PWR_ON goes High.
T17	FORCE_RECOV#	FORCE_RECOV#	NA	I OD CMOS ,1.8V	If low on carrier board module enters recovery mode.

2.7.17 Power and GND

The i.MX 93 or i.MX 91 OSM LGA Module works with 5V power input (VCC) from OSM LGA and generates all other required powers internally On-SOM itself. i.MX 93 or i.MX 91 OSM LGA Module also supports coin cell power input (VDD_RTC) from OSM LGA to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on OSM LGA, refer the below table.

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y17, Y8, Y9, Y10, Y11, Y25, Y26, Y27, Y28, AE4, AF4, AG4, AH3, AH4, AJ3, AJ4, AK4	VCC_IN_5V	VCC_IN_5V	NA	I, 5V Power	Supply Voltage.
M19	VCC_2_TEST	VDD_3V3	NA	I, 1.1V POWER	Module power voltage test point

Pin No.	OSM Pin Name	OSM Ball Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
Y16	VCC_3_TEST	NVCC_SD2	NA	I, 3.3V/1.8V POWER	Module power voltage test point
Y20	VCC_4_TEST	VDD_SOC_0V8	NA	I, 0.8V POWER	Module power voltage test point
D18, E15, E21, F16, F20, J16, J20, L18, M16, M20, P18, R16, R20, V16, V20, Y18, AA14, AA17, AA19, AA22, AB15, AB21,A4, A7, A10, B2, B5, B8, B9, C11, D1, D5, D8, E2, H2, H4, L2, L4, P2, P4, R1, U2, U4, V1, W3, Y2, AA1, AA4, AA7, AA8, AA10, AA11, AB3, AB6, AB9, AC4, AC7, AC10,A26, A29, A32, B27, B28, B30, B33, C25, C32, C35, D28, D34, F33, F35, G34, H32, J33, J35, K34, M35, N34, T34, W34, AA25, AA26, AA27, AA28, AA32, AB28, AB31, AB34, AC27, AC30, AC33,AE2, AE34, AF35, AG3, AH2, AH34, AJ35, AK3, AL2, AL34, AM13, AM16, AM19, AM22, AM35, AN3, AN6, AN9, AN11, AN15, AN18, AN21, AN33, AP2, AP5, AP8, AP13, AP16, AP19, AP22, AP25, AP28, AP31, AP34, AR14, AR17, AR20, AR26, AR29, AR32	GND	GND	NA	Power	Ground.
W17		VRTC_3V0	NA	I, 3V Power	3V coin cell input for RTC.

2.8 Other Features

2.8.1 Programming Header

The i.MX 93 or i.MX 91 OSM LGA Module supports 16 pin programming header for programming the board and testing the on-module features without soldering the module on the carrier board.

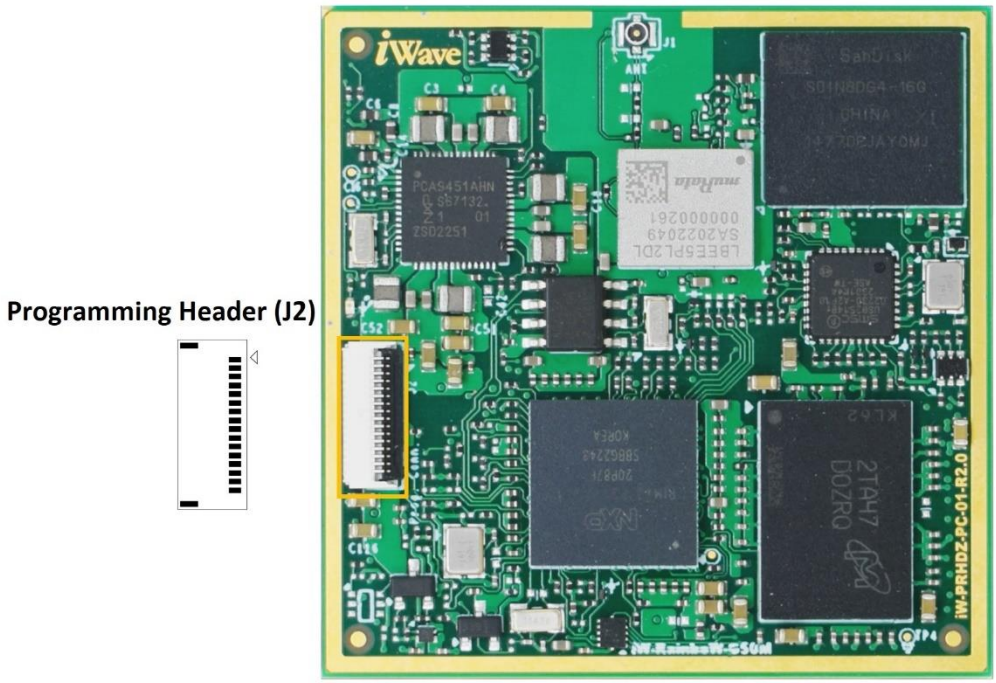

Figure 6: Programming Header

Number of Pins - 16

Connector Part - 503480-1600 from Molex

Table 4: Programming header Pin assignment

Pin No	Signal Name	SoC Ball Name/ Pin Number	Signal Type/ Termination	Description
1	VCC_IN_5V	NA	Power	Supply voltage
2	VCC_IN_5V	NA	Power	Supply voltage
3	VCC_IN_5V	NA	Power	Supply voltage
4	VCC_IN_5V	NA	Power	Supply voltage
5	VCC_IN_5V	NA	Power	Supply voltage
6	GND	NA	Power	Ground
7	USB1_DM	USB1_D_N/A14	IO, USB	USB2.0 Data Negative.
8	USB1_DP	USB1_D_P/B14	IO, USB	USB2.0 Data Positive.
9	GND	NA	Power	Ground
10	OTG1_VBUS	USB1_VBUS/F12	I, Power	USB VBUS power for detection.
11	GND	NA	Power	Ground
12	UART1_RXD	UART1_RXD/ E20	O, 1.8V CMOS	Debug UART Receiver.

13	UART1_TXD(BOOT_MODE0)	UART1_TXD/E21	4.7K PU, I, 1.8V CMOS	Debug UART Transmitter.
14	GND	NA	Power	Ground
15	GND	NA	Power	Ground
16	FORCE_RECOV#	-	I, OD 1.8V CMOS	If this signal is low, module enters recovery mode (Flash mode)

2.9 i.MX 93 or i.MX 91 Pin Multiplexing on OSM LGA

The i.MX 93 or i.MX 91 SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 93 or i.MX 91 SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 93 or i.MX 91 SoC pin connections to the OSM LGA and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 93 or i.MX 91 Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the OSM LGA for iWave's BSP reusability and to have compatible OSM modules in future for upgradability.

Table 5: i.MX 93 or i.MX 91 SoC IOMUX for OSM LGA interfaces

Interfaces	OSM Pin No.	SoC Pin No.	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
ENET1	J15	U10	enet_qos.RGMII_TXC	enet_qos.TX_ER			flexio2.FLEXIO[7]	gpio4.IO[7]		
	K16	Y8	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]		
	H15	W11	enet_qos.RGMII_TD0	uart3.TX			flexio2.FLEXIO[5]	gpio4.IO[5]		
	G15	T12	enet_qos.RGMII_TD1	uart3.RTS_B	i3c2.PUR	usb1.OTG_OC	flexio2.FLEXIO[4]	gpio4.IO[4]	i3c2.PUR_B	
	H16	U12	enet_qos.RGMII_TD2	INPUT=enet_qos.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_CLK_ROOT	can2.RX	usb2.OTG_OC	flexio2.FLEXIO[3]	gpio4.IO[3]		
	G16	V12	enet_qos.RGMII_TD3		can2.TX	usb2.OTG_ID	flexio2.FLEXIO[2]	gpio4.IO[2]		
	R15	AA7	enet_qos.RGMII_RXC	enet_qos.RX_ER			flexio2.FLEXIO[9]	gpio4.IO[9]		
	M15	Y8	enet_qos.RGMII_RX_CTL	uart3.DSR_B		usb2.OTG_PWR	flexio2.FLEXIO[8]	gpio4.IO[8]		
	K15	AA8	enet_qos.RGMII_RD0	uart3.RX			flexio2.FLEXIO[10]	gpio4.IO[10]		
	L15	Y9	enet_qos.RGMII_RD1	uart3.CTS_B		lptmr2.ALT1	flexio2.FLEXIO[11]	gpio4.IO[11]		
	N15	AA9	enet_qos.RGMII_RD2			lptmr2.ALT2	flexio2.FLEXIO[12]	gpio4.IO[12]		
	P15	Y10	enet_qos.RGMII_RD3			lptmr2.ALT3	flexio2.FLEXIO[13]	gpio4.IO[13]		
	T15	AA10	enet_qos.MDIO	uart3.RIN_B	i3c2.SDA	usb1.OTG_PWR	flexio2.FLEXIO[1]	gpio4.IO[1]		
	T16	AA11	enet_qos.MDC	uart3.DCB_B	i3c2.SCL	usb1.OTG_ID	flexio2.FLEXIO[0]	gpio4.IO[0]		
USDHC2	E20	Y19	usdhc2.CMD	enet2.1588_EVENT0_IN	i3c2.PUR	i3c2.PUR_B	flexio1.FLEXIO[2]	gpio3.IO[2]		
	F21	AA19	usdhc2.CLK	enet_qos.1588_EVENT0_OUT	i3c2.SDA		flexio1.FLEXIO[1]	gpio3.IO[1]		
	G20	Y18	usdhc2.DATA0	enet2.1588_EVENT0_OUT	can2.TX		flexio1.FLEXIO[3]	gpio3.IO[3]		
	G21	AA18	usdhc2.DATA1	enet2.1588_EVENT1_IN	can2.RX		flexio1.FLEXIO[4]	gpio3.IO[4]		

Interfaces	OSM Pin No.	SoC Pin No.	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
	H20	Y20	usdhc2.DATA2	enet2.1588_EVENT1_OUT	mqs2.RIGHT		flexio1.FLEXIO[5]	gpio3.IO[5]		
	H21	AA20	usdhc2.DATA3	lptmr2.ALT1	mqs2.LEFT		flexio1.FLEXIO[6]	gpio3.IO[6]		
	J21	Y17	usdhc2.CD_B	enet_qos.1588_EVENT0_IN	i3c2.SCL		flexio1.FLEXIO[0]	gpio3.IO[0]		
	D21	AA17	usdhc2.RESET_B	lptmr2.ALT2			flexio1.FLEXIO[7]	gpio3.IO[7]		
SPI4	F17	R17	gpio2.IO[19]	sai3.RX_SYNC	pdm.BIT_STREAM[3]	lcdif.D[15]	spi5.SIN	spi4.SIN	tpm5.CH2	flexio1.FLEXIO[18]
	G17	T20	gpio2.IO[20]	sai3.RX_DATA[0]	pdm.BIT_STREAM[0]	lcdif.D[16]	spi5.SOUT	spi4.SOUT	tpm6.CH2	sai3.TX_DATA[0]
	H17	T21	gpio2.IO[21]	sai3.TX_DATA[0]	pdm.CLK	lcdif.D[17]	spi5.SCK	spi4.SCK	tpm3.CH1	flexio1.FLEXIO[20]
	E17	R18	gpio2.IO[18]	sai3.RX_BCLK	isi.D[9]	lcdif.D[14]	spi5.PCS0	spi4.PCS0		
CAN1	AC17	G17	pdm.CLK	mqs1.LEFT			lptmr1.ALT1	gpio1.IO[8]	can1.TX	
	AB17	J17	pdm.BIT_STREAM[0]	mqs1.RIGHT	spi1.PCS1	tpm1.EXTCLK	lptmr1.ALT2	gpio1.IO[9]	can1.RX	
CAN2	AC19	V21	gpio2.IO[25]	usdhc3.DATA1	can2.TX	lcdif.D[21]	tpm4.CH3	dap.TCLK_SWCLK	spi7.PCS1	flexio1.FLEXIO[25]
	AB19	W21	gpio2.IO[27]	usdhc3.DATA3	can2.RX	lcdif.D[23]	tpm6.CH3	dap.TMS_SWDIO	spi5.PCS1	flexio1.FLEXIO[27]
USB OTG1	AB16	F12	USB1_VBUS							
	AB14	C11	USB1_ID							
	AC14	B14	USB1_D_P							
	AB13	A14	USB1_D_N							
UART5	B13	J21	gpio2.IO[0]	i2c3.SDA	isi.PCLK	lcdif.PCLK	spi6.PCS0	uart5.TX	i2c5.SDA	flexio1.FLEXIO[0]
	A14	J20	gpio2.IO[1]	i2c3.SCL	isi.D[0]	lcdif.DE	spi6.SIN	uart5.RX	i2c5.SCL	flexio1.FLEXIO[1]
	C13	K20	gpio2.IO[2]	i2c4.SDA	isi.FRAME_VALID	lcdif.VSYNC	spi6.SOUT	uart5.CTS_B	i2c6.SDA	flexio1.FLEXIO[2]
	C14	K21	gpio2.IO[3]	i2c4.SCL	isi.LINE_VALID	lcdif.HSYNC	spi6.SCK	uart5.RTS_B	i2c6.SCL	flexio1.FLEXIO[3]
LVDS PWM	AN22	L18	gpio2.IO[5]	tpm4.CH0	pdm.BIT_STREAM[0]	lcdif.D[1]	spi7.SIN	uart6.RX	i2c6.SCL	flexio1.FLEXIO[5]
i2C	AA16	L20	gpio2.IO[6]	tpm5.CH0	pdm.BIT_STREAM[1]	lcdif.D[2]	spi7.SOUT	uart6.CTS_B	i2c7.SDA	flexio1.FLEXIO[6]
	AA15	L21	gpio2.IO[7]	spi3.PCS1	isi.D[1]	lcdif.D[3]	spi7.SCK	uart6.RTS_B	i2c7.SCL	flexio1.FLEXIO[7]

Interfaces	OSM Pin No.	SoC Pin No.	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
	AA21	W20	gpio2.IO[28]	i2c3.SDA						flexio1.FLEXIO[28]
	AA20	Y21	gpio2.IO[29]	i2c3.SCL						flexio1.FLEXIO[29]
UART8	D14	N21	gpio2.IO[13]	tpm4.CH2	pdm.BIT_STREAM[3]	lcdif.D[9]	spi8.SIN	uart8.RX	i2c8.SCL	flexio1.FLEXIO[13]
	D13	N20	gpio2.IO[12]	tpm3.CH2	pdm.BIT_STREAM[2]	lcdif.D[8]	spi8.PCS0	uart8.TX	i2c8.SDA	sai3.RX_SYNC
	D15	P20	gpio2.IO[14]	uart3.TX	isi.D[6]	lcdif.D[10]	spi8.SOUT	uart8.CTS_B	uart4.TX	flexio1.FLEXIO[14]
	D16	P21	gpio2.IO[15]	uart3.RX	isi.D[7]	lcdif.D[11]	spi8.SCK	uart8.RTS_B	uart4.RX	flexio1.FLEXIO[15]
UART2	A22	F20	uart2.RX	uart1.CTS_B	spi2.SOUT	tpm1.CH2	sai1.MCLK	gpio1.IO[6]	uart2.RX	
	B23	F21	uart2.TX	uart1.RTS_B	spi2.SCK	tpm1.CH3		gpio1.IO[7]/ccmsrcgpcmix.BOOT_MODE[1]	uart2.TX	
UART1	D22	E20	uart1.RX	seco.RX	spi2.SIN	tpm1.CH0		gpio1.IO[4]		
	D23	E21	uart1.TX	seco.TX	spi2.PCS0	tpm1.CH1		gpio1.IO[5]/ccmsrcgpcmix.BOOT_MODE[0]		
Audio SAI	W20	G20	sai1.TX_BCLK	uart2.CTS_B	spi1.SIN	uart1.DSR_B	can1.RX	gpio1.IO[12]		
	W18	G21	sai1.TX_SYNC	sai1.TX_DATA[1]	spi1.PCS0	uart2.DTR_B	mqs1.LEFT	gpio1.IO[11]/ccmsrcgpcmix.BOOT_MODE[2]		
	V21	H20	sai1.RX_DATA[0]	sai1.MCLK	spi1.SOUT	uart2.DSR_B	mqs1.RIGHT	gpio1.IO[14]		
	W21	H21	sai1.TX_DATA[0]	uart2.RTS_B	spi1.SCK	uart1.DTR_B	can1.TX	gpio1.IO[13]/ccmsrcgpcmix.BOOT_MODE[3]		
JTAG	N19	W2	dap.TMS_SWDIO				flexio2.FLEXIO[31]	gpio3.IO[29]	uart5.RTS_B	
	N17	Y1	dap.TCLK_SWCLK				flexio1.FLEXIO[30]	gpio3.IO[30]	uart5.CTS_B	
	R17	Y2	dap.TDO_TRACESWO	mqs2.RIGHT		can2.RX	flexio1.FLEXIO[31]	gpio3.IO[31]	uart5.TX	
	P17	W1	dap.TDI	mqs2.LEFT		can2.TX	flexio2.FLEXIO[30]	gpio3.IO[28]	uart5.RX	
ENET2	H1	U6	enet2.RGMII_TXC	enet2.TX_ER	sai2.TX_BCLK		flexio2.FLEXIO[21]	gpio4.IO[21]		
	G2	V8	enet2.RGMII_TD2	INPUT=enet2.TX_CLK OUTPUT=ccmsrcgpcmix.ENET_REF_CLK_ROOT	sai2.RX_DATA[1]		flexio2.FLEXIO[17]	gpio4.IO[17]		
	J2	V6	enet2.RGMII_TX_CTL	uart4.DTR_B	sai2.TX_SYNC		flexio2.FLEXIO[20]	gpio4.IO[20]		

Interfaces	OSM Pin No.	SoC Pin No.	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
	F2	T10	enet2.RGMII_TD3		sai2.RX_DATA[0]		flexio2.FLEXIO[16]	gpio4.IO[16]		
	P1	AA3	enet2.RGMII_RXC	enet2.RX_ER	sai2.TX_DATA[1]		flexio2.FLEXIO[23]	gpio4.IO[23]		
	N1	Y6	enet2.RGMII_RD3	spdif1.OUT	spdif1.IN	mqs2.LEFT	flexio2.FLEXIO[27]	gpio4.IO[27]		
	M1	AA5	enet2.RGMII_RD2	uart4.CTS_B	sai2.MCLK	mqs2.RIGHT	flexio2.FLEXIO[26]	gpio4.IO[26]		
	K1	Y5	enet2.RGMII_RD1	spdif1.IN	sai2.TX_DATA[3]		flexio2.FLEXIO[25]	gpio4.IO[25]		
	G1	T8	enet2.RGMII_TD0	uart4.TX	sai2.RX_DATA[3]		flexio2.FLEXIO[19]	gpio4.IO[19]		
	F1	U8	enet2.RGMII_TD1	uart4.RTS_B	sai2.RX_DATA[2]		flexio2.FLEXIO[18]	gpio4.IO[18]		
	J1	AA4	enet2.RGMII_RD0	uart4.RX	sai2.TX_DATA[2]		flexio2.FLEXIO[24]	gpio4.IO[24]		
	L1	Y4	enet2.RGMII_RX_CTL	uart4.DSR_B	sai2.TX_DATA[0]		flexio2.FLEXIO[22]	gpio4.IO[22]		
	C6	AA6	enet2.MDIO	uart4.RIN_B	sai2.RX_BCLK		flexio2.FLEXIO[15]	gpio4.IO[15]		
	C7	Y7	enet2.MDC	uart4.DCB_B	sai2.RX_SYNC		flexio2.FLEXIO[14]	gpio4.IO[14]		
GPIO	D17	C21	i2c1.SDA	i3c1.SDA	uart1.RIN_B	tpm2.CH1		gpio1.IO[1]		
	E17	M21	gpio2.IO[9]	spi3.SIN	isi.D[3]	lcdif.D[5]	tpm3.EXTCLK	uart7.RX	i2c7.SCL	flexio1.FLEXIO[9]
	F17	N17	gpio2.IO[10]	spi3.SOUT	isi.D[4]	lcdif.D[6]	tpm4.EXTCLK	uart7.CTS_B	i2c8.SDA	flexio1.FLEXIO[10]
	G17	M20	gpio2.IO[8]	spi3.PCS0	isi.D[2]	lcdif.D[4]	tpm6.CH0	uart7.TX	i2c7.SDA	flexio1.FLEXIO[8]
	H17	N18	gpio2.IO[11]	spi3.SCK	isi.D[5]	lcdif.D[7]	tpm5.EXTCLK	uart7.RTS_B	i2c8.SCL	flexio1.FLEXIO[11]
	J17	C20	i2c1.SCL	i3c1.SCL	uart1.DCB_B	tpm2.CH0		gpio1.IO[0]		
	L17	V4	ccmsrcgpcmix.CLKO4				flexio2.FLEXIO[29]	gpio4.IO[29]		
	D19	U4	ccmsrcgpcmix.CLKO3				flexio2.FLEXIO[28]	gpio4.IO[28]		
	E19	R21	gpio2.IO[16]	sai3.TX_BCLK	pdm.BIT_STREAM[2]	lcdif.D[12]	uart3.CTS_B	spi4.PCS2	uart4.CTS_B	flexio1.FLEXIO[16]
	F19	R20	gpio2.IO[17]	sai3.MCLK	isi.D[8]	lcdif.D[13]	uart3.RTS_B	spi4.PCS1	uart4.RTS_B	flexio1.FLEXIO[17]
	J19	V20	gpio2.IO[26]	usdhc3.DATA2	pdm.BIT_STREAM[1]	lcdif.D[22]	tpm5.CH3	dap.TDI	spi8.PCS1	sai3.TX_SYNC
	F3	U18	gpio2.IO[22]	usdhc3.CLK	spdif1.IN	lcdif.D[18]	tpm5.CH1	tpm6.EXTCLK	tpm4.CH1	sai3.RX_BCLK
	F4	L17	gpio2.IO[4]	tpm3.CH0	pdm.CLK	lcdif.D[0]	spi7.PCS0	uart6.TX	i2c6.SDA	flexio1.FLEXIO[4]
	G3	U21	gpio2.IO[24]	usdhc3.DATA0		lcdif.D[20]	tpm3.CH3	dap.TDO_TRACESWO	spi6.PCS1	flexio1.FLEXIO[24]
	G4	U20	gpio2.IO[23]	usdhc3.CMD	spdif1.OUT	lcdif.D[19]	tpm6.CH1		i2c5.SCL	flexio1.FLEXIO[23]
ADC	M18	B19	anamix.adc_in0							
	N18	A20	anamix.adc_in1							

Interfaces	OSM Pin No.	SoC Pin No.	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7
Vendor defined	B22	A17	bbsmmix.PMIC_ON_REQ							
	C16	B20	anamix.adc_in2							
	P16	B21	anamix.adc_in3							
	D7	F14	bbsmmix.TAMPER1							
	D6	B16	bbsmmix.TAMPER0							

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 93or i.MX 91 OSM LGA Module technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the seventeen VCC_IN_5V in Size-L Module and returned through the numerous GND pins on the connector.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX 93 OSM LGA Module.

Table 6: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_IN_5V [1]	4.75	5V	5.25	-
2	VDD_RTC [2]	-	3V	-	-

[1] i.MX 93 or i.MX 91 OSM LGA Module is designed to work with VCC_IN_5V input power rail from OSM.
[2] i.MX 93 or i.MX 91 OSM LGA Module use this voltage as backup power source when VCC_IN_5V is OFF.

3.1.2 Power Input Sequencing

The i.MX 93 or i.MX 91 OSM LGA Module Power Input sequence requirement is explained below.

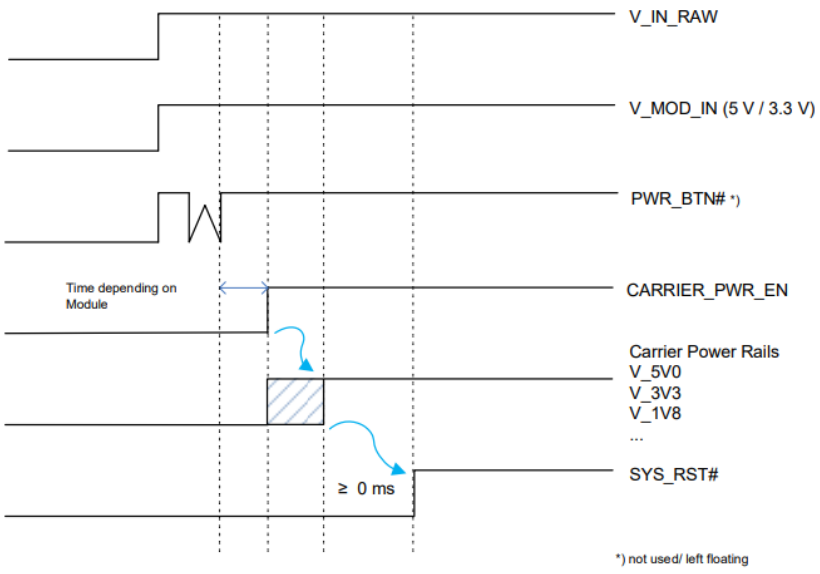

Figure 7: Power Input Sequencing

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. Also make sure that all Carrier board interface peripherals' power supply must be OFF if SOM is powered OFF, otherwise it can cause internal latch-up and malfunctions/bootup issues due to reverse current flows. NXP recommends customers to remove power (Voltage source) to all components on the board in the event of a processor reset.

3.1.3 Power Consumption

Table 7: i.MX 93 OSM Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Boot time Power consumption		
While booting	VCC_IN_5V	0.309A/1.545W
Run Mode Power Consumption		
Play Audio	VCC_IN_5V	0.171A/0.855W
Camera Streaming in MIPI	VCC_IN_5V	0.226A/1.13W
Camera Streaming in LVDS	VCC_IN_5V	0.197A/0.985W
Play Video run in LVDS(Gplay)	VCC_IN_5V	0.287A/1.435W
Play Video run in MIPI(Gplay)	VCC_IN_5V	0.32A/1.6W
Ping Bluetooth	VCC_IN_5V	0.165A/0.825W
Ping Wifi	VCC_IN_5V	0.21A/1.05W
Ping Ethernet (Eth0) at 1000Mbps	VCC_IN_5V	0.174A/0.87W
Ping Ethernet (Eth1) at 1000Mbps	VCC_IN_5V	0.173A/0.865W
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_IN_5V	0.177A/0.885W
eMMC to USB2.0 x 2 Host file transfer	VCC_IN_5V	0.307A/1.535W
eMMC to USB2.0 x1 OTG Host file transfer	VCC_IN_5V	0.225A/1.125W
eMMC to USB 2.0 x 1 Host (Type C) file transfer	VCC_IN_5V	0.367A/1.835W
eMMC to Micro SD file transfer	VCC_IN_5V	0.347A/1.735W
File Transfer - Transfer the 1MB files in storage devices	VCC_IN_5V	0.36A/1.8W
Dhrystone	VCC_IN_5V	0.219A/1.095W
Bluetooth file transfer	VCC_IN_5V	0.194A/0.97W
Wi-Fi file transfer	VCC_IN_5V	0.333A/1.665W
Ethernet Streaming (Video Play)	VCC_IN_5V	0.299A/1.495W
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1MB files in storage devices • Run the dry2 application on background • Ping Wifi • Camera Streaming • Play Video in LVDS	VCC_IN_5V	0.389A/1.954W
Low Power Mode Power Consumption		

Task/Status	Power Rail	Current Drawn/ Power Consumption
System Idle Mode	VCC_IN_5V	0.129A/0.645W
Deep Sleep Mode	VCC_IN_5V	0.035A/0.175W
RTC power when no VCC_IN_5V supply is provided	VRTC_3V0	0.04uA/0.12uW

Power consumption measurements have been done in iWave's i.MX 93 based Pico ITX SBC with iWave's iW-PRHDZ-SC-01-R2.0-REL0.1-Linux6.1.1 BSP.

Table 8: i.MX 91 OSM Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption		
Play Audio	VCC_IN_5V	TBD
Ping Bluetooth	VCC_IN_5V	TBD
Ping Wifi	VCC_IN_5V	TBD
Ping Ethernet (Eth0) at 1000Mbps	VCC_IN_5V	TBD
Ping Ethernet (Eth1) at 1000Mbps	VCC_IN_5V	TBD
Ping Ethernet (Eth0 & Eth1) at 1000Mbps	VCC_IN_5V	TBD
eMMC to USB2.0 file transfer	VCC_IN_5V	TBD
eMMC to USB2.0 OTG file transfer	VCC_IN_5V	TBD
eMMC to Micro SD file transfer	VCC_IN_5V	TBD
File Transfer - Transfer the 1GB files in storage devices	VCC_IN_5V	TBD
Dhrystone	VCC_IN_5V	TBD
Bluetooth file transfer	VCC_IN_5V	TBD
Maximum Power Test: Run the below during Maximum Power Test, • Ethernet (Eth0 & Eth1) - Run the ping (65500 packet size) test on background • File Transfer - Transfer the 1GB files in storage devices • Run the dry2 application on background • Ethernet Streaming (Video Play) • Ping Wifi • Ping Bluetooth	VCC_IN_5V	TBD
Low Power Mode Power Consumption		
System Idle Mode.	VCC_IN_5V	TBD
Deep Sleep Mode.	VCC_IN_5V	TBD
RTC power when no VCC_IN_5V supply is provided	VRTC_3V0	TBD

Power consumption measurements have been done in iWave's i.MX 91 based Pico ITX SBC with iWave's iW-PRHDZ-SC-01-R2.0-REL0.1-Linux6.1.1 BSP.

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX 93 or i.MX 91 OSM LGA Module.

Table 9: Environmental Specification

Parameters	Min	Max
Operating temperature range[1,2]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2]For more information on Thermal solution & Heat sink, refer the following section.

3.2.2 Heat Sink

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Note: iWave supports Heat Sink Solution for i.MX 93 or i.MX 91 OSM LGA Module. For more information on Heat Sink contact iWave support team. Do not Power ON the SOM without a proper thermal solution.

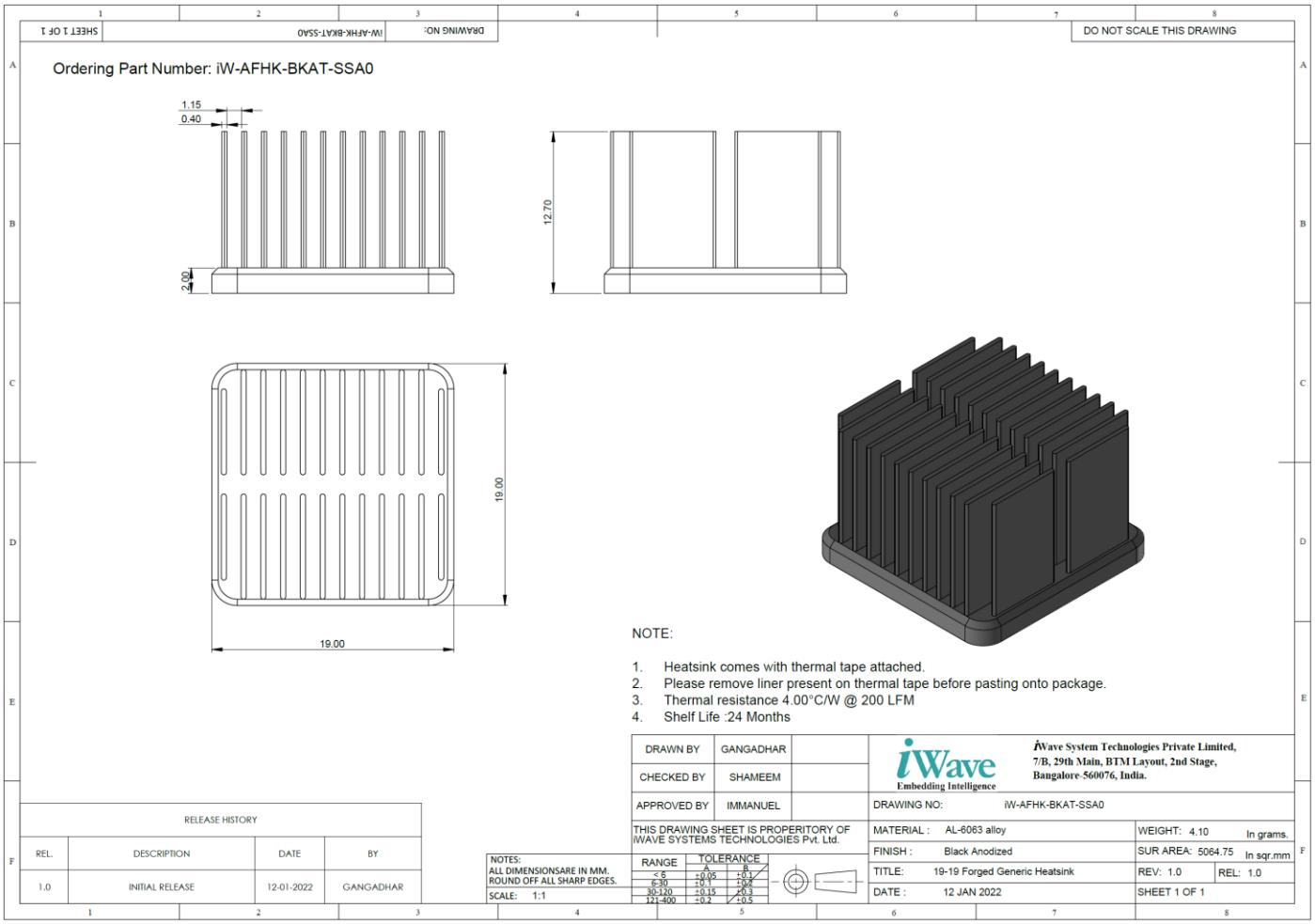

Figure 8: Mechanical dimension of Heat Sink

3.2.3 RoHS Compliance

iWave's i.MX 93 or i.MX 91 OSM LGA Module is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX 93 or i.MX 91 OSM LGA Module is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX 93 or i.MX 91 OSM LGA Module Mechanical Dimensions

i.MX 93 or i.MX 91 OSM LGA Module PCB size is 45 mm x 45 mm. Module mechanical dimensions are shown below. (All dimensions ae shown in mm).

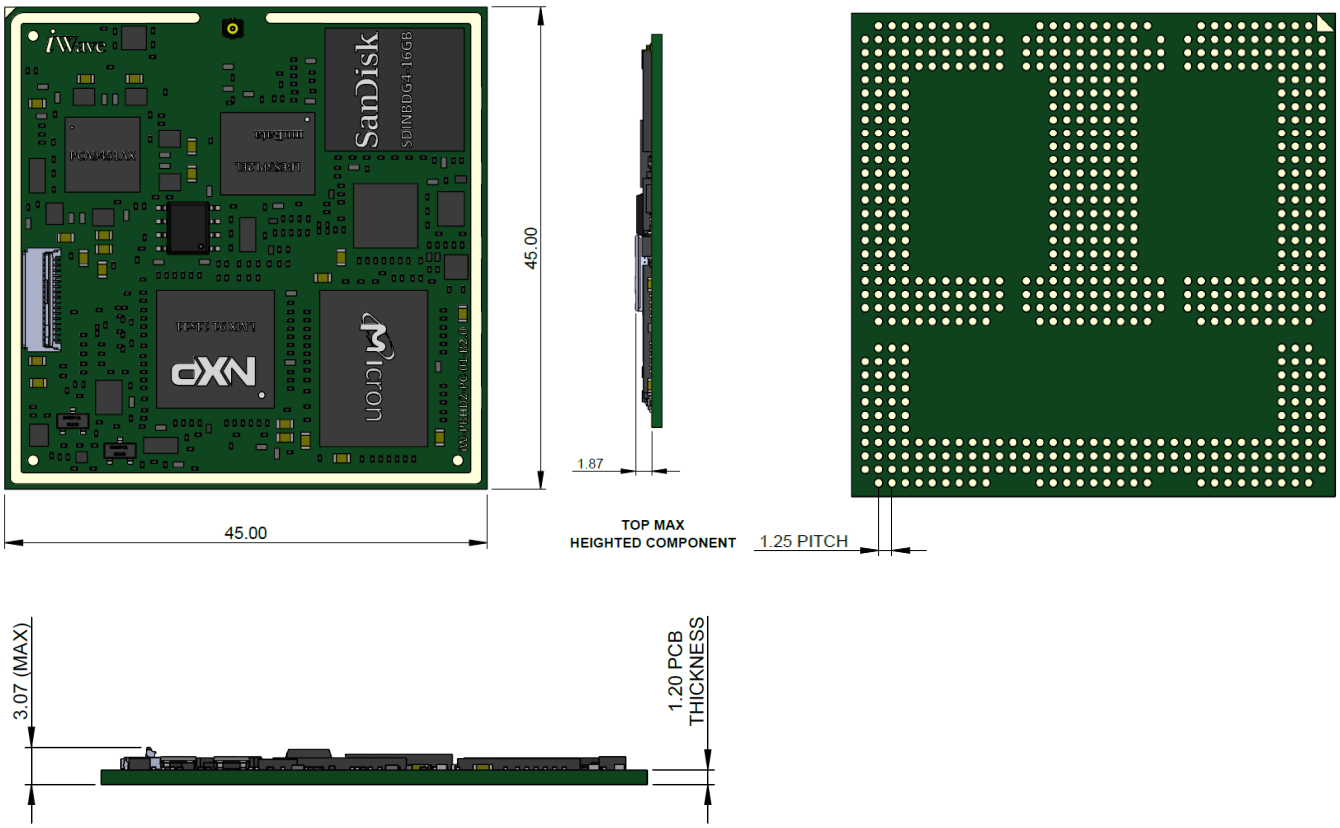

Figure 9: Mechanical dimension of i.MX 93 or i.MX 91 OSM LGA Module

The i.MX 93 or i.MX 91 OSM LGA Module PCB thickness is 1.2mm±0.1mm**,** top side maximum height component is 1.87mm (Programming Header) followed by RTC Controller (1.75mm). Please refer the above figure which gives height details of the Module.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 93 or i.MX 91 OSM LGA Module variants. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 10: Orderable Product Part Numbers

Product Part Number	Description	Temperature
Rainbow G50M - i.MX 9352 R2.0 OSM (Industrial grade)- With Wi-Fi, BT		
iW-G50M- OL93-4L002G-E016G-BIA	i.MX9352 Dual, 2GB LPDDR4X, 16GB eMMC-With Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 9352 R2.0 OSM (Industrial grade)- Without Wi-Fi, BT		
iW-G50M- OL93-4L002G-E016G-BIB	i.MX9352 Dual, 2GB LPDDR4X, 16GB eMMC-Without Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 91 R2.0 OSM (Industrial grade)- With Wi-Fi, BT		
iW-G50M- OL91-4L002G-E016G-BIA	i.MX 91, 2GB LPDDR4, 16GB eMMC-With Wi-Fi, BT	-40°C to 85°C
Rainbow G50M - i.MX 91 R2.0 OSM (Industrial grade)- Without Wi-Fi, BT		
iW-G50M- OL91-4L002G-E016G-BIB	i.MX 91, 2GB LPDDR4, 16GB eMMC-Without Wi-Fi, BT	-40°C to 85°C

Note:

- *Part Numbers mentioned in the above table are Pre-production silicon part numbers.*
- *Custom configuration Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.*
- *For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.*

5. APPENDIX-I

5.1 i.MX 93 or i.MX 91 SBC

iWave Systems supports iW-RainboW-G50S-i.MX 93 or i.MX 91 SBC which is targeted for quick validation of i.MX 93 or i.MX 91 SoC based OSM and its features. Being a Pico-ITX form factor with 100mm x 72mm size, the OSM Development Platform is highly packed with all necessary interfaces & on-board connectors to validate complete OSM supported features.

https://www.iwavesystems.com/product/i-mx-93-pico-itx-sbc/

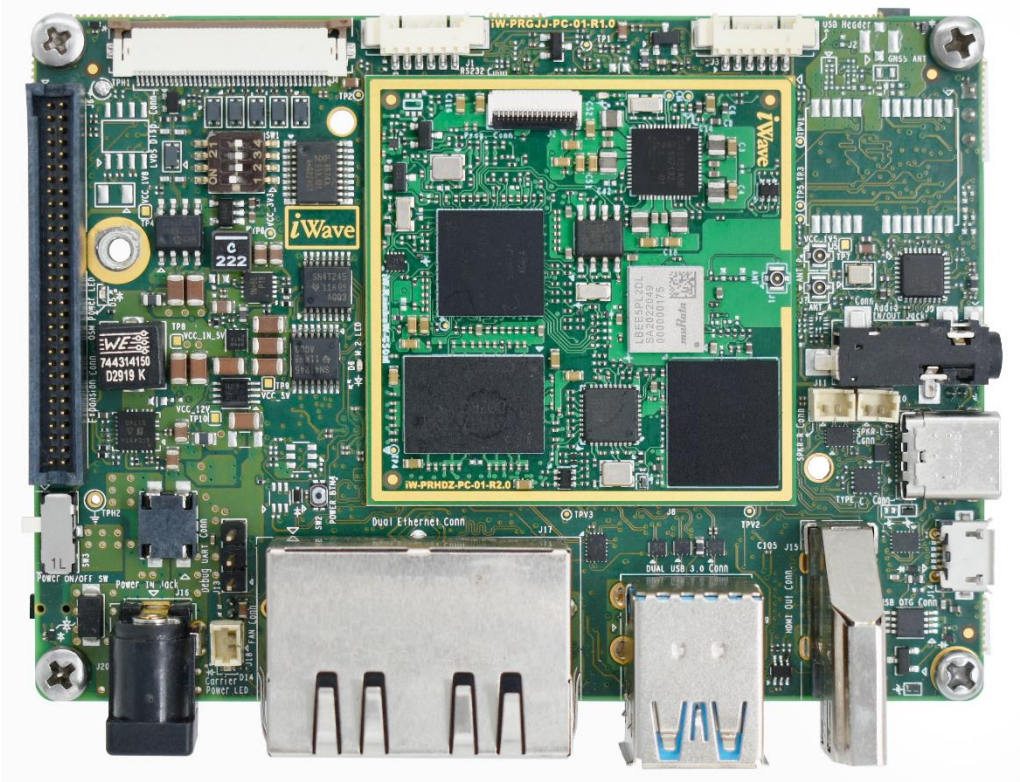

Figure 10: i.MX 93 or i.MX 91 SBC

6. APPENDIX-II

6.1 Design and Assembly recommendations

- It is recommended to give 50-100mils clearance in the Carrier Board from the OSM Module to other components and more than 200mils to connectors for easier assembly.
- For the vibration environment, it is better to use heat sink with mechanical fixing and it is recommended to have mounting holes in the carrier board.

  If iWave's thermal solution is planned to use, two Mounting holes are recommended in the Carrier Board. For the position and dimensions of the holes, please refer below drawing. (All the dimension are in mm).

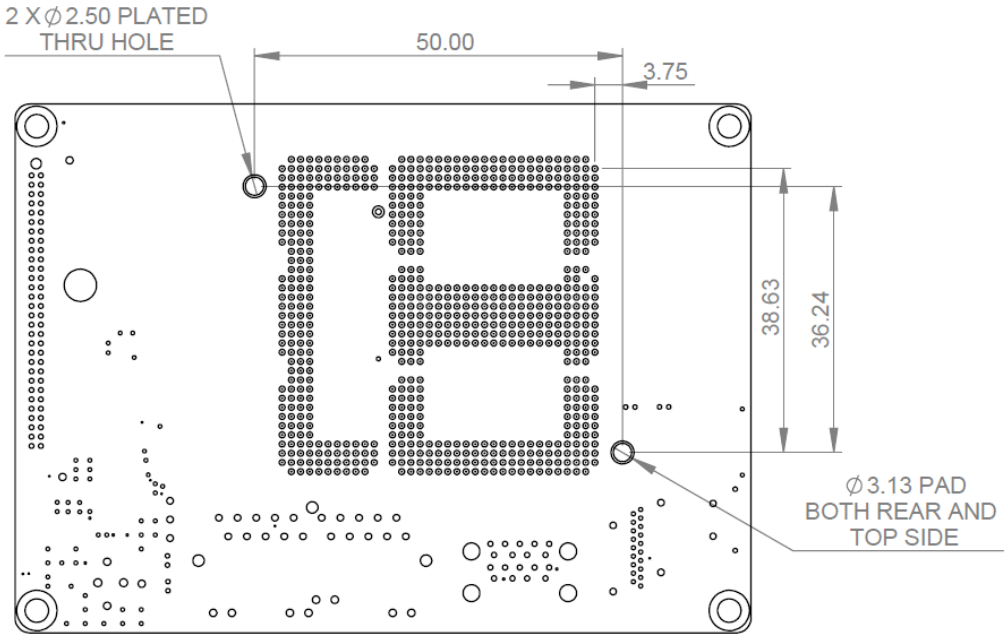

Figure 11: Dimensions of Mounting holes in the Carrier Board

- Contact iWave for more details regarding assembly of OSM on carrier board.


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