HI-84216

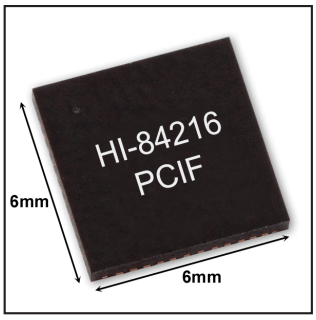
Programmable 16−Channel Low-Side Driver with SPI and Load Current Sensing

September, 2024

Overview

The HI-84216 is a smart 16-channel low-side driver designed for high reliability applications. The device uses a Serial Peripheral Interface (SPI) for intelligent switch control, monitoring and advanced diagnostics. It is capable of sinking 250mA per channel with up to 4A total sink current for parallel channel operation.

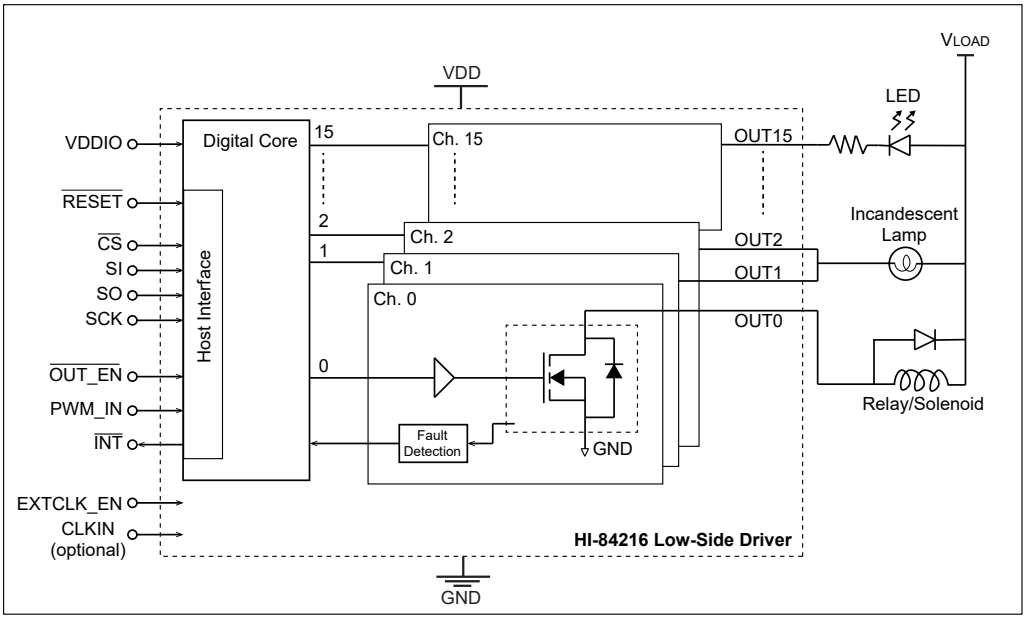
An 8-bit ADC provides accurate measurement of channel current and temperature while an internal PWM clock generator with 16-bit resolution provides application flexibility.



Features

- Compact 16 channel low-side driver (6mm x 6mm)
- 250mA sink current per channel
- Sink up to 4A when all channels used in parallel
- Accurate current/temperature measurement
- Access diagnostics and program via 10 MHz SPI
- 0.5 Ω On-Resistance per channel
- < 1µA leakage current with low quiescent power
- Digital I/O powered with 1.8V to 5.0V
- Continuous Online Built-in Self-Test
- Host-controlled output enable pin
- Operating Temperature:
  - -40°C to +85°C or -55°C to +125°C
- Over-current shutdown protection with programmable retries
- Thermal fail-safe
- Internal or external PWM option for soft-start or LED dimming
- Internal programmable PWM clock generator with 16-bit resolution on pulse width and period
- PWM configured on a per-channel basis over SPI
- PWM clock fault detection
- Optional programmable watchdog timer
- Programmable High/Low Current Thresholds
- Open/Short Load Detection
- Interrupt output pin set with enabled interrupts

Typical Applications



- Aerospace/Defense
- Avionics Discrete Output Signaling
- High Reliability
- LED Driver/Dimming
- Incandescent Lamp Control
- Relay and Solenoid
- Small DC Motor Control
- Valve/Actuator Control
- Automation
- General low-side-switch control

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Table of Contents

1. Block Diagram 7
2. Functional Description Summary 8
   2.1. Overview 8
   2.2. Fault Detection and Protection Features 8
      2.2.1. OverCurrent and Open Load Detection 8
      2.2.2. OverCurrent Shutdown with Retry Capability 8
      2.2.3. Thermal Fail-Safe Mechanism 8
   2.3. Internal PWM Clock Generator 8
   2.4. Watchdog Timer (WDT) 9
   2.5. Automated Built-In Self-Test 9
   2.6. Interrupts 9
3. Basic Set-Up and Configuration 10
   3.1. Additional Programmable Features 10
   3.2. Application Examples 11
      3.2.1. Generate a PWM waveform with duty cycle ratio 1:3000 and frequency 250 Hz. 11
      3.2.2. PWM Mode Output Driver 13
      3.2.3. Overcurrent Retry Operation for Incandescent Lamp Loads 14
4. Pin Diagram 15
5. Signal and Pin Descriptions 16
6. SPI Opcode and Register Summary 18
7. Registers 21
   7.1. Set-Up and Configuration Registers 21
      7.1.1. Configuration Register 0x00 21
      7.1.2. Channel Turn-On Register 0x01 23
      7.1.3. Individual Channel PWM Enable Register 0x02 23
      7.1.4. Channel PWM Source Enable Register 0x03 23
      7.1.5. Current Limit Threshold Register 0x05 24
      7.1.6. Channel Thermal Shutdown Disable Register 0x06 24
   7.2. Status Registers 25
      7.2.1. Built-In Self Test (BIST) Status Register 0x10 25

7.2.2. Die Temperature Status Register 0x11 25
7.2.3. Channel Average Current Status Register 0x12 26
7.2.4. Channel Recent Current Status Register 0x13 26
7.2.5. Channel High Current Status Register 0x14 26
7.2.6. Channel Low Current Status Register 0x15 27
7.2.7. Channel Over-temperature Status Register 0x16 27
7.3. Interrupt Registers 28
7.3.1. Interrupt Status Register 0x20 28
7.3.2. Channel Overcurrent Fault Pending Interrupt Register 0x21 30
7.3.3. Channel Current High Pending Interrupt Register 0x22 30
7.3.4. Channel Current Low Pending Interrupt Register 0x23 31
7.3.5. Channel Over-Temperature Shutdown Pending Interrupt Register 0x24 31
7.3.6. Global Interrupt Enable Register 0x25 32
7.3.7. Channel Overcurrent Fault Interrupt Enable Register 0x26 33
7.3.8. Channel Current High Interrupt Enable Register 0x27 33
7.3.9. Channel Current Low Interrupt Enable Register 0x28 33
7.3.10. Channel Overcurrent Fault Interrupt Output Enable Register 0x29 34
7.3.11. Channel Current High Interrupt Output Enable Register 0x2A 34
7.3.12. Channel Current Low Interrupt Output Enable Register 0x2B 35
7.4. PWM Registers 36
7.4.1. PWM Prescaler Register 0x30 36
7.4.2. PWM Period Register 0x31 36
7.4.3. PWM Pulsewidth Register 0x32 37
7.4.4. PWM Parallel Mask Register 0x33 37
7.4.5. PWM Parallel Prescaler Register 0x34 37
7.4.6. PWM Parallel Period Register 0x35 37
7.4.7. PWM Parallel Pulsewidth Register 0x36 38
7.5. Watchdog Timer Registers 39
7.5.1. Watchdog Timer Enable Register 0x40 39
7.5.2. Watchdog Timer Quiet Time Register 0x41 40
7.5.3. Watchdog Timer Active Time Register 0x42 40
7.5.4. Watchdog Timer Active Count Register 0x43 40
7.5.5. Watchdog Timer Quiet Count Register 0x44 41
7.5.6. Watchdog Timer Strobe Opcode 0xC5 41
7.6. OverCurrent Registers 42
7.6.1. Overcurrent Shutdown Delay Register 0x50 42

7.6.2. Overcurrent Retry Enable Register 0x51 42
7.6.3. Overcurrent Retry Attempts Register 0x52 43
7.6.4. Overcurrent Retry Delay Register 0x53 43

8. Reset and Initialization 44
8.1. Hardware Reset 44
8.2. Software Reset 44

9. Electrical Characteristics 45
9.1. Absolute Maximum Ratings 45
9.2. Recommended Operating Conditions 45
9.3. DC Electrical Characteristics 46
9.4. AC Electrical Characteristics 48

10. Package Dimensions 50

11. Ordering Information 51

12. Revision History 51

List of Figures

Figure 1. Block Diagram 7
Figure 2. PWM low duty cycle example flowchart 12
Figure 3. PWM output driver example 13
Figure 4. Overcurrent Retry example 14
Figure 5. OverCurrent Retry Operation 14
Figure 6. HI-84216PCxF QFN Package Pinout 15
Figure 7. SPI Register Access 18
Figure 8. SPI Read/Write Example 21
Figure 9. Watchdog Timer Process 39
Figure 10. Host Bus Interface Timing Diagram 49
Figure 11. Master Reset Timing Diagram 49

List of Tables

Table 1. SPI Opcodes and Register Functions 18

1. Block Diagram

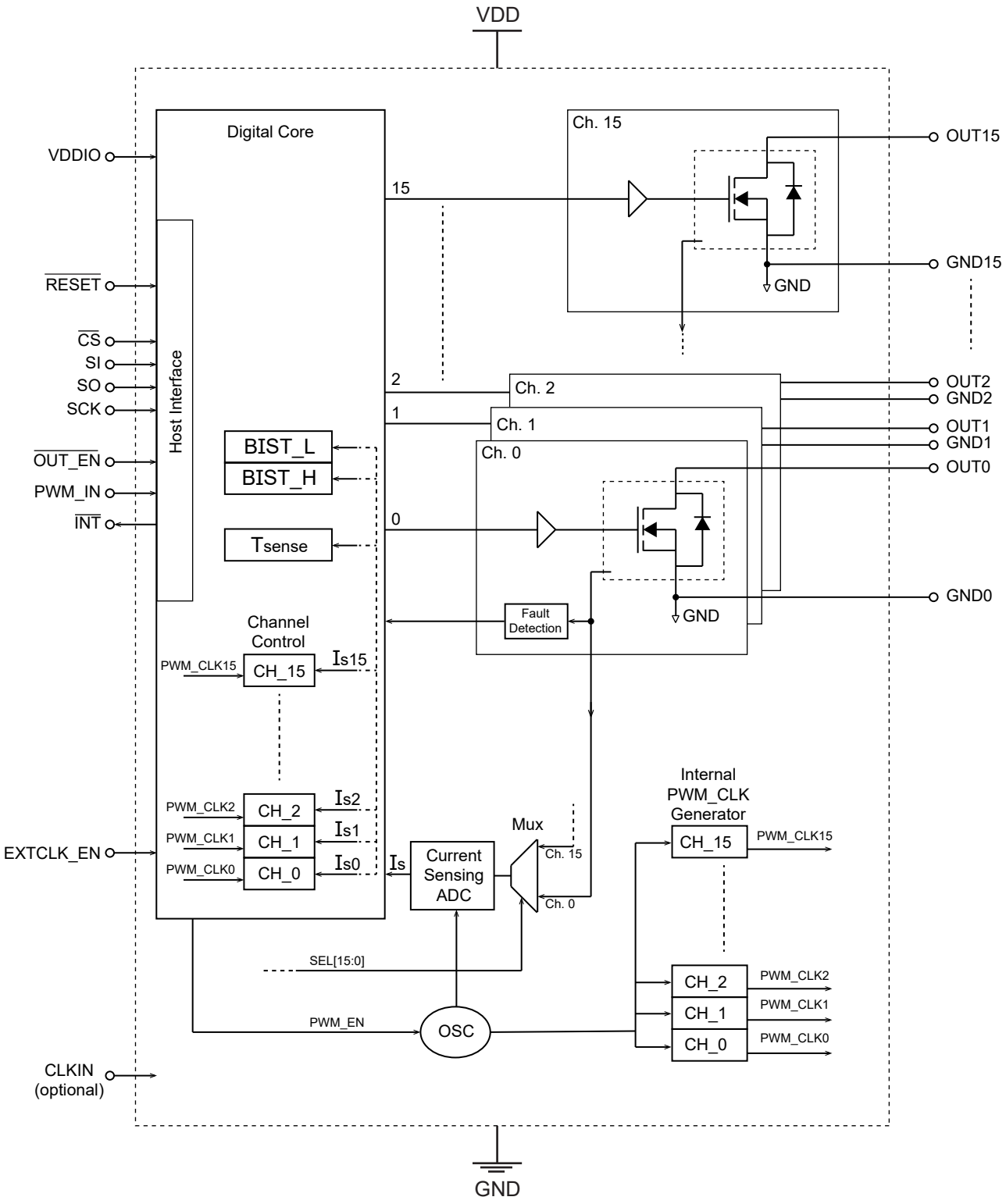


Figure 1. Block Diagram

2. Functional Description Summary

2.1. Overview

The HI-84216 is a 16−channel Low-Side output driver which interfaces to a host processor via a 10 MHz Serial Peripheral Interface (SPI). Each channel is configured to operate as OFF, ON, Internal PWM Drive, or External PWM Drive, with a capability to sink 250mA per channel. Channels may be connected in parallel to provide up to 4A sink current total. Internal analog circuitry is powered by a single 3.3V to 5.0V source (VDD).

2.2. Fault Detection and Protection Features

The device sequentially measures the global die temperature and output current of each turned-on channel using a single 8-bit A/D converter. The values are stored in registers as 8-bit binary words and may be read via host initiated SPI opcodes. The following subsections summarize the device protection features. In a fault condition, the host may also disable all outputs by setting the $\overline{\text{OUT\_EN}}$ pin.

2.2.1. OverCurrent and Open Load Detection

The user has the ability to program both high and low current threshold limits for overcurrent and open load detection respectively. Both hardware (via an $\overline{\text{INT}}$ pin) and software (via register) interrupts may be enabled on a per-channel basis to allow the user to monitor individual load current status.

2.2.2. OverCurrent Shutdown with Retry Capability

An overcurrent shutdown limit of 600 mA with a programmable shutdown delay protects the device against overcurrent faults or catastrophic inrush currents. The user may select retries on a per-channel basis, with a programmable retry delay and number of retries. This optional feature is useful for applications with large inrush currents that may trigger an overcurrent shutdown during start-up or turn on (e.g. incandescent bulbs).

2.2.3. Thermal Fail-Safe Mechanism

The device has a built-in thermal fail-safe mechanism which will automatically shut off any channel when its temperature exceeds the maximum fail-safe temperature (~215°C). The host may re-establish normal channel operation following a thermal shutdown by a single register write enable. All other programmed channel parameters such as PWM duty cycle and frequency will be retained.

2.3. Internal PWM Clock Generator

The device features an internal PWM clock generator which is fully programmable over the SPI bus on a per channel basis. A 5-bit clock period prescaler allows for extremely low duty cycles across a frequency range of 24 Hz to 48 kHz, with 16-bit resolution pulse width and period.

The user may also connect an external PWM clock, which will drive all turned-on channels with the same PWM waveform.

2.4. Watchdog Timer (WDT)

This optional feature is provided for applications that require the outputs to be disabled in a fail-safe event. Each channel has an individual WDT. If this feature is enabled, the host software must provide a periodic write strobe within the programmed timer interval to prevent an output driver from being disabled.

2.5. Automated Built-In Self-Test

A built-in self test, transparent to the user, runs continuously in the background. Two internal dummy loads (high and low) are periodically monitored and compared to check the integrity of internal signal paths. If a fault is indicated, an interrupt is generated and the result is stored in a status register.

2.6. Interrupts

Interrupts are provided for all fault protection events, such as thermal fail-safe, overcurrent shutdown, low current limit detection and WDT interval expiration. A pending interrupt register is provided with individual bits indicating all pending interrupts. This may be read at any time via SPI command. An interrupt output enable register enables individual interrupt signals to the $\overline{\text{INT}}$ output pin, ensuring the ability in hardware to flag when high priority interrupts have occurred.

3. Basic Set-Up and Configuration

The HI-84216 has many configurable features described in detail in the following sections, however it will operate from reset as a simple driver with built-in protection features requiring minimal configuration.

To utilize the part as a basic output driver, simply:

- Reset the HI-84216 by Hardware or Software
  - Issue SPI Opcode 0xE7, or Pulse $\overline{\text{RESET}}$ low for at least 200ns
- Turn on the channels required for use
  - Issue SPI Opcode 0x81 with values for the 16 outputs
  - For example, the sequence 0x81 0x00 0xFF 0xFF turns on all the drivers
  - The sequence 0x81 0x00 0x00 0x00 turns off all the drivers
  - **Notes:**
  - The turned-on channels will drive a load connected to the open-drain output (see “Typical Applications” on page 1) The recommended current limit for each channel is 250mA; if additional drive current is required, outputs should be connected in parallel to the load.
  - Turned-on channels are automatically protected by a thermal fail-safe and overcurrent shutdown protection. If either of these conditions occur, the channel will turn off and must be turned back on by the host by once again setting the corresponding bit in the “Channel Turn-On Register 0x01”.
  - **Turned-on channels will be driven continuously by default.** Internal or external PWM drive requires additional programming.

3.1. Additional Programmable Features

In addition to basic driver functionality with protections, many additional optional programmable features are available. These features all have default values following reset which do not need to be programmed for basic operation:

- Real-time accurate measurement of die temperature and individual channel current using an internal 8-bit ADC:
  - See “Die Temperature Status Register 0x11” and “Channel Average Current Status Register 0x12”.
- Programmable internal PWM clock generator:
  - See “PWM Registers” 0x30 – 0x36.
- Automated Built-in Self-Test:
  - See “Built-In Self Test (BIST) Status Register 0x10”.
- Programmable delay and retry on overcurrent protection:
  - See “OverCurrent Registers” 0x50 – 0x53.
- Flexible programmable interrupts:
  - See “Interrupt Registers” 0x20 – 0x2B.

- Optional Watchdog Timer:
    - See “Watchdog Timer Registers” 0x40 – 0xC5.

3.2. Application Examples

3.2.1. Generate a PWM waveform with duty cycle ratio 1:3000 and frequency 250 Hz.

This example is typical of a low duty cycle PWM waveform used in LED low dimming applications.

For the 50 MHz internal clock, the clock period (T_{CLK}) will be 1/(50 MHz) = 20 ns.

The number of clocks needed for a PWM waveform with period T_{PWM} is defined as

$$N = T_{PWM} \div (T_{CLK} \times P), \text{ where P is the prescaler value.}$$

Therefore, in this example, assuming a prescaler value of 1, N = 0.004 ÷ (20E-9 × 1) = 200,000.

The maximum number of clocks possible with a 16-bit period resolution is 65,536, therefore the prescaler, period and pulsewidth values must be calculated to provide the target frequency with the minimum error within an allowable number of clocks.

$$PW = N \div DC, \text{ where PW is pulsewidth}$$

$$T_{PWM} = PW \times N$$

In the example above, a prescaler value of 6 will deliver a frequency of 252.53 Hz (error 1%) with period 660 µs and pulsewidth 220 ns.

Therefore, program “PWM Period Register 0x31” with 660E-6/20E-9 = 33000 (Dec) or 0x80E8

Program “PWM Pulsewidth Register 0x32” with 220E-9/20E-9 = 11 (Dec) or 0x000B.

Figure 2 illustrates the process in a flow chart.

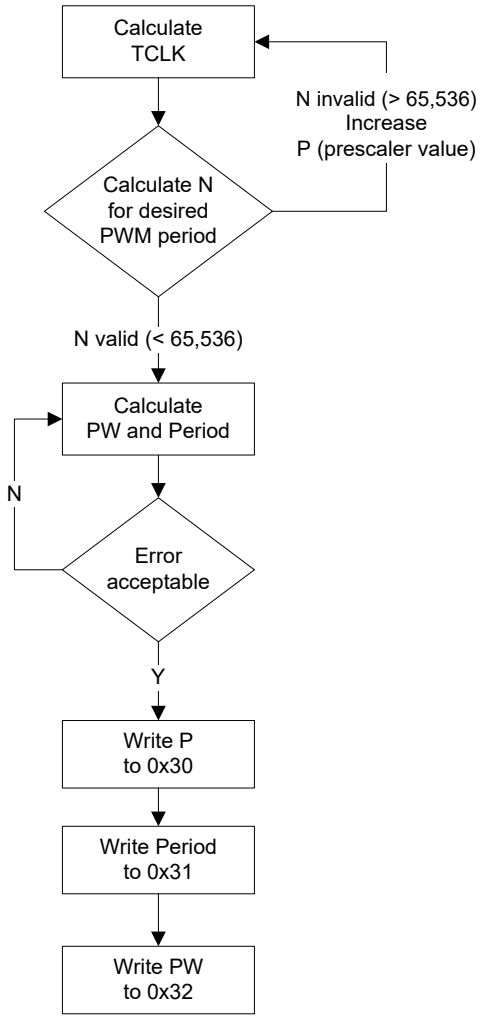


Figure 2. PWM low duty cycle example flowchart

3.2.2. PWM Mode Output Driver

To operate the device as a PWM output driver, execute the following steps

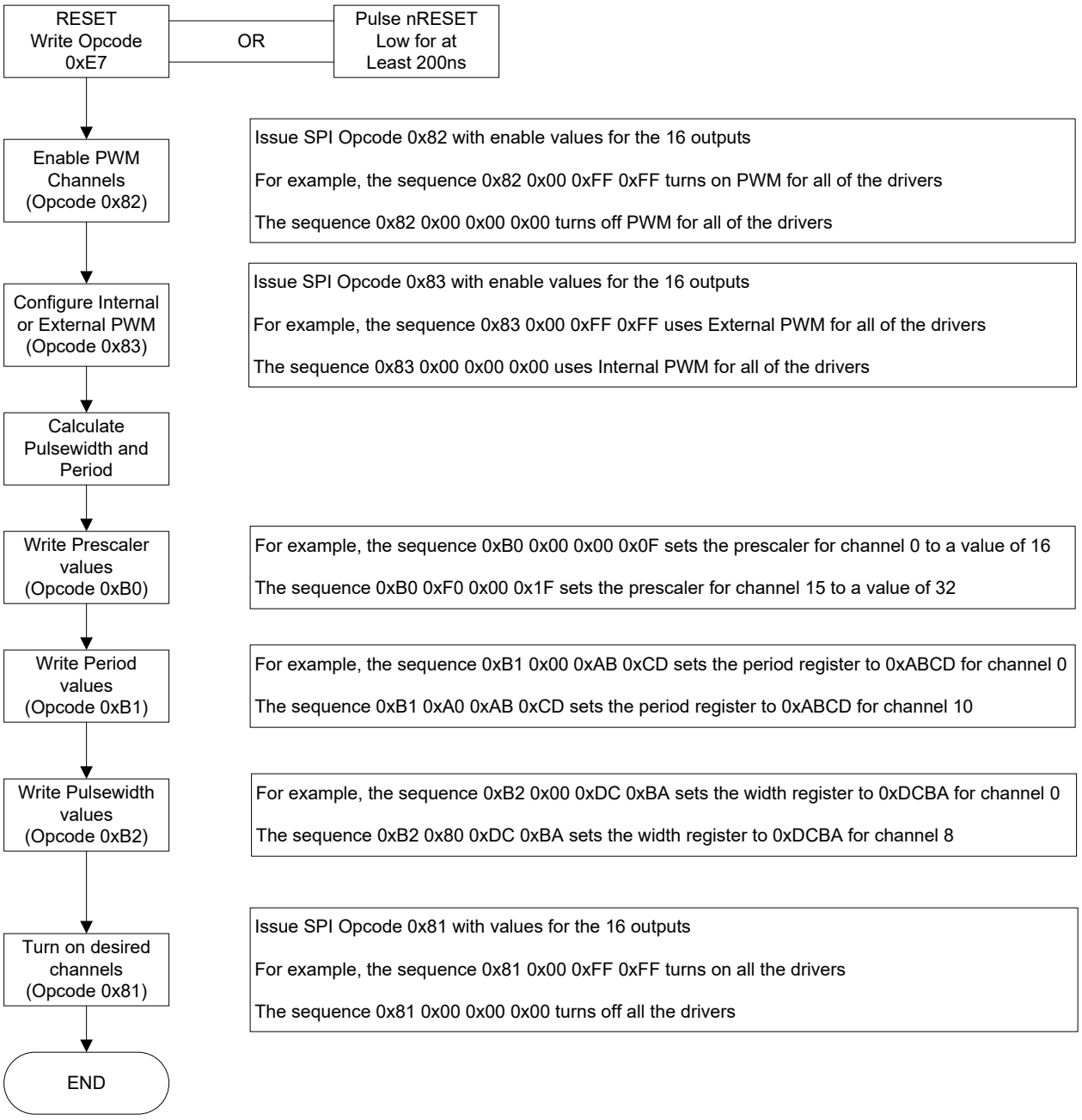


Figure 3. PWM output driver example

3.2.3. Overcurrent Retry Operation for Incandescent Lamp Loads

To enable OverCurrent Retry functionality, execute the following steps

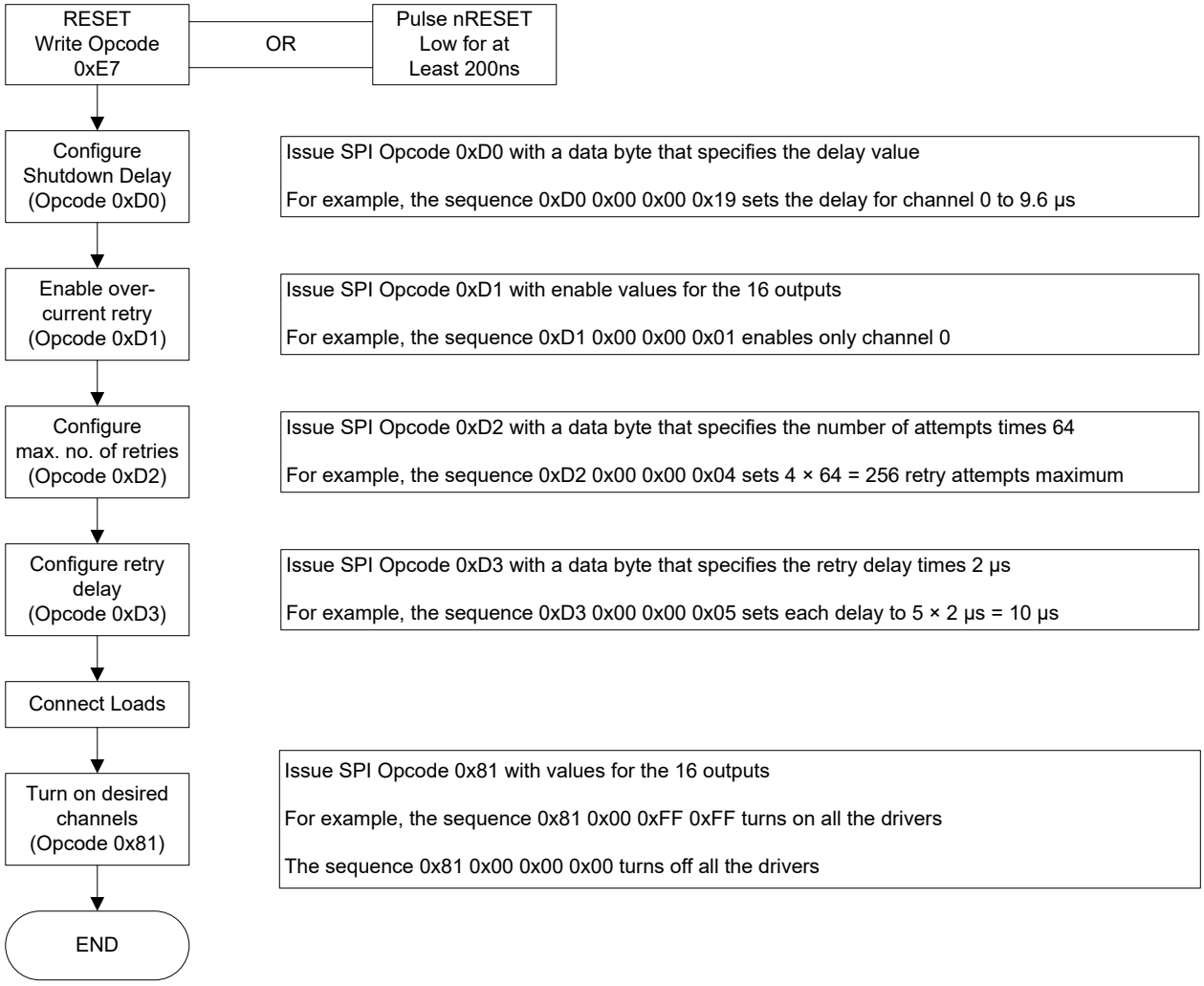


Figure 4. Overcurrent Retry example

The image below shows the relation between the configuration parameters and the retry process.

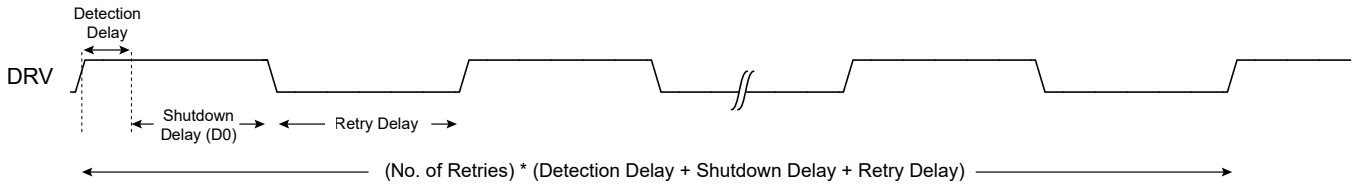
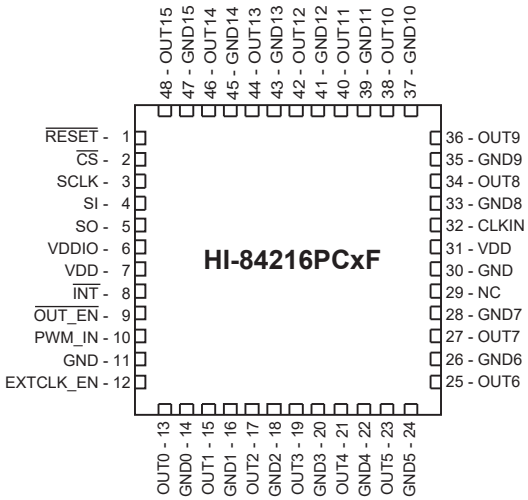


Figure 5. OverCurrent Retry Operation

4. Pin Diagram



48 - Pin Plastic 6mm x 6mm
Chip-Scale Package (QFN)

Figure 6. HI-84216PCxF QFN Package Pinout

5. Signal and Pin Descriptions

Pin	Signal Name	Function	Description
1	$\overline{\text{RESET}}$	Digital Input 50 kΩ Pull-Up	Reset, active low.
2	$\overline{\text{CS}}$	Digital Input	SPI Chip Select, active low. When asserted, this pin enables host read or write accesses to device registers via host SPI port. The SPI port operates in Slave mode. This pin is connected to the Slave Select output on the host SPI port.
3	SCLK	Digital Input	SPI clock pin.
4	SI	Digital Input	SPI Serial Input pin. This pin is connected to MOSI (Master Out - Slave In) pin on host SPI port.
5	SO	Digital Output	SPI Serial Output pin. This pin is connected to MISO (Master In - Slave Out) pin on host SPI port.
6	VDDIO	Power Supply	1.8V − 5.0V power supply for digital IO
7	VDD	Power Supply	3.3V − 5.0V power supply for analog circuitry
8	$\overline{\text{INT}}$	Digital Output	Interrupt pin. Open drain, active low.
9	$\overline{\text{OUT\_EN}}$	Digital Input	Output Enable, active low. Asserting this pin low will enable all outputs. Set this pin high to disable all outputs.
10	PWM_IN	Digital Input	Optional external PWM input.
11	GND	Power Supply	Power supply ground.
12	EXTCLK_EN	Digital Input	Enable optional external clock input (CLKIN). See pin 32.
13	OUT0	Analog Output	Low-side driver output, channel 0
14	GND0	Power Supply	Power supply ground, channel 0 (Note 1).
15	OUT1	Analog Output	Low-side driver output, channel 1
16	GND1	Power Supply	Power supply ground, channel 1
17	OUT2	Analog Output	Low-side driver output, channel 2
18	GND2	Power Supply	Power supply ground, channel 2
19	OUT3	Analog Output	Low-side driver output, channel 3
20	GND3	Power Supply	Power supply ground, channel 3
21	OUT4	Analog Output	Low-side driver output, channel 4
22	GND4	Power Supply	Power supply ground, channel 4
23	OUT5	Analog Output	Low-side driver output, channel 5
24	GND5	Power Supply	Power supply ground, channel 5
25	OUT6	Analog Output	Low-side driver output, channel 6

Pin	Signal Name	Function	Description
26	GND6	Power Supply	Power supply ground, channel 6
27	OUT7	Analog Output	Low-side driver output, channel 7
28	GND7	Power Supply	Power supply ground, channel 7
29	ADC_SYNC	Digital Output	This pin outputs a 60 ns pulse every time the ADC completes a measurement cycle. It may be used by the host to synchronize Channel Current and Die Temperature Status Register reads. If unused, this pin should be left floating.
30	GND	Power Supply	Power supply ground.
31	VDD	Power Supply	3.3V − 5.0V power supply for analog circuitry
32	CLKIN	Digital Input	Optional external clock input. An external clock may be connected if frequencies greater than the internal 50 MHz clock are desired. This feature must be enabled by setting pin 12, EXTCLK_EN.
33	GND8	Power Supply	Power supply ground, channel 8
34	OUT8	Analog Output	Low-side driver output, channel 8
35	GND9	Power Supply	Power supply ground, channel 9
36	OUT9	Analog Output	Low-side driver output, channel 9
37	GND10	Power Supply	Power supply ground, channel 10
38	OUT10	Analog Output	Low-side driver output, channel 10
39	GND11	Power Supply	Power supply ground, channel 11
40	OUT11	Analog Output	Low-side driver output, channel 11
41	GND12	Power Supply	Power supply ground, channel 12
42	OUT12	Analog Output	Low-side driver output, channel 12
43	GND13	Power Supply	Power supply ground, channel 13
44	OUT13	Analog Output	Low-side driver output, channel 13
45	GND14	Power Supply	Power supply ground, channel 14
46	OUT14	Analog Output	Low-side driver output, channel 14
47	GND15	Power Supply	Power supply ground, channel 15
48	OUT15	Analog Output	Low-side driver output, channel 15

Note 1: All power supply grounds are connected internally. For optimal current flow and power dissipation in a given channel, connect the corresponding channel ground. E.g. if using channel 0, connect GND0.

6. SPI Opcode and Register Summary

The device uses a SPI (Serial Peripheral Interface) for host access to internal registers for configuration and status updates. The SPI host interface operates using an 8-bit opcode followed by an 8-bit parameter and two 8-bit data bytes to provide the 16-bit data which is read from or written to each register. This is illustrated in Figure 7. The first data byte corresponds to register bits [15:8], the second data byte to register bits [7:0]. Read and write operations are distinguished by flipping the MSB in the opcode. For example, opcode 0x00 reads the Configuration Register, opcode 0x80 writes the Configuration Register.

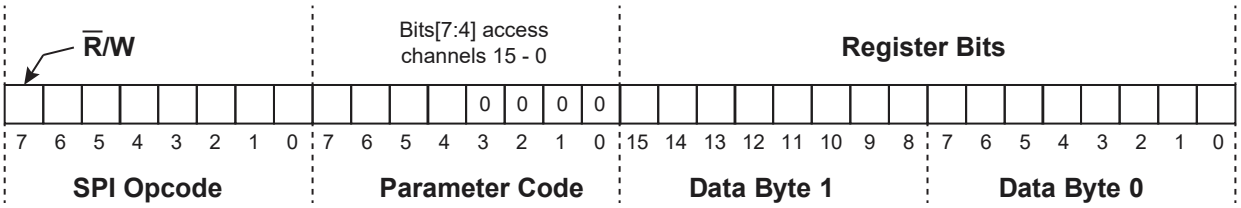


Figure 7. SPI Register Access

Table 1 summarizes the SPI Opcodes and register functions. In normal operation, select registers access individual channels by utilizing bits[7:4] of the parameter code to identify the channel, i.e. 0000 identifies channel 0, 0001 identifies channel 1, ... , 1111 identifies channel 15 respectively (see individual register sections below).

Registers providing status on each of the 16 channels utilize each bit[15:0] (bit 15 represents channel 15, bit 14 represents channel 14, bit 0 represents channel 0, etc. See for example “Channel High Current Status Register 0x14”.

See Section “7. Registers” for a more detailed description of the registers and bit functions.

Note: Undefined opcodes (e.g.0x07) should not be used as this may result in unexpected behavior.

Table 1. SPI Opcodes and Register Functions

Opcode		Param.	Register Read/Write	Data[15:8]	Data[7:0]
Read	Write				
Configuration Registers					
0x00	0x80	0x00	“Configuration Register 0x00”	0x00	See Section 7.1.1
0x01	0x81	0x00	“Channel Turn-On Register 0x01”	CH[15:8]	CH[7:0]
0x02	0x82	0x00	“Individual Channel PWM Enable Register 0x02”	CH[15:8]	CH[7:0]
0x03	0x83	0x00	“Channel PWM Source Enable Register 0x03”	CH[15:8]	CH[7:0]
0x04	0x84	–	Unused.	–	–
0x05	0x85	[7:4]	“Current Limit Threshold Register 0x05”	T_High[15:8]	T_Low[7:0]
0x06	0x86	0x00	“Channel Thermal Shutdown Disable Register 0x06”	CH[15:8]	CH[7:0]
Status Registers					
0x10	0x90	0x00	“Built-In Self Test (BIST) Status Register 0x10”	0x00	See Section 7.2.1

Opcode		Param.	Register Read/Write	Data[15:8]	Data[7:0]
Read	Write				
0x11	–	0x00	“Die Temperature Status Register 0x11”	0x00	TEMP[7:0]
0x12	–	[7:4]	“Channel Average Current Status Register 0x12”	0x00	I_Ave[7:0]
0x13	–	[7:4]	“Channel Recent Current Status Register 0x13”	0x00	I_Ave(R)[7:0]
0x14	–	0x00	“Channel High Current Status Register 0x14”	CH[15:8]	CH[7:0]
0x15	–	0x00	“Channel Low Current Status Register 0x15”	CH[15:8]	CH[7:0]
0x16	–	0x00	“Channel Over-temperature Status Register 0x16”	CH[15:8]	CH[7:0]
Interrupt Registers					
0x20	–	0x00	“Interrupt Status Register 0x20”	0x00	See Section 7.3.1
0x21	–	0x00	“Channel Overcurrent Fault Pending Interrupt Register 0x21”	CH[15:8]	CH[7:0]
0x22	–	0x00	“Channel Current High Pending Interrupt Register 0x22”	CH[15:8]	CH[7:0]
0x23	–	0x00	“Channel Current Low Pending Interrupt Register 0x23”	CH[15:8]	CH[7:0]
0x24	–	0x00	“Channel Over-Temperature Shutdown Pending Interrupt Register 0x24”	CH[15:8]	CH[7:0]
0x25	0xA5	0x00	“Global Interrupt Enable Register 0x25”	See Section 7.3.6	
0x26	0xA6	0x00	“Channel Overcurrent Fault Interrupt Enable Register 0x26”	CH[15:8]	CH[7:0]
0x27	0xA7	0x00	“Channel Current High Interrupt Enable Register 0x27”	CH[15:8]	CH[7:0]
0x28	0xA8	0x00	“Channel Current Low Interrupt Enable Register 0x28”	CH[15:8]	CH[7:0]
0x29	0xA9	0x00	“Channel Overcurrent Fault Interrupt Output Enable Register 0x29”	CH[15:8]	CH[7:0]
0x2A	0xAA	0x00	“Channel Current High Interrupt Output Enable Register 0x2A”	CH[15:8]	CH[7:0]
0x2B	0xAB	0x00	“Channel Current Low Interrupt Output Enable Register 0x2B”	CH[15:8]	CH[7:0]
PWM Configuration Registers					
0x30	0xB0	[7:4]	“PWM Prescaler Register 0x30”	0x00	PWM[4:0]
0x31	0xB1	[7:4]	“PWM Period Register 0x31”	PWM_Period[15:8]	PWM_Period[7:0]
0x32	0xB2	[7:4]	“PWM Pulsewidth Register 0x32”	PWM_Width[15:8]	PWM_Width[7:0]
0x33	0xB3	0x00	“PWM Parallel Mask Register 0x33”	CH[15:8]	CH[7:0]
0x34	0xB4	0x00	“PWM Parallel Prescaler Register 0x34”	0x00	PWM[4:0]
0x35	0xB5	0x00	“PWM Parallel Period Register 0x35”	PWM_Period[15:8]	PWM_Period[7:0]
0x36	0xB6	0x00	“PWM Parallel Pulsewidth Register 0x36”	PWM_Width[15:8]	PWM_Width[7:0]

Opcode		Param.	Register Read/Write	Data[15:8]	Data[7:0]
Read	Write				
Watchdog Configuration Registers					
0x40	0xC0	0x00	“Watchdog Timer Enable Register 0x40”	CH[15:8]	CH[7:0]
0x41	0xC1	0x00	“Watchdog Timer Quiet Time Register 0x41”	WDT_Active[15:8]	WDT_Active[7:0]
0x42	0xC2	0x00	“Watchdog Timer Active Time Register 0x42”	WDT_Quiet[15:8]	WDT_Quiet[7:0]
0x43	–	0x00	“Watchdog Timer Active Count Register 0x43”	[15:8]	[7:0]
0x44	–	0x00	“Watchdog Timer Quiet Count Register 0x44”	[15:8]	[7:0]
–	0xC5	0x5A	“Watchdog Timer Strobe Opcode 0xC5”	0x80	0x01
OverCurrent Configuration Registers					
0x50	0xD0	[7:4]	“Overcurrent Shutdown Delay Register 0x50”	0x00	Delay[5:0]
0x51	0xD1	0x00	“Overcurrent Retry Enable Register 0x51”	CH[15:8]	CH[7:0]
0x52	0xD2	0x00	“Overcurrent Retry Attempts Register 0x52”	0x00	[7:0]
0x53	0xD3	0x00	“Overcurrent Retry Delay Register 0x53”	[15:8]	[7:0]
–	0xE7	0x7E	“Software Reset”	–	–

7. Registers

The SPI host interface accesses 16-bit registers using an 8-bit opcode (Read or Write), followed by an 8-bit parameter code followed by two 8-bit data bytes. See “Table 1. SPI Opcodes and Register Functions” for a summary of SPI opcodes and parameter codes. Figure 8 gives an example of a SPI read/write.

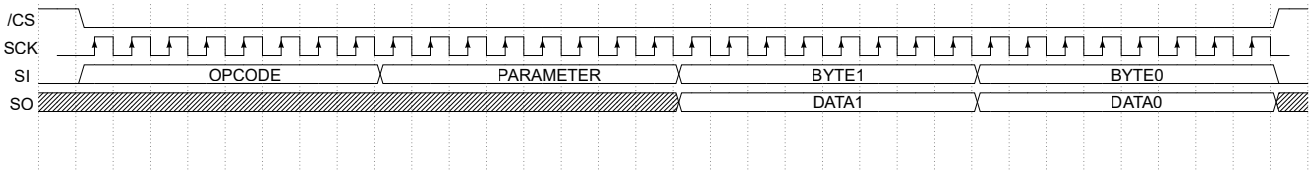


Figure 8. SPI Read/Write Example

7.1. Set-Up and Configuration Registers

7.1.1. Configuration Register 0x00

Read: SPI Opcode: 0x00

Write: SPI Opcode: 0x80

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 8	R/W	0	Not Used.
7	R/W	0	Setting this bit to logic “1” enables die temperature monitoring. This bit must be set in order to read the die temperature value from the “Die Temperature Status Register 0x11”. If this bit is set to logic “0”, thermal fail-safe protection will still be enabled for each channel (unless disabled by setting the corresponding channel bit in “Channel Thermal Shutdown Disable Register 0x06”), however the actual channel temperature value will not be recorded.
6	R/W	0	Setting this bit to logic “1” enables built-in self test mode utilizing the “High” internal dummy load (see “Built-In Self Test (BIST) Status Register 0x10”)
5	R/W	0	Setting this bit to logic “1” enables built-in self test mode utilizing the “Low” internal dummy load (see “Built-In Self Test (BIST) Status Register 0x10”).
4	R/W	0	Enable external PWM fail-safe mode. Setting this bit enables detection of a fault on the external PWM drive. A fault is defined as loss of detection of a rising edge of the PWM signal within a 50 ms period (i.e. 20 Hz min.). An interrupt will be generated (if enabled).

<table>
<tr><th>Bit No.</th><th>R/W</th><th>Reset</th><th>Bit Description</th></tr>
<tr><td rowspan="10">3 − 1</td><td rowspan="10">R/W</td><td rowspan="10">000</td><td>Average Channel Current Accuracy.
The driver output current is sequentially measured continuously to an 8-bit accuracy (4.38 mA/LSB) through each of the turned-on channels in turn. These bits specify the number of times the current is sampled before the average is recorded (once per cycle) in the “Channel Average Current Status Register 0x12”. The higher the sampling average, the greater the accuracy, however the measurement time is significantly increased.</td></tr>
<tr><td>
<table>
<tr><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Accuracy</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1 sample (Default)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4 sample average</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>16 sample average</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>64 sample average</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>256 sample average</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1,024 sample average</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>4,096 sample average</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>16,384 sample average</td></tr>
</table>
</td></tr>
<tr><td>0 (LSB)</td><td>R/W</td><td>0</td><td>Pulse/$\overline{\text{Level}}$ Interrupt.
When this bit is logic “1”, the $\overline{\text{INT}}$ output generates a negative pulse when an enabled interrupt event occurs.
When this bit is logic “0”, the $\overline{\text{INT}}$ output will be a continuous low level output when an enabled interrupt event occurs.</td></tr>
</table>

7.1.2. Channel Turn-On Register 0x01

Read: SPI Opcode: 0x01

Write: SPI Opcode: 0x81

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Set bits [15:0] to Turn On the corresponding channel number. To drive a load, a channel must be turned on by setting the corresponding bit in this register. If a bit is logic “0”, the corresponding channel is Turned Off. **Note:** If a channel has been turned off due to a thermal fail-safe or a watchdog timer fault, the corresponding channel bit will be reset and the channel will remain turned off. The host must write a logic “1” to the corresponding bit in this register to turn the channel back on.

7.1.3. Individual Channel PWM Enable Register 0x02

Read: SPI Opcode: 0x02

Write: SPI Opcode: 0x82

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	If bits [15:0] are logic “1”, PWM drive is enabled for the corresponding channel number. If bits [15:0] are logic “0”, the corresponding channel input is driven continuously.

7.1.4. Channel PWM Source Enable Register 0x03

Read: SPI Opcode: 0x03

Write: SPI Opcode: 0x83

Parameter: 0x00

This register selects the PWM source on a per-channel basis (either external via the PWM_IN pin or internally generated). PWM drive must also be enabled by setting the corresponding channel bits in the “Individual Channel PWM Enable Register 0x02” above.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	If bits [15:0] are logic “1”, External PWM drive via the PWM_IN pin is enabled for the corresponding channel number. If bits [15:0] are logic “0”, Internal PWM drive is enabled for the corresponding channel number.

7.1.5. Current Limit Threshold Register 0x05

Read: SPI Opcode: 0x05

Write: SPI Opcode: 0x85

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

This register sets the current limits for overcurrent detection (upper threshold limit) and open load detection (lower threshold limit) in each channel. An interrupt will be generated, if enabled. The recommended maximum operating current for each channel is 250mA per channel (4.38mA/LSB).

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 8	R/W	0xFF	Upper Threshold Current Limit. Bits [15:8] set the upper limit above which an interrupt is generated if the average channel current exceeds this value. The maximum programmable limit with 8 bits is approximately 1.1 A (default), however any value greater than 600 mA will result in channel shutdown following the user-programmed overcurrent fault delay time (see “Overcurrent Shutdown Delay Register 0x50”). To set an upper limit of 250 mA (recommended maximum), program these bits with 250/4.38 = 57 decimal or 0x39.
7 − 0 (LSB)	R/W	0	Lower Threshold Current Limit. Bits [7:0] set the lower limit below which an interrupt is generated if the average channel current falls below this value. The minimum value is 0.

7.1.6. Channel Thermal Shutdown Disable Register 0x06

Read: SPI Opcode: 0x06

Write: SPI Opcode: 0x86

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	If bits [15:0] are logic “1”, thermal shutdown is disabled for the corresponding channel number. If bits [15:0] are logic “0” (default), thermal shutdown is enabled for the corresponding channel number. If the die temperature exceeds the maximum fail-safe temperature at the driver (approximately 215°C) for a specific channel, then that channel will shut off.

7.2. Status Registers

7.2.1. Built-In Self Test (BIST) Status Register 0x10

Read: SPI Opcode: 0x10

Write: SPI Opcode: 0x90

Parameter: 0x00

The device utilizes a single 8-bit A/D converter to sequentially measure the die temperature and the current of each of the turned-on 16 channels. The sequence includes a BIST which comprises two measurements (High and Low) for self-testing the A/D and corresponding digital logic. Each A/D measurement takes 150µs.

For noise tolerance, the BIST High test will pass with an ADC result of 0xFFFF or 0xFFFE. Similarly, the BIST Low test will pass with 0x0001 or 0x0000. The die temperature and two BIST tests are disabled by default and can be enabled by setting bits[7:5] in the “Configuration Register 0x00”.

The status of BIST test results are monitored by reading register 0x10. A BIST High/Low Pass/Fail will result in the corresponding bit being set below.

If both the Pass and Fail bits are asserted, the device has seen both a passing and failing measurement since the last reset. If enabled by “Global Interrupt Enable Register 0x25”, an interrupt will be asserted on “Interrupt Status Register 0x20” on the first occurrence of either a BIST High or BIST Low test fail after reset.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 8	R/W	0	Not Used.
7 − 4	R/W	0	Not Used.
3	R/W	0	If this bit is logic “1”, BIST High test Pass
2	R/W	0	If this bit is logic “1”, BIST Low test Pass.
1	R/W	0	If this bit is logic “1”, BIST High test Fail.
0 (LSB)	R/W	0	If this bit is logic “1”, BIST Low test Fail.

7.2.2. Die Temperature Status Register 0x11

Read: SPI Opcode: 0x11

Write: SPI Opcode: Read Only

Parameter: 0x00

This register contains an 8-bit value equivalent to the approximate die temperature. Resolution is 6°C/LSB, with 30 decimal representing –55°C, 42 decimal representing 22°C and 72 decimal representing 200°C. To record/read the die temperature value from this register, die temperature monitoring must be first be enabled by setting bit 7 of “Configuration Register 0x00”.

Bit No.	R	Reset	Bit Description
15 (MSB) − 8	R	0	Not Used.
7 − 0 (LSB)	R	0	Approximate die temperature.

7.2.3. Channel Average Current Status Register 0x12

Read: SPI Opcode: 0x12

Write: SPI Opcode: Read Only

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

This register contains an 8-bit value equivalent to the individual channel average current. Channels are accessed individually with bits[7:4] of the parameter code. The resolution is 4.38mA/LSB. The accuracy of the average current value is based on the sampling average defined by bits[3:1] in “Configuration Register 0x00”.

Bit No.	R	Reset	Bit Description
15 (MSB) − 8	R	0	Not Used.
7 − 0 (LSB)	R	0	Channel average current.

7.2.4. Channel Recent Current Status Register 0x13

Read: SPI Opcode: 0x13

Write: SPI Opcode: Read Only

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

This register contains an 8-bit value equivalent to the most recently updated channel current. In cases where a high sampling average was programmed by bits[3:1] in “Configuration Register 0x00”, resulting in longer update times, it may be useful to read this register to obtain an immediate value rather than wait for the next average current update in the “Channel Average Current Status Register 0x12”.

Bit No.	R	Reset	Bit Description
15 (MSB) − 8	R	0	Not Used.
7 − 0 (LSB)	R	0	Most recent channel average current.

7.2.5. Channel High Current Status Register 0x14

Read: SPI Opcode: 0x14

Write: SPI Opcode: Read Only

Parameter: 0x00

Each bit in this register represents a status bit for the equivalent channel number (bit 0 represents channel 0, bit 1 represents channel 1, bit 15 represents channel 15, etc.

If a bit reads logic “1” then the corresponding channel average current exceeds the upper threshold current limit set by bits [15:8] in the “Current Limit Threshold Register 0x05”. The bit will remain set while the channel average current is above the upper threshold limit and will reset when the current drops below the limit.

Bit No.	R	Reset	Bit Description
15 (MSB) −0	R	0	Logic “1” signifies the upper threshold current limit has been exceeded for the corresponding channel 15 − 0 respectively.

7.2.6. Channel Low Current Status Register 0x15

Read: SPI Opcode: 0x15

Write: SPI Opcode: Read Only

Parameter: 0x00

If a bit reads logic “1” then the corresponding channel average current is less than the lower threshold current limit set by bits [7:0] in the “Current Limit Threshold Register 0x05”. The bit will remain set while the channel average current is below the lower threshold limit and will reset when the current exceeds the lower limit.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0	R	0	Logic “1” signifies the average current is less than the lower threshold current limit for the corresponding channel 15 − 0 respectively.

7.2.7. Channel Over-temperature Status Register 0x16

Read: SPI Opcode: 0x16

Write: SPI Opcode: Read Only

Parameter: 0x00

If a bit reads logic “1” then the corresponding channel temperature has exceeded the maximum fail-safe temperature (approximately 215°C) and the channel has been shutdown (assuming thermal fail-safe protection has not been disabled by setting the corresponding channel bit in the “Channel Thermal Shutdown Disable Register 0x06”). Normal channel operation must be re-established following a thermal shutdown by turning the channel back on, (i.e. writing the corresponding channel bit in the “Channel Turn-On Register 0x01”). All other programmed channel parameters will be retained.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0	R	0	Logic “1” signifies the channel temperature has exceeded the maximum fail-safe temperature for the corresponding channel 15 − 0 respectively.

7.3. Interrupt Registers

The device has a flexible interrupt scheme, allowing interrupts to be generated on a global basis or on a channel-by-channel basis. To generate interrupts on a per channel basis, they must be individually enabled. This is explained in more detail below.

7.3.1. Interrupt Status Register 0x20

Read: SPI Opcode: 0x20

Write: SPI Opcode: Read Only

Parameter: 0x00

This register allows the user to identify all pending interrupts with one register read. The register is **cleared on read**. Note that if a "level" interrupt type is selected (bit[0] of "Configuration Register 0x00" is set to logic "0"), then reading this register will also de-assert the $\overline{\text{INT}}$ pin. **Interrupts must be enabled** by setting the corresponding bit in the "Global Interrupt Enable Register 0x25" (see below). If an interrupt is enabled by setting a bit in the "Global Interrupt Enable Register 0x25", the corresponding bit in this register will be asserted following the interrupt causing event.

Bit No.	R	Reset	Bit Description
15 (MSB) − 8	R	0	Not Used.
7	R	0	BIST Interrupt. This bit will be set to logic "1" following the first occurrence of a BIST High or BIST Low test fail. . It will be asserted on the first occurrence of either a BIST High or BIST Low test (see also "Built-In Self Test (BIST) Status Register 0x10").
6	R	0	Channel High Current Interrupt. This bit will be asserted when **any** channel average current exceeds the Upper Threshold Current Limit set by bits [15:8] in the "Current Limit Threshold Register 0x05". To determine the channel(s) causing the interrupt, interrupts must **also** be enabled on an individual channel basis via the "Channel Current High Interrupt Enable Register 0x27" and serviced via the "Channel Current High Pending Interrupt Register 0x22".
5	R	0	Channel Low Current Interrupt. This bit will be asserted when **any** channel average current drops below the Lower Threshold Current Limit set by bits [7:0] in the "Current Limit Threshold Register 0x05". To determine the channel(s) causing the interrupt, interrupts must **also** be enabled on an individual channel basis via the "Channel Current Low Interrupt Enable Register 0x28" and serviced via the "Channel Current Low Pending Interrupt Register 0x23".

Bit No.	R	Reset	Bit Description
4	R	0	Channel Temperature Fail-Safe Shutdown Interrupt. This bit will be asserted when any channel temperature has exceeded the maximum fail-safe temperature (approximately 215°C) and the channel has been switched off. Normal channel operation must be re-established following a thermal shutdown by turning the channel back on, (i.e. writing the corresponding channel bit in the “Channel Turn-On Register 0x01”), however all other programmed channel parameters will be retained. Over-Temperature Shutdown Interrupts for **all** channels are enabled by setting bit 4 of the “Global Interrupt Enable Register 0x25”. To determine the channel(s) causing the interrupt, the “Channel Over-Temperature Shutdown Pending Interrupt Register 0x24” may be read.
3	R	0	External PWM Input Source Failure Interrupt. This bit will be asserted when there is a fault in the external PWM input source, e.g. loss of signal. The rising edge of the PWM input source is continuously monitored. A fault is defined as loss of detection of a rising edge of the PWM signal within a 50 ms period (i.e. 20 Hz min.).
2	R	0	Not Used.
1	R	0	Watchdog Timer Fault (WDT) Interrupt. This bit will be asserted when the host has failed to provide the specified write strobe signal within the programmed active watchdog timer interval and a channel has shut down as a result. Normal channel operation must be re-established following a WDT fault by turning the channel back on, (i.e. writing the corresponding channel bit in the “Channel Turn-On Register 0x01”), however all other programmed channel parameters will be retained. Each channel has its own individual WDT. See “Watchdog Timer Registers” for more detail.
0 (LSB)	R	0	Overcurrent Fault Interrupt. This bit will be asserted when a channel has incurred a overcurrent fault and the channel has been switched off as a result. A overcurrent fault occurs when a channel current exceeds 600 mA for longer than the programmed overcurrent fault delay (see “Overcurrent Shutdown Delay Register 0x50”). To determine the channel(s) causing the interrupt, interrupts must **also** be enabled on an individual channel basis via the “Channel Overcurrent Fault Interrupt Enable Register 0x26” and serviced via the “Channel Overcurrent Fault Pending Interrupt Register 0x21”.

7.3.2. Channel Overcurrent Fault Pending Interrupt Register 0x21

Read: SPI Opcode: 0x21

Write: SPI Opcode: Read Only

Parameter: 0x00

Each bit in this register provides a pending interrupt for the equivalent channel number (bit 0 represents channel 0, bit 1 represents channel 1, bit 15 represents channel 15, etc.). If interrupts are enabled on a per channel basis by setting bits in the ”Channel Overcurrent Fault Interrupt Enable Register 0x26”, the corresponding bit in this register will be asserted following an overcurrent fault for that channel. If an interrupt is not enabled, the corresponding pending interrupt bit will not be set.

A overcurrent fault occurs when a channel current exceeds 600 mA for longer than the programmed overcurrent fault delay defined in the “Overcurrent Shutdown Delay Register 0x50”, and the channel has been switched off as a result. Bits are **set on fault detection** and remain set until this register is read, regardless of whether the fault is still present. The register is **cleared when read**.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0	R	0	Logic “1” signifies a overcurrent fault has occurred in the corresponding channel 15 − 0 respectively.

7.3.3. Channel Current High Pending Interrupt Register 0x22

Read: SPI Opcode: 0x22

Write: SPI Opcode: Read Only

Parameter: 0x00

Each bit in this register provides a pending interrupt for the equivalent channel number. If interrupts are enabled on a per channel basis by setting bits in the “Channel Current High Interrupt Enable Register 0x27”, the corresponding bit in this register will be asserted when the channel average current exceeds the Upper Threshold Current Limit set by bits [15:8] in the “Current Limit Threshold Register 0x05”. If an interrupt is not enabled, the interrupt causing event will be ignored and the corresponding bit is not set.

Bits are **set on transition** to the interrupt causing event and remain set until this register is read, regardless of whether the event is still present. The register is **cleared when read**.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0	R	0	Logic “1” signifies the channel average current exceeds the Upper Threshold Current Limit for the corresponding channel 15 − 0 respectively.

7.3.4. Channel Current Low Pending Interrupt Register 0x23

Read: SPI Opcode: 0x23

Write: SPI Opcode: Read Only

Parameter: 0x00

Each bit in this register provides a pending interrupt for the equivalent channel number. If interrupts are enabled on a per channel basis by setting bits in the “Channel Current Low Interrupt Enable Register 0x28”, the corresponding bit in this register will be asserted when the channel average current drops below the Lower Threshold Current Limit set by bits [7:0] in the “Current Limit Threshold Register 0x05”. If an interrupt is not enabled, the interrupt causing event will be ignored and the corresponding bit is not set.

Bits are **set on transition** to the interrupt causing event and remain set until this register is read, regardless of whether the event is still present. The register is **cleared when read**.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0	R	0	Logic “1” signifies the channel average current is less than the Lower Threshold Current Limit for the corresponding channel 15 − 0 respectively.

7.3.5. Channel Over-Temperature Shutdown Pending Interrupt Register 0x24

Read: SPI Opcode: 0x24

Write: SPI Opcode: Read Only

Parameter: 0x00

Each bit in this register provides a pending interrupt for the equivalent channel number. If interrupts are enabled by setting bit 4 of the “Global Interrupt Enable Register 0x25”, the corresponding bit in this register will be asserted when the channel temperature exceeds the maximum fail-safe temperature (approximately 215°C) and the channel has been switched off. If interrupts are not enabled for over-temperature shutdown, the corresponding pending interrupt bit is not set.

Bits are **set on transition** to the fault and remain set until the register is read, regardless of whether the fault is still present. The register is **cleared when read**.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0	R	0	Logic “1” signifies the channel temperature has exceeded the maximum fail-safe temperature in the corresponding channel 15 − 0 respectively.

7.3.6. Global Interrupt Enable Register 0x25

Read: SPI Opcode: 0x25

Write: SPI Opcode: 0xA5

Parameter: 0x00

This register provides the ability to globally enable both hardware interrupts (bits[15:8]), or host serviceable software interrupts (bits[7:0]) .

Setting a bit in this register to logic “1” will enable the described interrupt. Bits[15:8] enable a hardware interrupt resulting in assertion of the $\overline{\text{INT}}$ pin following the interrupt causing event. Setting bits[7:0] will result in the corresponding bits in the “Interrupt Status Register 0x20” being set following the event. In this way, the $\overline{\text{INT}}$ pin may be reserved for higher priority interrupts and lower priority interrupts may be serviced by polling “Interrupt Status Register 0x20”

Bit No.	R/W	Reset	Bit Description
15 (MSB)	R/W	0	BIST Interrupt Output Enable.
14	R/W	0	Channel Current High Interrupt Output Enable.
13	R/W	0	Channel Current Low Interrupt Output Enable.
12	R/W	0	Channel Over-Temperature Shutdown Interrupt Output Enable.
11	R/W	0	PWM Input Source Failure Interrupt Output Enable.
10	R/W	0	Not Used.
9	R/W	0	Watchdog Timer Fault (WDT) Interrupt Output Enable.
8	R/W	0	Overcurrent Fault Interrupt Output Enable.
7	R/W	0	BIST Interrupt Enable.
6	R/W	0	Channel Current High Interrupt Enable.
5	R/W	0	Channel Current Low Interrupt Enable.
4	R/W	0	Channel Over-Temperature Shutdown Interrupt Enable.
3	R/W	0	External PWM Input Source Failure Interrupt Enable.
2	R/W	0	Not Used.
1	R/W	0	Watchdog Timer Fault (WDT) Interrupt Enable.
0 (LSB)	R/W	0	Overcurrent Fault Interrupt Enable.

7.3.7. Channel Overcurrent Fault Interrupt Enable Register 0x26

Read: SPI Opcode: 0x26

Write: SPI Opcode: 0xA6

Parameter: 0x00

This register enables interrupts for overcurrent faults on a per channel basis. Bits in this register must be set to logic “1” to set the equivalent pending interrupt bit in the “Channel Overcurrent Fault Pending Interrupt Register 0x21”.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables an interrupt to occur for overcurrent faults on the corresponding channel 15 − 0 respectively.

7.3.8. Channel Current High Interrupt Enable Register 0x27

Read: SPI Opcode: 0x27

Write: SPI Opcode: 0xA7

Parameter: 0x00

This register enables interrupts to occur on a per channel basis when the channel average current exceeds the Upper Threshold Current Limit set by bits [15:8] in the “Current Limit Threshold Register 0x05”. Bits in this register must be set to logic “1” to set the equivalent pending interrupt bit in the “Channel Current High Pending Interrupt Register 0x22”.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables an interrupt to occur when the channel average current exceeds the Upper Threshold Current Limit on the corresponding channel 15 − 0 respectively.

7.3.9. Channel Current Low Interrupt Enable Register 0x28

Read: SPI Opcode: 0x28

Write: SPI Opcode: 0xA8

Parameter: 0x00

This register enables interrupts to occur on a per channel basis when the channel average current is less than the Lower Threshold Current Limit set by bits [7:0] in the “Current Limit Threshold Register 0x05”. Bits in this register must be set to logic “1” to set the equivalent pending interrupt bit in the “Channel Current Low Pending Interrupt Register 0x23”.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables an interrupt to occur when the channel average current is less than the Lower Threshold Current Limit on the corresponding channel 15 − 0 respectively.

7.3.10. Channel Overcurrent Fault Interrupt Output Enable Register 0x29

Read: SPI Opcode: 0x29

Write: SPI Opcode: 0xA9

Parameter: 0x00

This register enables hardware interrupts for overcurrent faults on a per channel basis. This results in assertion of the $\overline{INT}$ pin following an overcurrent fault for any of the turned-on channels. The channel causing the fault may be determined by reading the “Channel Overcurrent Fault Pending Interrupt Register 0x21” (interrupts must **also** be enabled on a per channel basis by setting the equivalent bit in the “Channel Overcurrent Fault Interrupt Enable Register 0x26”).

Bit No.	R/W	Reset	Bit Description
15 (MSB) −0	R/W	0	Setting a bit to logic “1” enables a hardware interrupt to occur for overcurrent faults on the corresponding channel 15 − 0 respectively. The $\overline{INT}$ pin will be asserted following the interrupt causing event for any of the turned-on channels.

7.3.11. Channel Current High Interrupt Output Enable Register 0x2A

Read: SPI Opcode: 0x2A

Write: SPI Opcode: 0xAA

Parameter: 0x00

This register enables hardware interrupts on a per channel basis for when the channel average current exceeds the Upper Threshold Current Limit set by bits [15:8] in the “Current Limit Threshold Register 0x05”. When this condition occurs for any turned-on channel, the $\overline{INT}$ pin will be asserted. The channel causing the fault may be determined by reading the “Channel Current High Pending Interrupt Register 0x22” (interrupts must **also** be enabled on a per channel basis by setting the equivalent bit in the “Channel Current High Interrupt Enable Register 0x27”).

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables a hardware interrupt to occur when the channel average current exceeds the Upper Threshold Current Limit on the corresponding channel 15 − 0 respectively. The $\overline{INT}$ pin will be asserted following the interrupt causing event for any of the turned-on channels.

7.3.12. Channel Current Low Interrupt Output Enable Register 0x2B

Read: SPI Opcode: 0x2B

Write: SPI Opcode: 0xAB

Parameter: 0x00

This register enables hardware interrupts on a per channel basis for when the channel average current is less than the Lower Threshold Current Limit set by bits [7:0] in the “Current Limit Threshold Register 0x05”. When this condition occurs for any turned-on channel, the $\overline{INT}$ pin will be asserted. The channel causing the fault may be determined by reading the “Channel Current Low Pending Interrupt Register 0x23” (interrupts must **also** be enabled on a per channel basis by setting the equivalent bit in the “Channel Current Low Interrupt Enable Register 0x28”).

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables a hardware interrupt to occur when the channel average current is less than the Lower Threshold Current Limit on the corresponding channel 15 − 0 respectively. The $\overline{INT}$ pin will be asserted following the interrupt causing event for any of the turned-on channels.

7.4. PWM Registers

The device uses an internal PWM clock generator which is fully programmable over the SPI bus for each channel and does not require the digital input (PWM_IN) to drive the outputs. A wide frequency range of 24 Hz to 48 kHz is possible, with a 16-bit resolution period and pulse width (see “PWM Period Register 0x31” and “PWM Pulsewidth Register 0x32”). A programmable 5-bit prescaler allows division of the internal 50 MHz clock up to a maximum of 32, enabling the programmability of very low duty cycles (see “PWM Prescaler Register 0x30”). For example, a 3000:1 LED dimming ratio is easily achieved (see Section “3.2.1. Generate a PWM waveform with duty cycle ratio 1:3000 and frequency 250 Hz.” on page 11).

For applications requiring modification of PWM parameters **simultaneously** on multiple channels (e.g. LED dimming applications requiring dimming of all LEDs simultaneously), the user should use the “PWM Parallel Mask Register 0x33” to define which channels require parallel operation and the “PWM Parallel Prescaler Register 0x34”, “PWM Parallel Period Register 0x35” and “PWM Parallel Pulsewidth Register 0x36” to program the prescaler, period and pulsewidth respectively for these parallel channels.

NOTE: Since the internal ADC works in a “round robin” fashion for each of the enabled PWM channels, it operates asynchronously to the internal PWM clock. Therefore it is not possible to instantaneously measure the channel current during PWM operation.

7.4.1. PWM Prescaler Register 0x30

Read: SPI Opcode: 0x30

Write: SPI Opcode: 0xB0

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 5	R/W	0	Not used.
4 − 0 (LSB)	R/W	0	5 bits provide 1 through 32 steps (2^5) clock divisions of the internal 50 MHz clock. If the optional external clock CLKIN is used, the same clock division will apply. 00000 is divide by 1, 00001 is divide by 2, ... 11111 is divide by 32 respectively.

7.4.2. PWM Period Register 0x31

Read: SPI Opcode: 0x31

Write: SPI Opcode: 0xB1

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	16 bits provide 1 through 65536 steps (2^{16}) in increments of (20 ns/LSB × Prescaler value (1 to 32)).

7.4.3. PWM Pulsewidth Register 0x32

Read: SPI Opcode: 0x32

Write: SPI Opcode: 0xB2

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	16 bits provide 1 through 65536 steps in increments of (20 ns/LSB × Prescaler value (1 to 32)). . **Note:** The pulsewidth programmed here must be less than the period programmed in the “PWM Period Register 0x31”.

7.4.4. PWM Parallel Mask Register 0x33

Read: SPI Opcode: 0x33

Write: SPI Opcode: 0xB3

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	Setting bits to logic “1” will cause the corresponding channels of registers 0x30, 0x31 and 0x32 to be programmed simultaneously by registers 0x34, 0x35, and 0x36 respectively.

7.4.5. PWM Parallel Prescaler Register 0x34

Read: SPI Opcode: 0x34

Write: SPI Opcode: 0xB4

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 5	R/W	0	Not used.
4 − 0 (LSB)	R/W	0	These bits provide the prescaler clock divider value simultaneously for all channels selected by the “PWM Parallel Mask Register 0x33”. It is programmed in the same way as the “PWM Prescaler Register 0x30”.

7.4.6. PWM Parallel Period Register 0x35

Read: SPI Opcode: 0x35

Write: SPI Opcode: 0xB5

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	These bits provide the PWM period value simultaneously for all channels selected by the “PWM Parallel Mask Register 0x33”. It is programmed in the same way as the “PWM Period Register 0x31”.

7.4.7. PWM Parallel Pulsewidth Register 0x36

Read: SPI Opcode: 0x36

Write: SPI Opcode: 0xB6

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	These bits provide the PWM pulsewidth value simultaneously for all channels selected by the “PWM Parallel Mask Register 0x33”. It is programmed in the same way as the “PWM Pulsewidth Register 0x32” **Note:** The pulsewidth programmed here must be less than the period programmed in the “PWM Parallel Period Register 0x35”.

7.5. Watchdog Timer Registers

An individual watchdog timer (WDT) is provided for each channel for applications that require the outputs to be shut off in a fail-safe event. If this feature is enabled for a channel in “Watchdog Timer Enable Register 0x40”, then the host software must provide a periodic write strobe pattern (see “Watchdog Timer Strobe Opcode 0xC5”) within the programmed Active WDT interval (see “Watchdog Timer Active Time Register 0x42”) to prevent the channel output driver from being shut off. Once a channel is shut off, it must be turned back on by the host (write “Channel Turn-On Register 0x01”). Only one strobe should be written during the active period.

The Active Time period is preceded by a Quiet Time period (see “Watchdog Timer Quiet Time Register 0x41”), within which no write strobe is allowed. Writing a strobe pattern within a Quiet Time interval will shut off the channel, which must be turned back on by the host writing “Channel Turn-On Register 0x01”. The timer for the beginning of the next Quiet Time interval is initiated by the strobe signal during the current Active Time interval (see Figure 9 below). This will simultaneously terminate the current Active Time period, ensuring the strobe is not delivered more than once within that period.

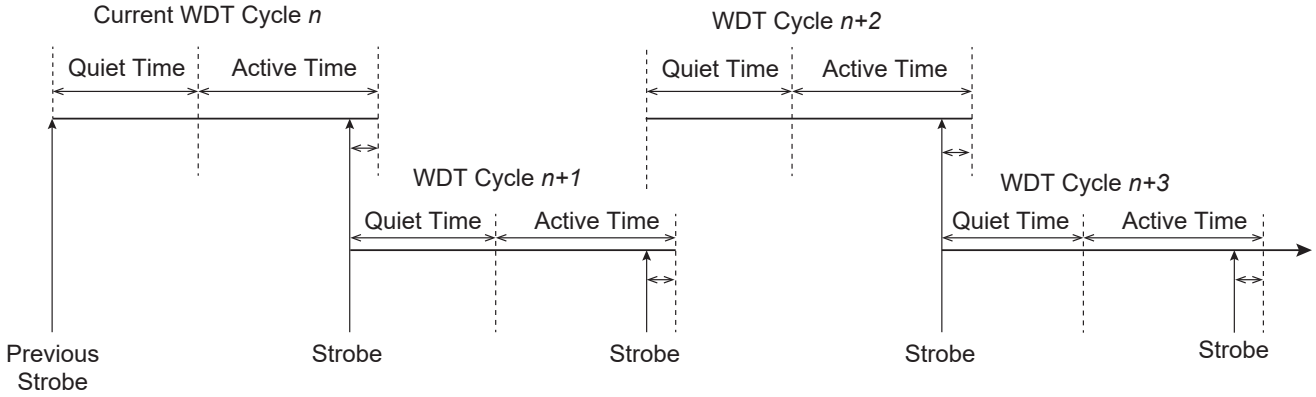


Figure 9. Watchdog Timer Process

7.5.1. Watchdog Timer Enable Register 0x40

Read: SPI Opcode: 0x40

Write: SPI Opcode: 0xC0

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables a watchdog timer on the corresponding channel 15 − 0 respectively.

7.5.2. Watchdog Timer Quiet Time Register 0x41

Read: SPI Opcode: 0x41

Write: SPI Opcode: 0xC1

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	These bits program the time interval between watchdog timer (WDT) active intervals. 16 bits provide 0 through 65535 steps (2^{16}) in increments of 5ms/LSB to give a range of 0ms – 327.68 sec. of WDT quiet time.

7.5.3. Watchdog Timer Active Time Register 0x42

Read: SPI Opcode: 0x42

Write: SPI Opcode: 0xC2

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0	These bits program the time interval over which the watchdog timer (WDT) is active. During this time interval, the device will expect a write strobe pattern for all channels with WDT enabled (see “Watchdog Timer Strobe Opcode 0xC5”). 16 bits provide 0 through 65535 steps (2^{16}) in increments of 5ms/LSB to give a range of 0ms – 327.68 sec. of possible WDT active time.

7.5.4. Watchdog Timer Active Count Register 0x43

Read: SPI Opcode: 0x43

Write: SPI Opcode: 0xC3

Parameter: 0x00

This register can be polled to determine the time remaining in the WDT active interval.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	16 bits count down from the value programmed in the “Watchdog Timer Active Time Register 0x42” to 0 over the WDT active interval. When zero, the WDT active interval has expired and the WDT is in its quiet period.

7.5.5. Watchdog Timer Quiet Count Register 0x44

Read: SPI Opcode: 0x44

Write: SPI Opcode: 0xC4

Parameter: 0x00

This register can be polled to determine the time remaining in the WDT quiet interval i.e. the time before the next WDT write strobe pattern is required.

Bit No.	R	Reset	Bit Description
15 (MSB) − 0 (LSB)	R	0	16 bits count down from the value programmed in the “Watchdog Timer Quiet Time Register 0x41” to 0 over the WDT quiet interval. When zero, the WDT quiet interval has expired and the WDT is in its active period.

7.5.6. Watchdog Timer Strobe Opcode 0xC5

Write: SPI Opcode: 0xC5

Parameter: 0x5A

During the WDT active interval defined in “Watchdog Timer Active Time Register 0x42”, the device will expect a write strobe pattern, opcode 0xC5 with parameter code 0x5A and two data words 0x80 and 0x01. If the write strobe is not received in the active WDT interval for a channel with enabled WDT, then the channel is shut off.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 8	R/W	0	WDT strobe data word 1 = 0x80
7 − 0 (LSB)	R/W	0	WDT strobe data word 2 = 0x01

7.6. OverCurrent Registers

7.6.1. Overcurrent Shutdown Delay Register 0x50

Read: SPI Opcode: 0x50

Write: SPI Opcode: 0xD0

Parameter: 0x00 – 0xF0. Access individual channels with bits[7:4]

This register provides the ability to program a delay (0 to 25.2 µs) before overcurrent shutdown occurs following detection of a current in excess of the overcurrent limit (350 − 600 mA). This may be used in applications to avoid shutdown where short term current spikes in excess of the overcurrent limit occur during normal operation (e.g. start-up inrush currents).

Note: The absolute maximum rating for the channel output current (800 mA) must not be exceeded.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 6	R/W	0	Not used.
5 − 0 (LSB)	R/W	0	6 bits provide 0 through 63 steps in increments of 400ns/LSB to give a range of 0 – 25.2 µs. The default delay before overcurrent shutdown occurs is zero. **Note:** An internal detection delay in the circuitry will result in a minimum delay of approximately 300 – 400 ns, even if this register is programmed to zero (see “DC Electrical Characteristics” for exact values).

7.6.2. Overcurrent Retry Enable Register 0x51

Read: SPI Opcode: 0x51

Write: SPI Opcode: 0xD1

Parameter: 0x00

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0	R/W	0	Setting a bit to logic “1” enables retries following a channel overcurrent shutdown on the corresponding channel 15 − 0 respectively. The number of retries is programmed in the “Overcurrent Retry Attempts Register 0x52”.

7.6.3. Overcurrent Retry Attempts Register 0x52

Read: SPI Opcode: 0x52

Write: SPI Opcode: 0xD2

Parameter: 0x00

This register programs the number of retries to restart a channel following overcurrent shutdown.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 8	R/W	0	Not used.
7 − 0 (LSB)	R/W	0x9C	8 bits provide 0 through 255 steps in increments of 64 retries/LSB to give a range of 0 – 16,320 retries. The default value of this register is 156(Dec) or 9,984 retries.

7.6.4. Overcurrent Retry Delay Register 0x53

Read: SPI Opcode: 0x53

Write: SPI Opcode: 0xD3

Parameter: 0x00

This register provides a programmable delay on retries following a channel overcurrent shutdown.

Bit No.	R/W	Reset	Bit Description
15 (MSB) − 0 (LSB)	R/W	0x05	16 bits provide 0 through 65535 steps in increments of 400ns/LSB to give a range of 0 – 26.2ms. The default delay on retries is 2µs.

8. Reset and Initialization

The device may be returned to its default state either by hardware reset ($\overline{\text{RESET}}$ pin) or software reset (opcode 0xE7 + parameter code 0x7E).

8.1. Hardware Reset

Hardware reset is initiated by a low to high transition on the $\overline{\text{RESET}}$ pin. The $\overline{\text{RESET}}$ pin should be asserted for a minimum of 200ns for system reliability however the device will enter a reset state asynchronously with the falling edge of $\overline{\text{RESET}}$.

The device will not exit the reset state until two clock edges after the rising edge of $\overline{\text{RESET}}$.

8.2. Software Reset

Write: SPI Opcode: 0xE7

Parameter: 0x7E

A software reset may be performed by writing SPI opcode 0xE7 with parameter code 0x7E. A software reset has the same effect as a hardware reset and brings the device back to its default state.

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

Supply voltages	VDDIO	-0.3 V to +7 V
	VDD	-0.3 V to +7 V
Logic input voltage range		-0.3 V to +7 V
Output Current per Channel		800 mA
Output Drain Voltage		40 V
ESD Capability	Human Body Model	± 4 kV
Solder Temperature (reflow)		260°C
Junction Temperature		175°C
Storage Temperature		-65°C to +150°C

Stresses above Absolute Maximum Ratings or outside Recommended Operating Conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

9.2. Recommended Operating Conditions

Parameters		Limits			Unit
		Min	Typ	Max	
Supply Voltages	VDDIO	1.65		5.25	V
	VDD	3.15		5.25	V
Output Current per Channel				250	mA
Output Drain Voltage				36	V
Temperature Range	Industrial	-40		85	°C
	Extended	-55		125	°C

9.3. DC Electrical Characteristics

V_{DD} = 3.3V or 5.0V, V_{DDIO} = 1.8V to 5.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters		Symbol	Test Conditions	Limits			Unit
				Min	Typ	Max	
Supply Voltage							
Supply Voltage		V_{DD}		3.15	3.30	5.25	V
Supply Current		I_{VDD}		18	21	60	mA
Digital I/O							
Digital I/O Supply Voltage		V_{DDIO}	1.8V Digital I/O	1.65	1.8	1.95	V
			2.5V Digital I/O	2.3	2.5	2.7	V
			3.3V Digital I/O	3.0	3.3	3.6	V
			5.0V Digital I/O	4.5	5.0	5.25	V
Digital I/O Supply Current		I_{VDDIO}	V_{DDIO} = 5.0V, No Load			200	µA
Min. Input Voltage (High)		V_{IH}	Digital Inputs	70%	-	-	V_{DDIO}
Max. Input Voltage (Low)		V_{IL}	Digital Inputs	-	-	30%	V_{DDIO}
Input Voltage Hysteresis		V_{HYS}	V_{DDIO} = 1.8V	350			mV
			V_{DDIO} = 5.0V	700			mV
Input Current (High): Inputs with pull-down.	$\overline{RESET}$, SI, SCLK, PWM_IN, EXTCLK_EN, CLKIN	I_{IH}	$V_{IH} = V_{DDIO}$	5	-	200	µA
Input Current (Low) Inputs with pull-up.	$\overline{CS}$, $\overline{OUT\_EN}$	I_{IL}	V_{IL} = 0V	-200	-	-5	µA
Max. Output Voltage (High)	SO	V_{OH}	I_{OUT} = 1.0mA, Digital outputs	90%	-	-	V_{DDIO}
Max. Output Voltage (Low)	SO, $\overline{INT}$ (Open drain)	V_{OL}	I_{OUT} = 1.0mA, Digital outputs	-	-	10%	V_{DDIO}
On Resistance							
Channel On Resistance		R_{DSon}	V_{DD} = 3.3V, Iout = 250mA T_A = 25°C	325	500	650	mΩ
			V_{DD} = 5.0V, Iout = 250mA T_A = 25°C	320	500	650	mΩ
			V_{DD} = 3.3V, Iout = 250mA T_A = 125°C	460	500	650	mΩ
			V_{DD} = 5.0V, Iout = 250mA T_A = 125°C	420	500	650	mΩ
Fault Protection							
Overcurrent shutdown limit		I_{SD}		350	475	600	mA
Overcurrent shutdown delay	I_{SD} = 600mA Overcurrent fault delay (Register 0x50) set to zero.	t_{SD}	V_{DD} = 3.15V – 5.25V	150	300	400	ns

Parameters	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Thermal fail-safe limit	T_{LIM}	Over-temperature duration = 10 clock cycles (200ns for 50MHz internal clock). Single point measurement at center of die.		215		°C
Channel Outputs (OUT0 – OUT15)						
Leakage Current	I_{OL}	Channel Turned-Off	-1.0	-	+1.0	µA
Channel Average Current Resolution (1 LSB)	I_{OAVE}		3.50	4.00	5.25	mA/ LSB
Channel Temperature Status Resolution (1 LSB)	T_{Ch}		4.8	6.0	7.2	°C/ LSB

9.4. AC Electrical Characteristics

V_{DD} = 3.3V or 5.0V, V_{DDIO} = 1.8V to 5.0V, GND = 0V, T_A = Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Limits			Units
		Min	Typ	Max	
INTERFACE TIMING (SPI Host Bus Interface). See Figure 10.					
SCK clock Period[1]	t_{CYC}	50	-	-	ns
$\overline{CE}$ set-up time to first SCK rising edge	t_{CES}	15	-	-	ns
$\overline{CE}$ hold time after last SCK rising edge	t_{CEH}	15	-	-	ns
$\overline{CE}$ inactive between SPI instructions	t_{CPH}	100	-	-	ns
SPI SI Data set-up time to SCK rising edge	t_{DS}	5	-	-	ns
SPI SI Data hold time after SCK rising edge	t_{DH}	5	-	-	ns
SO valid after SCK falling edge	t_{DV}	0	-	25	ns
SO high-impedance after $\overline{CE}$ inactive	t_{CHZ}	-	-	100	ns
Watchdog Timer (WDT)					
Active/Quiet Time Interval	t_{WDT}	0		327	s
Minimum Active/Quiet Time Interval	$t_{WDT(min.)}$	0	5	6	ms
External PWM Timing					
Maximum Frequency (each channel)				1.0	MHz
Propagation Delay			60		ns
Internal Oscillator					
Frequency	F_{OSC}	40	45	50	MHz
Optional External Clock (CLKIN pin)					
Frequency[3]	F_{CLKIN}	-	50	60	MHz
MASTER RESET $\overline{MR}$. See Figure 11.					
Minimum pulse width **Note:** Two rising clock edges are required following the rising edge of $\overline{MR}$ to complete reset (see Figure 11).	PW_{MR}	200			ns

Note 1: There is no minimum frequency specified for the SPI clock (no maximum SPI clock period, t_{CYC}). Operating at lower frequencies (longer clock periods) is permitted.

Note 2: This value is independent of the digital delay programmed in “Overcurrent Shutdown Delay Register 0x50” and must be added to the value programmed in Register 0x50 to account for the total shutdown delay (see also Figure 5).

Note 3: It is recommended to run the optional external clock (CLKIN) at 50 MHz to maintain the integrity of the timing values in the datasheet (e.g. WDT LSB = 5ms). Running at any other CLKIN frequency will scale the timing values by the same percentage as the frequency difference. If required in an application, it is possible to run at frequencies lower than the capability of the internal oscillator.

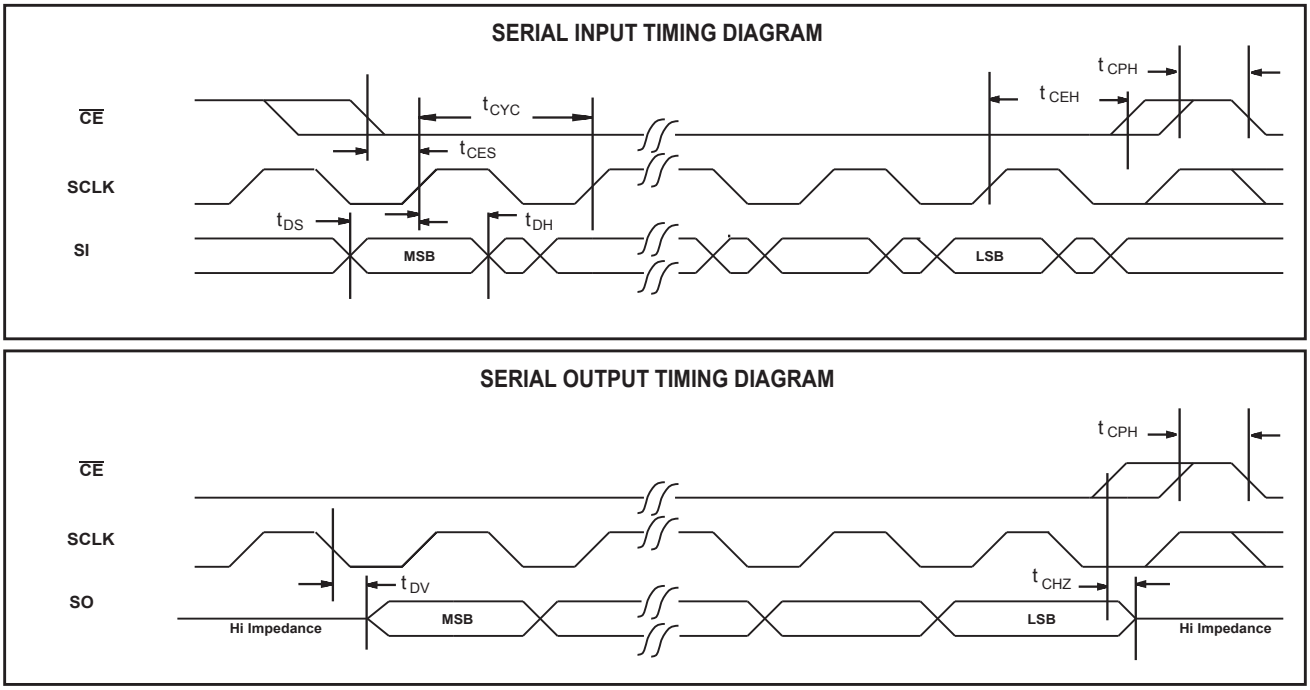


Figure 10. Host Bus Interface Timing Diagram

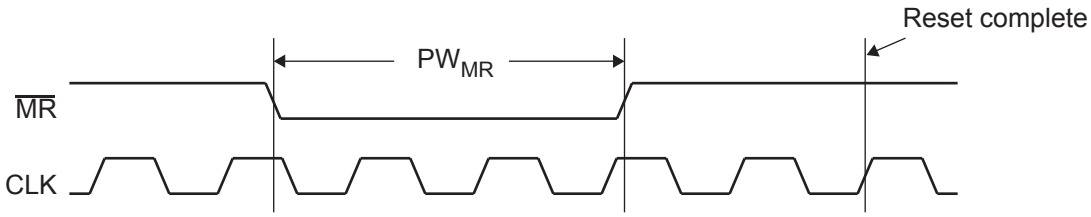


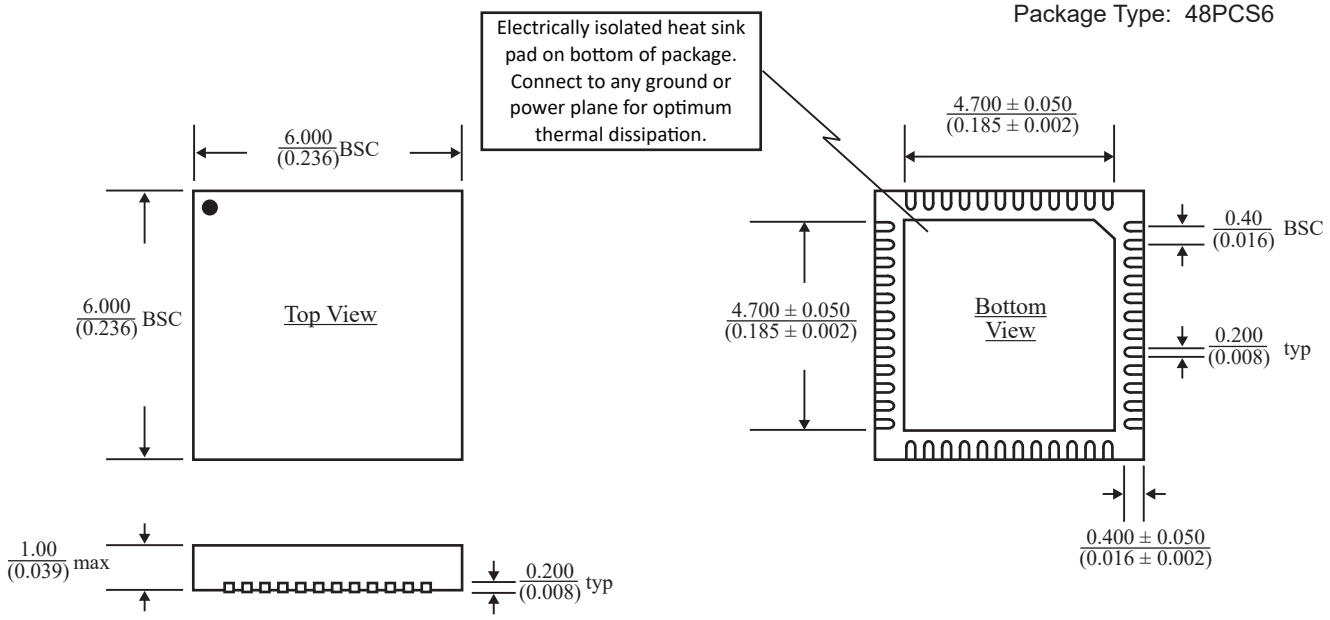
Figure 11. Master Reset Timing Diagram

10. Package Dimensions

48-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)

millimeters (inches)

Package Type: 48PCS6



BSC = "Basic Spacing between Centers" is theoretical true position dimension and has no tolerance. (JEDEC Standard 95)

11. Ordering Information

HI - 84216 PC x F

PART NUMBER	LEAD FINISH
F*	NiPdAu (Pb-free, RoHS compliant)

* Compatible with both leaded and lead-free assemblies.

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
PC	48 PIN PLASTIC CHIP-SCALE PACKAGE, 6 x 6mm QFN (48PCS6)

12. Revision History

Revision		Date	Description of Change
DS84216,	Rev. New	09/18/2024	Initial Release.
	Rev. A	09/26/2024	Change Absolute Maximum Rating for output current per channel from 600 mA to 800 mA.