# HI-1592
# Rad Hard MIL-STD-1553 Evaluation Board Quick Start Guide

## Devices Supported
## HI-1592

**August 2024**

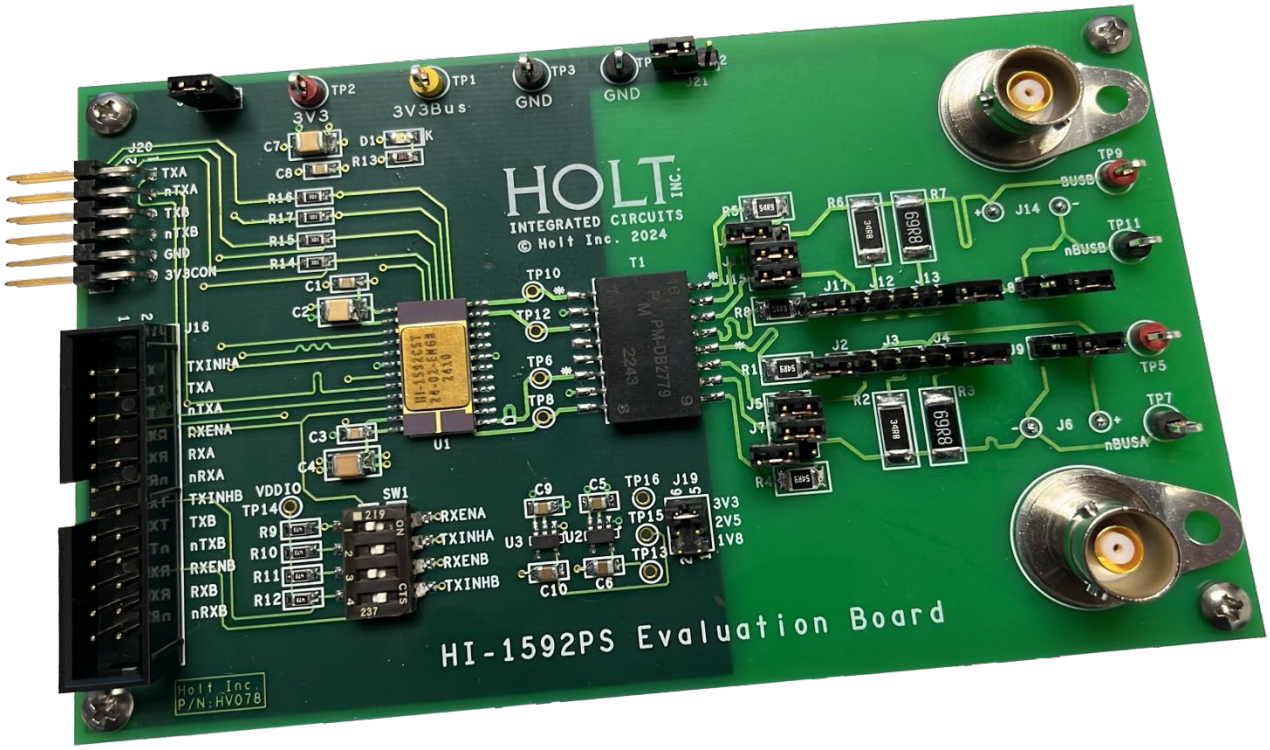
## REVISION HISTORY

| Revision | Date | Description of Change |
|---|---|---|
| Rev. New | 8/19/2024 | Initial Release |
| | | |

## Introduction

This evaluation board demonstrates the operation of the HI-1592. The HI- 1592 is a radiation hardened MIL-1553 transceiver. The kit is composed of a HI-1592 and associated circuitry to support FPGAs or driverless MIL-1553 protocol controllers.

This guide describes how to set up and run the board.



## Evaluation Kit Contents

- This Quick Start Guide.
- One HI-1592 evaluation board.

## Default Jumper Settings

The HI-1592 evaluation board image above shows the default positions and settings of the jumpers and switches. Those settings are also described in the table below. The table sorts the switches and jumpers from top left to bottom right.

| Header | Default | Description |
|---|---|---|
| J1 | Shorted | Connect PMOD power to PCB power rails |
| J21 | Open | Connect BUS ground to PCB ground |
| J10 | Open | BUSB "direct" connection |
| J11 | Shorted | BUSB "transformer" connection |
| J15 | Shorted | /BUSB "transformer" connection |
| J17 | Open | /BUSB "direct" connection |
| J12 | Open | 35 ohm BUSB shunt resistor |
| J13 | Open | 70 ohm BUSB shunt resistor |
| J18 | Open | /BUSB to GND jumper |
| J2 | Open | BUSA "direct" connection |
| J3 | Open | 35 ohm BUSA shunt resistor |
| J4 | Open | 70 ohm BUSA shunt resistor |
| J9 | Open | /BUSA to GND jumper |
| J5 | Shorted | BUSA "transformer" connection |
| J7 | Shorted | /BUSA to GND jumper |
| J8 | Open | /BUSA "direct" connection |
| | | |
| J19 | 3V3 | VDDIO Selection |
| | | |
| | | SWITCH SETTINGS FOR PMOD J20 Usage |
| SW1-1 | Off | RXENA - enabled |
| SW1-2 | On | TXINHA - enabled, not inhibited |
| SW1-3 | Off | RXENB - enabled |
| SW1-4 | On | THINHB - enabled, not inhibited |
| | | |

| | | SWITCH SETTINGS FOR J16 Usage |
|---|---|---|
| SW1-1 | Off | RXENA - controlled by J16 |
| SW1-2 | Off | TXINHA - controlled by J16 |
| SW1-3 | Off | RXENB - controlled by J16 |
| SW1-4 | Off | THINHB - controlled by J16 |

## Hardware Design Overview

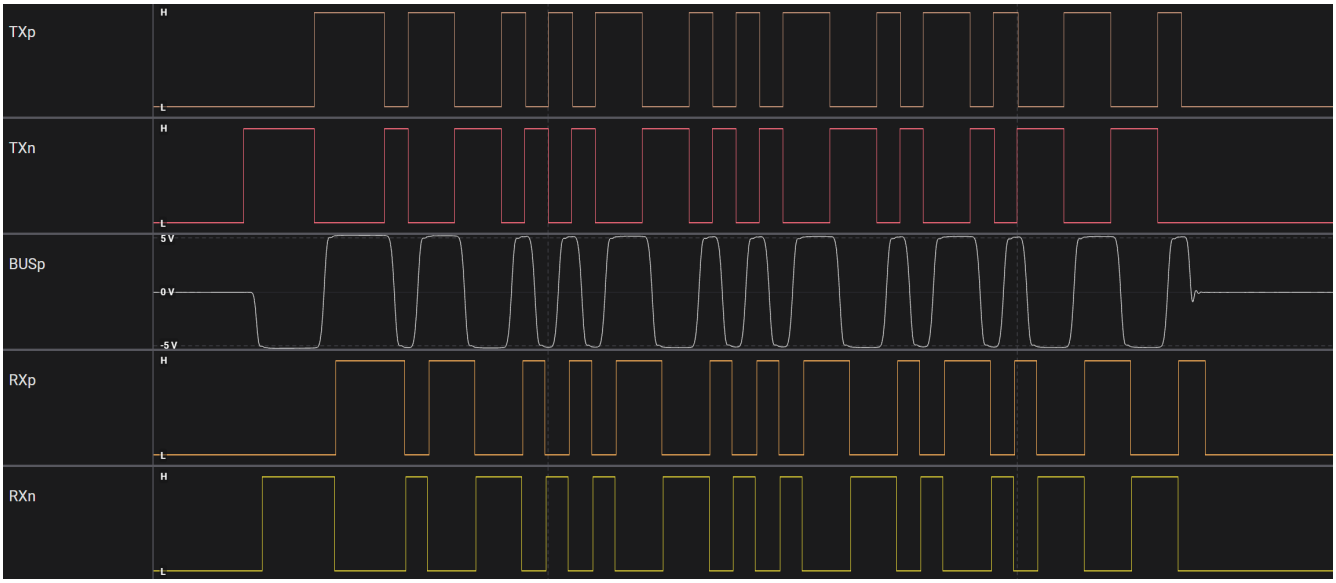
Refer to the end of this guide for schematic diagram and bill of materials for the evaluation board (EVB) design. The EVB connects to a MIL-1553 protocol controller or FPGA using the J20 PMOD port. This port has the logic level transmit and receive signals needed to send and receive MIL-STD-1553 bus data. J16 is an additional connection port. SW1 has the default transmit and receive enable lines that will need to be set to use the PMOD port. When using J16, these switches will need to be placed in the "off" state when using the RXEN and TXINH control lines of J16.

## Initial Kit Setup

- Connect a MIL-1553 protocol controller (FPGA or ASIC) to either J20 or J16.
- Power up both the protocol controller board and the EVB board simultaneously.
- Apply test signals to demonstrate operation.

## Demonstration Images

The image below shows a data signal being generated using a protocol controller connected to the PMOD port. BUSA was looped-back to BUSB using a MIL-1553 bus coupler for this demonstration. TXp and TXn are connected to the BUSA digital transmit input signals. RXp and RXn are connected to the digital receive outputs of BUSB. The BUSp signal shows the signal present on BUS B.




## Board Files and Schematic Links

BOM and Schematic Files: EV-1592