HT32F49041
Datasheet

32-Bit Arm® Cortex®-M4 Microcontroller,
up to 64 KB Flash and 20 KB SRAM with 2 MSPS ADC,
USART, SPI, I²S, I²C, GPTMR, ACTMR, BTMR, CRC,
ERTC, WDT, WWDT, DMA, CAN, IRTMR and OTGFS

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1 General Description

The HT32F49041 device is based on the high-performance Arm® Cortex®-M4 32-bit RISC core running up to 96 MHz. The Cortex®-M4 core features a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The device incorporates high-speed embedded memories (up to 64 Kbytes of internal Flash memory and 20 Kbytes of SRAM), enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib”, functioning as a security area with code-executable only.

The device offers one 12-bit ADC, six general-purpose 16-bit timers, one 32-bit general-purpose timer, two basic timers, one advanced timer and one low-power ERTC. It supports standard and advanced communication interfaces: up to two I²Cs, three SPIs (all multiplexed as I²Ss), four USARTs, one CAN, one OTGFS interface and one infrared transmitter.

The device operates in the -40 to +105 °C temperature range, with a power supply from 2.4 to 3.6 V. A comprehensive set of power-saving modes meet the requirements of low-power applications.

The device is supplied in various package types. Depending on the different packages, the pin-to-pin is completely compatible among devices, and also the software and functionality. Only different sets of peripherals are included.

2 Features

Arm® Cortex®-M4

The Arm® Cortex®-M4 processor is the latest generation of Arm® processor for embedded systems. It is a 32-bit high-performance RISC processor that features exceptional code efficiency, outstanding computational performance and advanced response to interrupts. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution.

Memory

Internal Flash Memory

Up to 64 Kbytes of embedded Flash is available for storing programs and data. User can configure any part of the embedded Flash memory protected by the sLib, functioning as a security area with code-executable only but non-readable. “sLib” is a mechanism that protects the intelligence of solution vendors and facilitates the second-level development by customers.

There is another 4-Kbyte boot memory in which the bootloader is stored. If it is not needed, this boot memory can be used as a general instruction / data memory (one-time-configured) instead.

A User System Data block is included, which is used as configuration of the hardware behaviors such as access / erase / write protection and watchdog self-enable. User System Data allows to set erase / write and access protection. The access protection is divided into low-level and high-level protections.

Memory Protection Unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

Embedded SRAM

Up to 20 Kbytes of embedded SRAM (read / write) is accessible at CPU clock speed with 0 wait state.

Interrupts

Nested Vectored Interrupt Controller (NVIC)

The device has embedded a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4. This hardware block provides flexible interrupt management features with minimal interrupt latency.

External Interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 21 edge-detector lines used to generate interrupt requests. Each line can be independently configured to

select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

Power Control (PWC)

Power Supply Schemes

- V_{DD} = 2.4 ~ 3.6 V: external power supply for GPIOs and the internal blocks such as ERTC, external 32 kHz oscillator (LEXT), battery powered register (BPR) and the internal regulator (LDO), etc..
- V_{DDA} = 2.4 ~ 3.6 V: external analog power supply for ADC through V_{DDA} pin. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.

Reset and Power Voltage Monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR) and low voltage reset (LVR) circuitry. It is always active and allows proper operation starting from 2.4 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

The device has embeded a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

Voltage Regulator (LDO)

The LDO has three operating modes: normal, low-power, and power-down.

- Normal mode: used in Run / Sleep mode and in Deepsleep mode;
- Low-power mode: used in Deepsleep mode;
- Power-down mode: used in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

This LDO always operates in its normal mode after reset.

Low-power Modes

The device supports three low-power modes:

- Sleep Mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- Deepsleep Mode

  Deepsleep mode achieves the lowest power consumption while holding the contents of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The voltage regulator can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm, wakeup, tamper, time stamp event, or the OTG wakeup signal.

- Standby Mode

  The Standby mode is used to acquire the lowest power consumption. The internal LDO is switched off so that the entire LDO power domain is powered off. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for ERTC and BPR registers and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm, wakeup, tamper, time stamp occurs.

Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. The WDT depends on the User System Data setting.

Boot Modes

At startup, BOOT0 pin and nBOOT1 bit in the User System Data are used to select one of three boot options:

- Boot from Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in the boot memory. It is used to reprogram the Flash memory through USART1 or USART2. The following table provides the pin configurations for bootloader.

Table 1. Pin Configurations for Bootloader

Interface	Pins
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX PA3: USART2_RX

Clocks

The internal 48 MHz clock (HICK) through a divided-by-6 divider (8 MHz) is selected as the default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are used for the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB and APB domains is 96 MHz.

The device has embeded an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK. This assures the most precise accuracy of the HICK in the full range of the operating temperatures.

General-purpose Inputs / Outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as multiple function. Most of the GPIO pins are shared with digital or analog multiple functions. All GPIOs are high current-capable.

The GPIO's configuration can be locked, if needed, in order to avoid false writing to the GPIO's registers by following a specific sequence.

Direct Memory Access Controller (DMA)

The device features a general-purpose 7-channel DMA controller that is able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. These DMA channels can be connected to peripherals for flexible mapping purposes.

The DMA controller supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software, and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI and I^2S, I^2C, USART, advanced, general-purpose and basic timers TMRx (except TMR13/14), and ADC.

Timers (TMR)

The device includes an advanced timer, up to seven general-purpose timers, two basic timers and a SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 2. Timer Feature Comparison

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request Generation	Capture/ Compare Channels	Complementary Output
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR2	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR13 TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TMR15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TMR16 TMR17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6 TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

Advanced Timer (TMR1)

The advanced timer (TMR1) can be seen a three-phase PWM multiplexed on 6 channels. It has complementary PWM outputs with programmable dead-time insertion. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)

- One-cycle mode output

If configured as a standard 16-bit timer, it has the same features as that of the TMRx timer. If configured as a 16-bit PWM generator, it boasts full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen, and the PWM outputs are disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TMRs that have the same architecture. Thus, the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

General-Purpose Timers (TMR2 ~ 3 and TMR13 ~ 17)

Up to seven synchronizable general-purpose timers are available in the device.

TMR2 and TMR3

The TMR2 timer is based on a 32-bit auto-reload up counter / down counter and a 16-bit prescaler. The TMR3 timer is based on a 16-bit auto-reload up counter / down counter and a 16-bit prescaler. They can offer four independent channels on the largest packages. Each channel can be used for input capture / output compare, PWM or one-cycle mode outputs.

These general-purpose timers can work with the advanced timers via the link feature for synchronization or event chaining. In debug mode, their counters can be frozen. Any of these general-purpose timers can be used for the generation of PWM output. Each timer has its individual DMA request mechanism.

They are capable of handling incremental quadrature encoder signals and the digital outputs coming from 1 to 3 hall-effect sensors.

TMR13 and TMR14

These timers are based on a 16-bit auto-reload up counter, a 16-bit prescaler, and one independent channel for input capture / output compare, PWM, or one-cycle mode output. They can be synchronized with the full-featured general-purpose timers. They can also be used as simple time bases. In debug mode, these timers can be frozen.

TMR15, TMR16 and TMR17

These three timers are based on a 16-bit auto-reload up counter and a 16-bit prescaler. The TMR15 offers two channels and one complementary channel, whereas TMR16 and TMR17 have one channel and one complementary channel for input capture/output compare, PWM, or one-cycle mode output.

They can work together via the link feature for synchronization or event chaining.

In debug mode, their counters can be frozen. Each timer has its individual DMA request mechanism.

Basic Timers (TMR6 and TMR7)

These two timers are used as a generic 16-bit time base.

SysTick Timer

This timer is dedicated to real-time operating systems, but it could also be used as a standard down counter. Its features include:

- A 24-bit down counter
- Auto-reload capability

- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

Watchdog (WDT)

The watchdog consists of a 12-bit down counter and an 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabling or not configurable through the User System Data. The counter can be frozen in debug mode.

Window Watchdog (WWDT)

The window watchdog embeds a 7-bit down counter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock. It has an early warning interrupt capability, and the counter can be frozen in debug mode.

Enhanced Real-Time Clock (ERTC) and Battery Powered Registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- Five 32-bit battery powered registers (BPRs)

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), weekday, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value is also available in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic interrupts wakeup from Deepsleep or Standby mode.
- To compensate quartz crystal inaccuracy, ERTC can be calibrated via a 512 Hz external output.

The alarm registers are used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload down counter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 μs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, weekday and date.

A prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 20 bytes of user application data. Battery powered registers are not reset by a system or power reset, or when the device is woken up from the Standby mode.

Communication Interfaces

Serial Peripheral Interface (SPI)

There are up to three SPIs able to communicate at up to 36 Mbits/s in slave and master modes in full-duplex and half-duplex modes. The prescaler generates several master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD card / MMC / SDHC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master and slave modes.

Inter-Integrated Sound Interface (I^2S)

Three standard I^2S interfaces (multiplexed with SPI) are available, which can be operated in master or slave mode in half-duplex mode. These interfaces can be configured to operate with 16/24/32 bit resolution, as input or output channels. Audio sampling frequencies ranges from 8 kHz up to 192 kHz. When the I^2S is configured in master mode, the master clock can be output to the external 256 times sampling frequency.

In addition, any two of these I^2S interfaces in half-duplex mode can be combined to achieve full-duplex communication function, while the remaining interface can still be operated independently or used as a SPI.

All I^2Ss can use the DMA controller.

Universal Synchronous / Asynchronous Receiver Transmitters (USART)

The device has embeded four universal synchronous/asynchronous receiver transmitters (USART1~4).

These four interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. They also offer hardware management of the CTS and RTS signals, RS485 drive enable signal, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller, with TX/RX swap support.

All interfaces are able to communicate at a speed of up to 6 Mbit/s.

Inter-Integrated-Circuit Interface (I^2C)

Two I^2C bus interfaces can operate in multi-master and slave modes. They can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz). Several GPIOs provide ultra-high sink current 20 mA.

They support 7-bit/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation / verification is included.

They can be served by DMA and they support SMBus 2.0/PMBus.

Controller Area Network (CAN)

The controller area network (CAN) is compliant with specifications 2.0A and 2.0B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages, and 14 scalable filter banks. It also has dedicated 256 bytes of SRAM, which is not shared with any other peripherals.

To guarantee transmission, according to the clock accuracy requirements in CAN 2.0 specification, the CAN clock source should be the PLL clock sourced by HEXT.

Universal Serial bus On-The-Go Full-Speed (OTGFS)

The device has embeded one OTG full-speed (12 Mb/s) modules that consists of PHY and can be set as a device/host. It has software-configurable endpoint setting and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock; as the host, the HICK 48 MHz clock source is generated by PLL; as a device peripheral, the HICK 48 MHz clock source can be used as the OTGFS clock directly.

OTGFS has the major features such as:

- Dedicated 1280 bytes of buffer (not shared with any other peripherals)
- 8 IN + 8 OUT endpoints (endpoint 0 included, device mode)
- 16 channels (host mode)
- SOF and OE outputs
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - Host mode: full-speed and low-speed
  - Device mode: full-speed

Infrared Transmitter (IRTMR)

The device provides an infrared transmitter solution. The solution is based on the internal connection between TMR16, USART1, or USART4 and TMR17. TMR17 is used to provide the carrier frequency, and TMR16, USART1, or USART4 provides the main signal to be sent. The infrared output signal is available on PB9 or PA13.

To generate infrared remote control signals, TMR16 channel 1 and TMR17 channel 1 must be correctly configured to generate a correct waveform. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

Cyclic Redundancy Check (CRC) Calculation Unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

Analog-to-Digital Converter (ADC)

There is one 12-bit 2 MSPS analog-to-digital converter (ADC) embedded in the device. This ADC shares up to 16 external channels and two internal channels, with the internal channels connected to V_{SSA} and the internal reference voltage (V_{INTRV}), respectively. The ADC controller, with 2 to 256 times hardware over-sampling, up to equivalent 16-bit resolution, can implement single or sequence conversion. In sequential mode, automatic conversion is performed on a selected group of analog channels.

The internal reference voltage (V_{INTRV}) provides a stable voltage output for the ADC. The V_{INTRV} is internally connected to the ADC1_IN17 channel.

This ADC can be served by the DMA controller.

A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is above the programmed

thresholds.

The events generated by the general-purpose timers (TMRx) and advanced timers (TMR1) can be cascaded to the ordinary conversion and preempted conversion of ADC, respectively. The ADC conversion can be synchronized with clocks through the application program.

Serial Wire Debug (SWD) and Serial Wire Output (SWO) Interfaces

The Arm® SWD interface is embedded in the device. It is a serial wire debug interface that enables a serial wire debugger to be connected to the target for programming and debugging. It also offers a SWO feature for asynchronous trace in debug mode.

3 Overview

Device Information

Table 3. Features and Peripheral List

Part Number		HT32F49041			
Frequency (MHz)		96			
Int. Flash (KB)		64			
SRAM (KB)		20			
Timers	Advanced	1	1	1	1
	32-bit general-purpose	1	1	1	1
	16-bit general-purpose	6	6	6	6
	Basic	2	2	2	2
	SysTick	1	1	1	1
	WDT	1	1	1	1
	WWDT	1	1	1	1
	ERTC	1	1	1	1
Communication interfaces	I²C	2	2	2	2
	SPI(1)	2(2)	3	3	3
	I²S (half-duplex) (1)(3)	2(2)	3	3	3
	USART	4(4)	4	4	4
	CAN	1	1	1	1
	OTGFS	1	1	1	1
	IRTMR	1	1	1	1
Analog	Number of 12-bit ADC	1	1	1	1
	Number of external channels	9	10	10	16
GPIO		15	27	39	55
Operating temperatures		-40 °C to +105 °C			
Packages		20-pin TSSOP 6.5 × 4.4 mm	32-pin QFN 4 × 4 mm	48-pin LQFP 7 × 7 mm	64-pin LQFP 7 × 7 mm

Note: 1. Half-duplex I²S shares the same pin with SPI.
2. For the 20-pin TSSOP package, only SPI1/I²S1 and SPI2/I²S2 are available.
3. Two combined half-duplex I²S can achieve one full-duplex I²S function.
4. For the 20-pin TSSOP package, USART3 cannot provide all functional pins at the same time; USART1 and USART4 are used as UART since they can only offer TX and RX pins.

Block Diagram

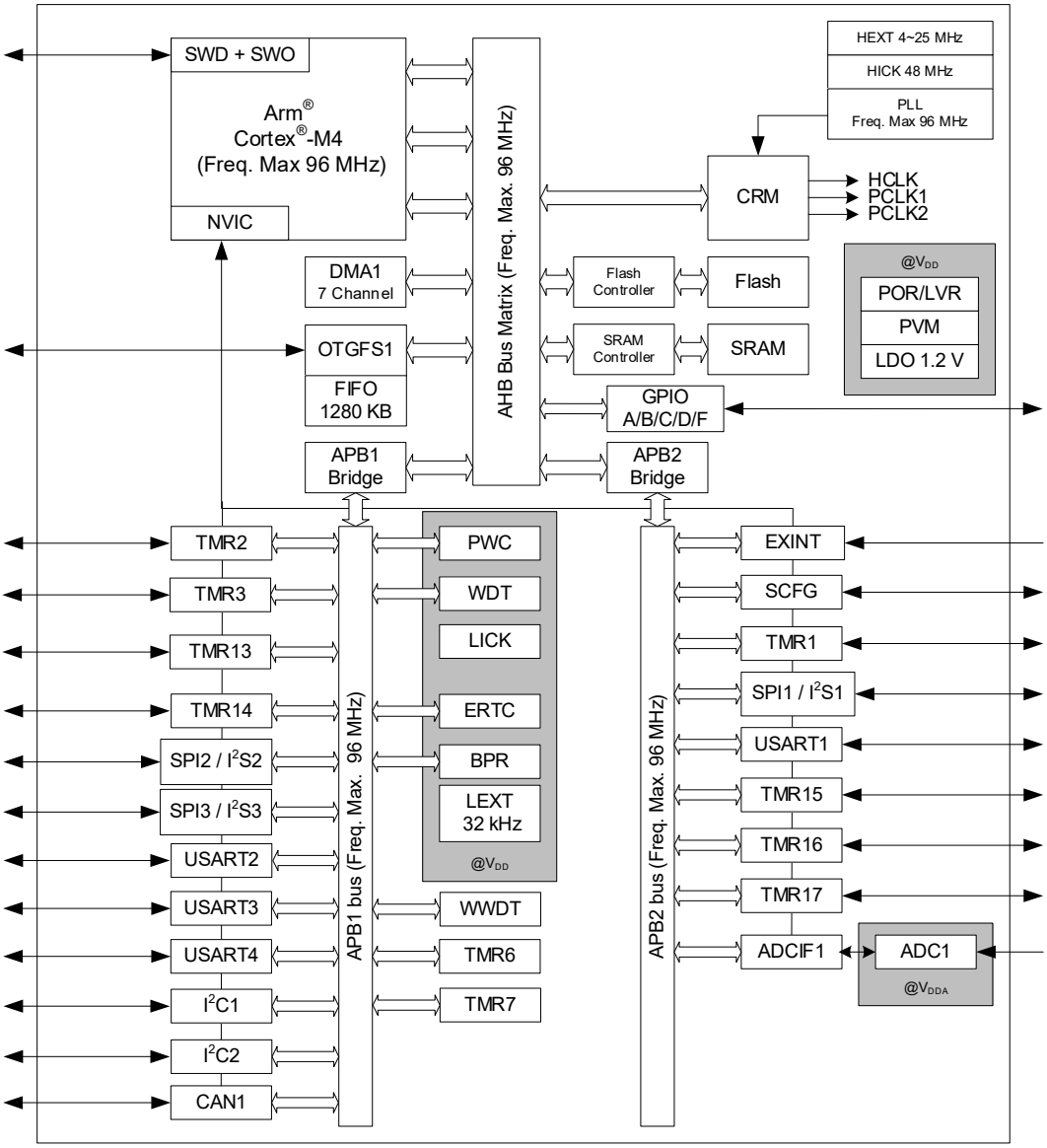


Figure 1. Block Diagram

Memory Map

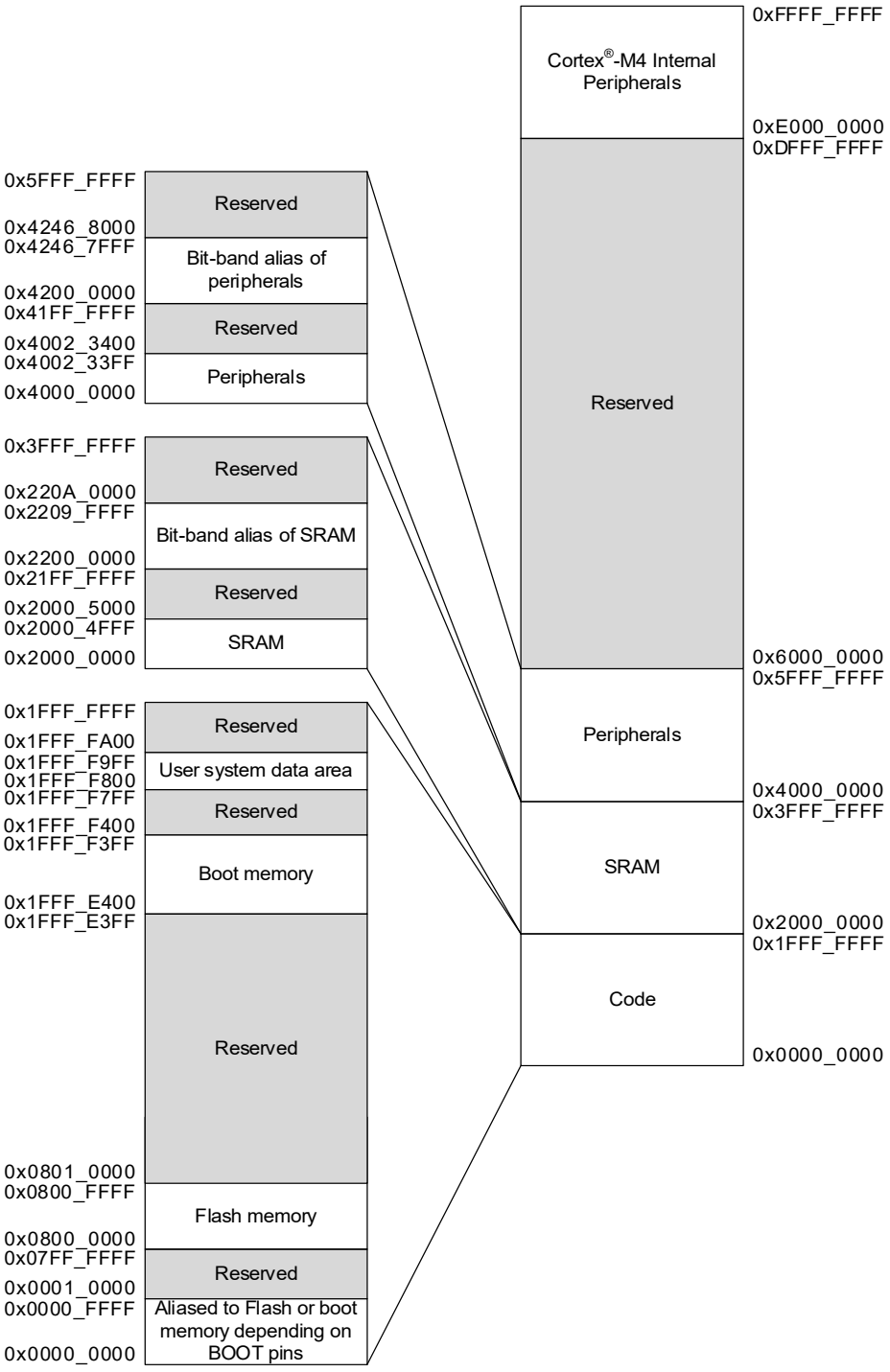


Figure 2. Memory Map

Clock Structure

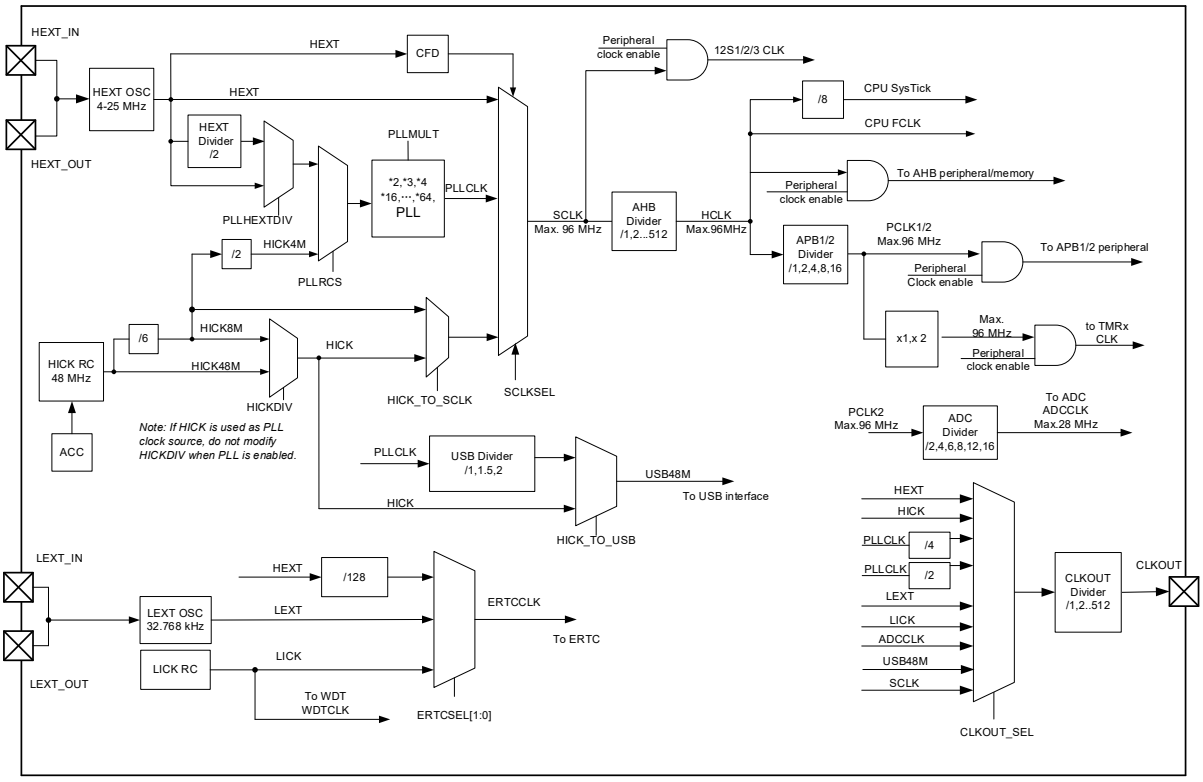


Figure 3. Clock Structure

4 Pin Assignment

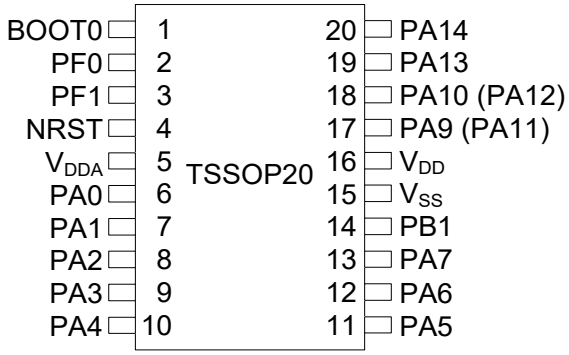


Figure 4. 20-pin TSSOP Pin Assignment

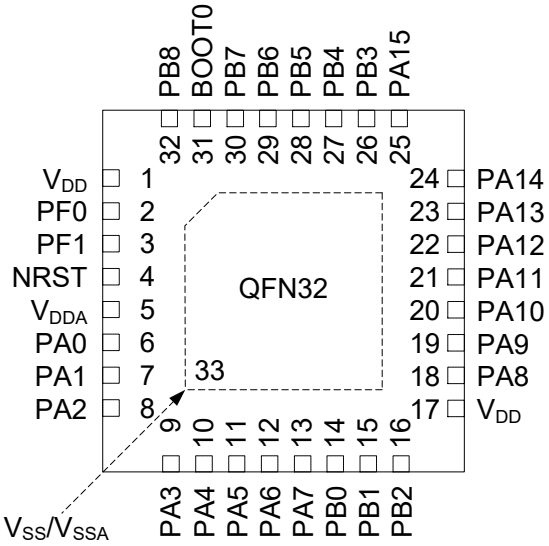


Figure 5. 32-pin QFN Pin Assignment

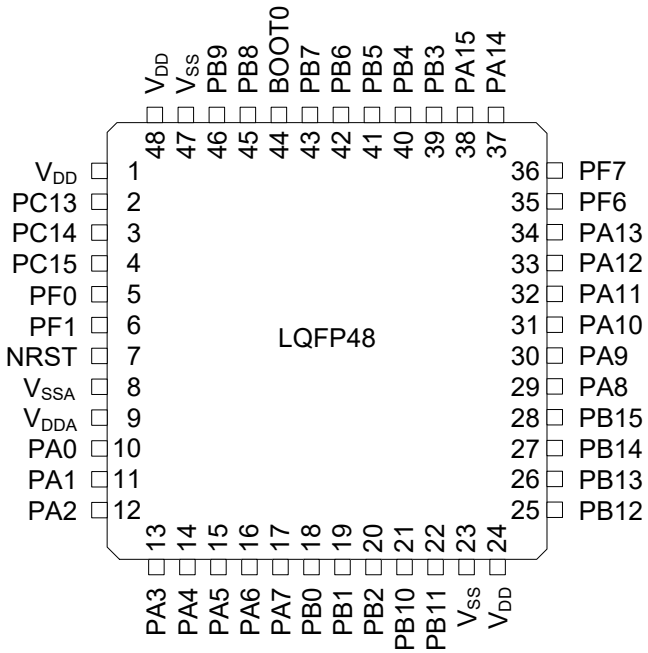


Figure 6. 48-pin LQFP Pin Assignment

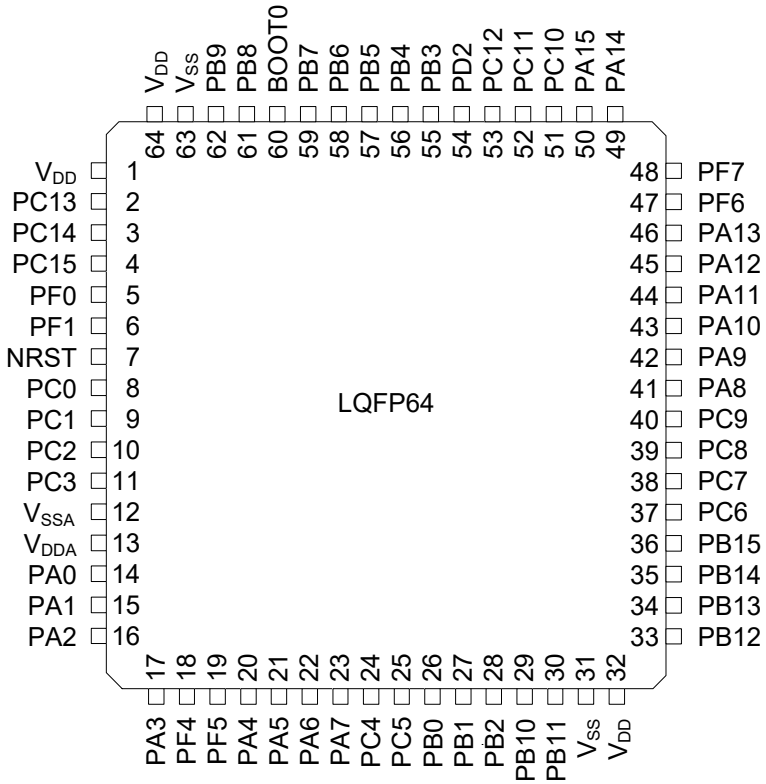


Figure 7. 64-pin LQFP Pin Assignment

The table below is the pin definition of the HT32F49041. "—" represents that there is no such pinout on the related package. Unless descriptions in ( ) under pin name, the function during reset and after reset is the same as the actual pin name. Unless otherwise specified, all GPIOs are set as input floating during reset and after reset. Pin multi-functions are selected via GPIOx_MUXx registers and the additional functions are directly selected and enabled through peripheral registers.

Table 4. Series Pin Definitions

Pin Number				Pin Name (Function after Reset)	Type(1)	GPIO Level(2)	IOMUX Functions	Additional Functions
20TSSOP	32QFN	48LQFP	64LQFP					
	1	1	1	V_{DD}	S	—	Digital power supply	
		2	2	PC13	I/O	FT	—	ERTC_OUT / TAMP1 / WKUP2
		3	3	PC14	I/O	TC	—	LEXT_IN
		4	4	PC15	I/O	TC	—	LEXT_OUT
2	2	5	5	PF0	I/O	TC	TMR1_CH1	HEXT_IN
3	3	6	6	PF1	I/O	TC	TMR1_CH2C / SPI2_CS / I2S2_WS	HEXT_OUT
4	4	7	7	NRST	I/O	R	Device reset input / internal reset output (active low)	
			8	PC0	I/O	FTa	EVENTOUT / I2C2_SCL / I2C1_SCL	ADC1_IN10
			9	PC1	I/O	FTa	EVENTOUT / I2C2_SDA / SPI3_MOSI / I2S3_SD / SPI1_MOSI / I2S1_SD / SPI2_MOSI / I2S2_SD / I2C1_SDA	ADC1_IN11
			10	PC2	I/O	FTa	EVENTOUT / SPI2_MISO / I2S2_MCK / I2S_SDEXT	ADC1_IN12
			11	PC3	I/O	FTa	EVENTOUT / SPI2_MOSI / I2S2_SD	ADC1_IN13
		8	12	V_{SSA}	S	—	Analog ground	
5	5	9	13	V_{DDA}	S	—	Analog power supply	
6	6	10	14	PA0	I/O	FTa	USART2_RX / USART2_CTS / TMR2_CH1 / TMR2_EXT / I2C2_SCL / USART4_TX / TMR1_EXT	ADC1_IN0 / WKUP1
7	7	11	15	PA1	I/O	FTa	EVENTOUT / USART2_RTS_DE / TMR2_CH2 / I2C2_SDA / USART4_RX / TMR15_CH1C / I2C1_SMBA / SPI3_MOSI / I2S3_SD	ADC1_IN1
8	8	12	16	PA2	I/O	FTa	TMR15_CH1 / USART2_TX / TMR2_CH3 / CAN1_RX	ADC1_IN2 / WKUP4
9	9	13	17	PA3	I/O	FTa	TMR15_CH2 / USART2_RX / TMR2_CH4 / CAN1_TX / I2S2_MCK	ADC1_IN3
			18	PF4	I/O	FT	I2C1_SDA / TMR2_CH1	—
			19	PF5	I/O	FT	I2C1_SCL / TMR2_CH2	—
10	10	14	20	PA4	I/O	FTa	SPI1_CS / I2S1_WS / USART2_CK / OTGFS1_OE / SPI3_CS / I2S3_WS / TMR14_CH1 / I2C1_SCL / SPI2_CS / I2S2_WS	ADC1_IN4
11	11	15	21	PA5	I/O	FTa	SPI1_SCK / I2S1_CK / TMR2_CH1 / TMR2_EXT / USART3_CK / USART3_RX	ADC1_IN5
12	12	16	22	PA6	I/O	FTa	SPI1_MISO / I2S1_MCK / TMR3_CH1 / TMR1_BRK / USART3_RX / USART3_CTS / TMR16_CH1 / I2S2_MCK / TMR13_CH1	ADC1_IN6
13	13	17	23	PA7	I/O	FTa	SPI1_MOSI / I2S1_SD / TMR3_CH2 / TMR1_CH1C / USART3_TX / TMR14_CH1 / TMR17_CH1 / EVENTOUT / I2C2_SCL	ADC1_IN7
			24	PC4	I/O	FTa	EVENTOUT / USART3_TX / TMR13_CH1 / I2S1_MCK	ADC1_IN14
			25	PC5	I/O	FTa	USART3_RX	ADC1_IN15 / WKUP5
	14	18	26	PB0	I/O	FTa	EVENTOUT / TMR3_CH3 / TMR1_CH2C / USART2_RX / USART3_CK / SPI1_MISO / I2S1_MCK	ADC1_IN8
14	15	19	27	PB1	I/O	FTa	TMR14_CH1 / TMR3_CH4 / TMR1_CH3C / USART2_CK / USART3_RTS_DE / SPI2_SCK / I2S2_CK / SPI1_MOSI / I2S1_SD	ADC1_IN9
	16	20	28	PB2	I/O	FTa	TMR3_EXT / SPI3_MOSI / I2S3_SD / I2C1_SMBA	—
		21	29	PB10	I/O	FT	I2C2_SCL / TMR2_CH3 / USART3_TX / SPI2_SCK / I2S2_CK	—
		22	30	PB11	I/O	FT	EVENTOUT / I2C2_SDA / TMR2_CH4 / USART3_RX	—
15		23	31	V_{SS}	S	—	Digital ground	
16	17	24	32	V_{DD}	S	—	Digital power supply	
		25	33	PB12	I/O	FT	SPI2_CS / I2S2_WS / EVENTOUT / TMR1_BRK / USART3_CK / TMR15_BRK / SPI3_CS / I2S3_WS / I2C2_SMBA	—
		26	34	PB13	I/O	FTf	SPI2_SCK / I2S2_CK / TMR15_CH1C / TMR1_CH1C / CLKOUT / USART3_CTS / I2C2_SCL / SPI3_SCK / I2S3_CK	—

Pin Number				Pin Name (Function after Reset)	Type[1]	GPIO Level[2]	IOMUX Functions	Additional Functions
20TSSOP	32QFN	48LQFP	64LQFP					
		27	35	PB14	I/O	FTf	SPI2_MISO / I2S2_MCK / TMR15_CH1 / TMR1_CH2C / I2S_SDEXT / USART3_RTS_DE / I2C2_SDA / SPI3_MISO / I2S3_MCK	—
		28	36	PB15	I/O	FT	SPI2_MOSI / I2S2_SD / TMR15_CH2 / TMR1_CH3C / TMR15_CH1C / ERTC_REFIN / SPI3_MOSI / I2S3_SD	WKUP7
			37	PC6	I/O	FT	TMR3_CH1 / I2C1_SCL / TMR1_CH1 / I2S2_MCK	—
			38	PC7	I/O	FT	TMR3_CH2 / I2C1_SDA / TMR1_CH2 / I2S2_MCK / SPI2_SCK / I2S2_CK	—
			39	PC8	I/O	FT	TMR3_CH3 / TMR1_CH3	—
			40	PC9	I/O	FT	TMR3_CH4 / I2C2_SDA / TMR1_CH4 / OTGFS1_OE / I2C1_SDA	—
	18	29	41	PA8	I/O	FT	CLKOUT / USART1_CK / TMR1_CH1 / OTGFS1_SOF / USART2_TX / EVENTOUT / I2C2_SCL	—
	19	30	42	PA9	I/O	FT	TMR15_BRK / USART1_TX / TMR1_CH2 / OTGFS1_VBUS / I2C1_SCL / CLKOUT / SPI3_SCK / I2S3_CK / I2C2_SMBA	—
	20	31	43	PA10	I/O	FT	TMR17_BRK / USART1_RX / TMR1_CH3 / OTGFS1_ID / I2C1_SDA / ERTC_REFIN / SPI3_MOSI / I2S3_SD	—
17[3]				PA9	I/O	TC[4]	TMR15_BRK / USART1_TX / TMR1_CH2 / I2C1_SCL / CLKOUT / I2C2_SMBA	—
18[3]				PA10	I/O	TC[4]	TMR17_BRK / USART1_RX / TMR1_CH3 / I2C1_SDA / ERTC_REFIN	—
17[3]	21	32	44	PA11	I/O	TC	EVENTOUT / USART1_CTS / TMR1_CH4 / SPI3_CS / I2S3_WS / CAN1_RX / I2C2_SCL / I2C1_SMBA	OTGFS1_D-[3]
18[3]	22	33	45	PA12	I/O	TC	EVENTOUT / USART1_RTS_DE / TMR1_EXT / CAN1_TX / I2C2_SDA / SPI3_MISO / I2S3_MCK	OTGFS1_D+[3]
19	23	34	46	PA13 (SWDIO[5])	I/O	FT	PA13 / IR_OUT / OTGFS1_OE / I2S_SDEXT / SPI3_MISO / I2S3_MCK / I2C1_SDA / SPI2_MISO / I2S2_MCK	—
		35	47	PF6	I/O	FT	I2C2_SCL / USART4_RX	—
		36	48	PF7	I/O	FT	I2C2_SDA / USART4_TX	—
20	24	37	49	PA14 (SWCLK[5])	I/O	FT	PA14 / USART2_TX / SPI3_MOSI / I2S3_SD / I2C1_SMBA / SPI2_MOSI / I2S2_SD	—
	25	38	50	PA15	I/O	FT	SPI1_CS / I2S1_WS / USART2_RX / TMR2_CH1 / TMR2_EXT / EVENTOUT / USART4_RTS_DE / OTGFS1_OE / SPI2_CS / I2S2_WS / SPI3_CS / I2S3_WS	—
			51	PC10	I/O	FT	USART4_TX / USART3_TX / SPI3_SCK / I2S3_CK	—
			52	PC11	I/O	FT	USART4_RX / USART3_RX / I2S_SDEXT / SPI3_MISO / I2S3_MCK	—
			53	PC12	I/O	FT	USART4_CK / USART3_CK / SPI3_MOSI / I2S3_SD	—
			54	PD2[6]	I/O	FT	TMR3_EXT / USART3_RTS_DE	—
	26	39	55	PB3	I/O	FT	SPI1_SCK / I2S1_CK / EVENTOUT / TMR2_CH2 / USART1_RTS_DE / USART2_CTS / SPI2_SCK / I2S2_CK / SWO	—
	27	40	56	PB4	I/O	FT	SPI1_MISO / I2S1_MCK / TMR3_CH1 / EVENTOUT / I2S_SDEXT / USART1_CTS / TMR17_BRK / SPI2_MISO / I2S2_MCK / I2C1_SDA	—
	28	41	57	PB5	I/O	FT	SPI1_MOSI / I2S1_SD / TMR3_CH2 / TMR16_BRK / I2C1_SMBA / USART1_CK / USART2_RTS_DE / SPI2_MOSI / I2S2_SD	WKUP6
	29	42	58	PB6	I/O	FT	USART1_TX / I2C1_SCL / TMR16_CH1C / USART4_CK / I2S1_MCK / SPI3_CS / I2S3_WS	—
	30	43	59	PB7	I/O	FT	USART1_RX / I2C1_SDA / TMR17_CH1C / USART4_CTS / SPI3_SCK / I2S3_CK	—
1	31	44	60	BOOT0	I	B	Boot mode 0	
	32	45	61	PB8	I/O	FTf	USART1_TX / I2C1_SCL / TMR16_CH1 / EVENTOUT / CAN1_RX / SPI3_MISO / I2S3_MCK	—
		46	62	PB9	I/O	FTf	IR_OUT / I2C1_SDA / TMR17_CH1 / EVENTOUT / CAN1_TX / SPI2_CS / I2S2_WS / I2S1_MCK / SPI3_MOSI / I2S3_SD	—
		47	63	V_{SS}	S	—	Digital ground	
		48	64	V_{DD}	S	—	Digital power supply	
		-/49		EPAD (V_{SS})	S	—	Digital ground	
	33			EPAD (V_{SS}/V_{SSA})	S	—	Digital ground / analog ground	

Note: 1. I = input, O = output, S = supply.

2. TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor. Among them, FTa pin has 5 V-tolerant characteristics when configured as input floating, input pull-up, or input pull-down mode. However, it cannot be 5 V-tolerant when configured as analog mode. In this case, its input level should not be higher than V_{DD} + 0.3 V.
3. For the 20TSSOP package, if OTGFS1 is disabled, it is possible to replace PA9/PA10 and their multiplexed functions with PA11/PA12 and their multiplexed functions by means of software remapping. If OTGFS1 is enabled, PA9/PA10/PA11/PA12 and their relevant multiplexed functions will be owned by OTGFS1_D- and OTGFS1_D+. In this case, the OTGFS1_VBUS and OTGFS1_ID signals are not present, and some of OTG functions are restricted when it is used as a host.
4. PA9/10 in the 20TSSOP package are not FT 5 V-tolerant.
5. After any reset, PA13/PA14 are used as their multiplexed functions SWDIO/SWCLK, and the internal pull-up resistor of SWDIO and the internal pull-down resistor of SWCLK are both ON.
6. When LEXT is enabled, PD2 and its multiple functions cannot be used.

5 Electrical Characteristics

Test Conditions

Minimum and Maximum Values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

Typical Values

Typical values are based on T_A = 25 °C, V_{DD} = 3.3 V.

Typical Curves

All typical curves are provided only as design guidelines and are not tested.

Power Supply Scheme

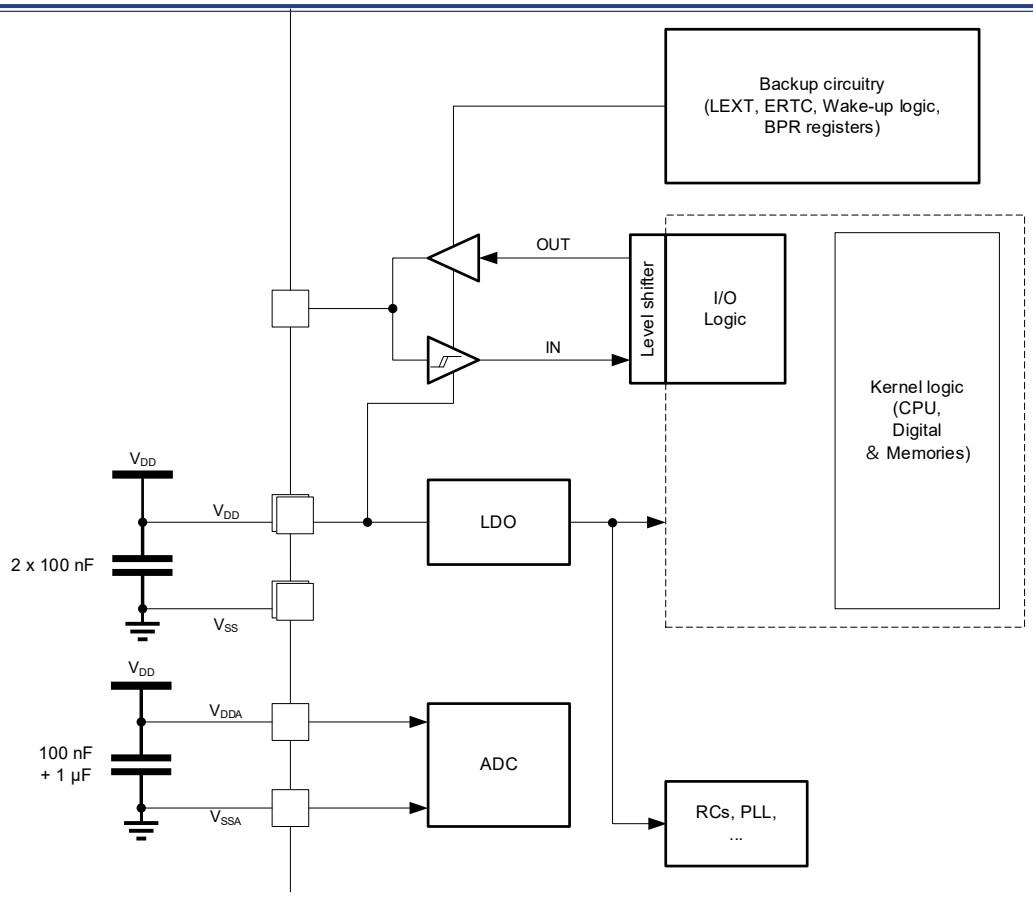


Figure 8. Power Supply Scheme

Absolute Maximum Values

Ratings

If stresses were out of the absolute maximum ratings listed in the following tables, it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 5. Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
V_{DDx}-V_{SS}	External Main Supply Voltage	-0.3	4.0	V
V_{IN}	Input Voltage on FT and FTf GPIO	V_{SS}-0.3	6.0	
	Input Voltage on FTa GPIO (Set as Input Floating, Input Pull-up, or Input Pull-down Mode)			
	Input Voltage on TC GPIO	V_{SS}-0.3	4.0	
	Input Voltage on FTa GPIO (Set as Analog Mode)			
$\lvert\Delta V_{DDx}\rvert$	Variations between Different V_{DD} Power Pins	—	50	mV
$\lvert V_{SSx}$-$V_{SS}\rvert$	Variations between All the Different Ground Pins	—	50	

Table 6. Current Characteristics

Symbol	Description	Max.	Unit
I_{VDD}	Total Current into V_{DD} Power Line (Source)	150	mA
I_{VSS}	Total Current out of V_{SS} Ground Lines (Sink)	150	
I_{IO}	Output Current Sunk by any GPIO and Control Pin	25	
	Output Current Source by any GPIO and Control Pin	-25	

Table 7. Temperature Characteristics

Symbol	Description	Max.	Unit
T_{STG}	Storage Temperature Range	-60 ~ +150	°C
T_J	Maximum Junction Temperature	125	

Electrical Sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic Discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2017/JS-002-2018 standard.

Table 8. ESD Values

Symbol	Parameter	Conditions	Class	Min.	Unit
$V_{ESD(HBM)}$	Electrostatic Discharge Voltage (Human Body Model)	T_A = +25 °C, conforming to JS-001-2017	3A	±6000	V
$V_{ESD(CDM)}$	Electrostatic Discharge Voltage (Charge Device Model)	T_A = +25 °C, conforming to JS-002-2018	III	±2000	

Static Latch-up

Tests compliant with EIA/JESD78E IC latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 9. Static Latch-up Values

Symbol	Parameter	Conditions	Level/Class
LU	Static Latch-up Class	T_A = +105 °C, conforming to EIA/JESD78E	II level A (±200 mA)

General Operating Conditions

Table 10. General Operating Conditions

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{HCLK}	Internal AHB Clock Frequency	—	0	96	MHz
$f_{PCLK1/2}$	Internal APB1/2 Clock Frequency	—	0	f_{HCLK}	MHz
V_{DD}	Digital Operating Voltage	—	2.4	3.6	V
V_{DDA}	Analog Operating Voltage	Must be the same potential as V_{DD}	V_{DD}		V
P_D	Power Dissipation, T_A = 105 °C	64LQFP (7 mm × 7 mm)	—	234	
		48LQFP (7 mm × 7 mm)	—	234	
		32QFN (4 mm × 4 mm)	—	370	
		20TSSOP (6.5 mm × 4.4 mm)	—	195	
T_A	Ambient Temperature	—	-40	105	°C

Operating Conditions at Power-up / Power-down

Table 11. Operating Conditions at Power-up / Power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t_{VDD}	V_{DD} Rising Time Rate	—	0	∞	ms/V
	V_{DD} Falling Time Rate		20	∞	μs/V

Embedded Reset and Rower Control Block Characteristics

Table 12. Embedded Reset and Power Management Block Characteristics (1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{POR}	Power on Reset Threshold	1.91	2.11	2.4	V
V_{LVR}	Low Voltage Reset Threshold	1.78(2)	1.93	2.08	V
$V_{LVRhyst}$	LVR Hysteresis	—	180	—	mV
$T_{RESTTEMPO}$	Reset Temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RESTTEMPO}$	—	3.5	—	ms

Note: 1. Guaranteed by design, not tested in production.
2. The product behavior is guaranteed by design down to the minimum VLVR value.

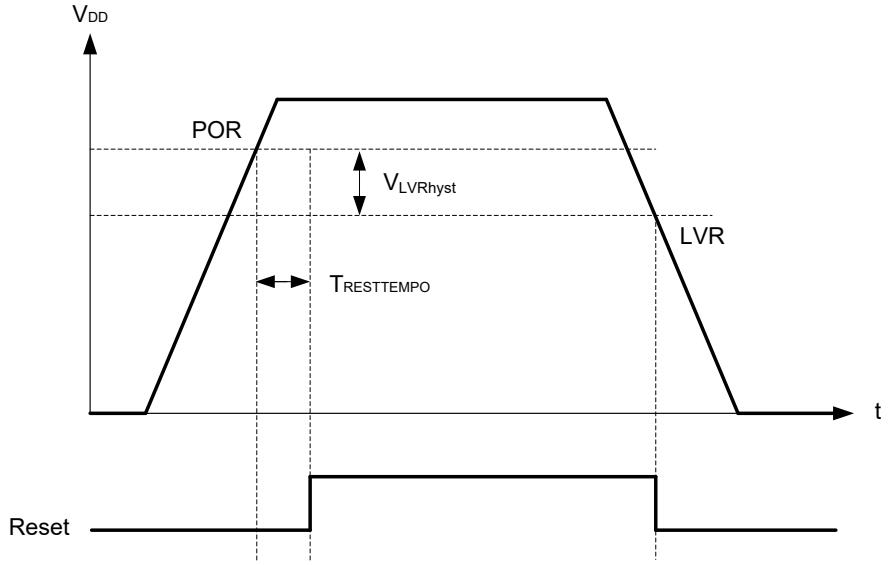


Figure 9. Power on Reset and Low Voltage Reset Waveform

Table 13. Programmable Voltage Regulator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{PVM1}	PVM Threshold 1 (PVMSEL[2:0] = 001)	Rising edge(1)	2.19	2.28	2.37	V
		Falling edge(1)	2.09	2.18	2.27	V
V_{PVM2}	PVM Threshold 2 (PVMSEL[2:0] = 010)	Rising edge(2)	2.28	2.38	2.48	V
		Falling edge(2)	2.18	2.28	2.38	V
V_{PVM3}	PVM Threshold 3 (PVMSEL[2:0] = 011)	Rising edge(2)	2.38	2.48	2.58	V
		Falling edge(2)	2.28	2.38	2.48	V
V_{PVM4}	PVM Threshold 4 (PVMSEL[2:0] = 100)	Rising edge(2)	2.47	2.58	2.69	V
		Falling edge(2)	2.37	2.48	2.59	V
V_{PVM5}	PVM Threshold 5 (PVMSEL[2:0] = 101)	Rising edge(2)	2.57	2.68	2.79	V
		Falling edge(2)	2.47	2.58	2.69	V
V_{PVM6}	PVM Threshold 6 (PVMSEL[2:0] = 110)	Rising edge(2)	2.66	2.78	2.9	V
		Falling edge(2)	2.56	2.68	2.8	V
V_{PVM7}	PVM Threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(2)	PVM Hysteresis	—	—	100	—	mV
$I_{DD\ (PVM)}$(2)	PVM Current Dissipation	—	—	20	30(2)	μA

Note: 1. PVMSEL[2:0] = 001 level may not be used because it is lower than V_{POR}.
2. Guaranteed by characterization results, not tested in production.

Memory Characteristics

Table 14. Internal Flash Memory Characteristics (Note)

Symbol	Parameter	Typ.	Max.	Unit
T_{PROG}	Programming Time	60	65	μs
t_{SE}	Sector Erase Time	6.6	8	ms
t_{ME}	Mass Erase Time	8.2	10	ms

Note: Guaranteed by design, not tested in production.

Table 15. Internal Flash Memory Endurance and Data Retention (Note)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	—	—	kcycles
t_{RET}	Data Retention	T_A = 105 °C	10	—	—	year

Note: Guaranteed by design, not tested in production.

Supply Current Characteristics

The current consumption is subjected to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on the f_{HCLK} frequency (0 ~ 32 MHz : zero-wait state; 33 ~ 64 MHz: one wait state; 65 ~ 96 MHz: two wait states)
- Prefetch ON, HalfCycle OFF
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition, and the maximum values are measured with V_{DD} = 3.6 V.

Table 16. Typical Current Consumption in Run Mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				All Peripherals Enabled	All Peripherals Disabled	
I_{DD}	Supply Current in Run Mode	High speed external crystal (HEXT) (1)(2)	96 MHz	17.7	7.88	mA
			72 MHz	13.5	6.09	
			48 MHz	9.52	4.62	
			36 MHz	7.32	3.65	
			24 MHz	5.44	2.99	
			16 MHz	3.87	2.24	
			8 MHz	1.94	1.20	
			4 MHz	1.31	0.94	
			2 MHz	1.00	0.81	
			1 MHz	0.83	0.74	
			500 kHz	0.76	0.71	
			125 kHz	0.70	0.69	
		High speed internal clock (HICK) (2)	96 MHz	17.6	7.76	mA
			72 MHz	13.4	5.96	
			48 MHz	9.41	4.48	
			36 MHz	7.20	3.50	
			24 MHz	5.30	2.83	
			16 MHz	3.72	2.08	
			8 MHz	1.78	1.03	
			4 MHz	1.15	0.78	
			2 MHz	0.82	0.64	
			1 MHz	0.67	0.58	
			500 kHz	0.59	0.54	
			125 kHz	0.53	0.52	

Note: 1. External clock is 8 MHz.
2. PLL is on when f_{HCLK} > 8 MHz.

Table 17. Typical Current Consumption in Sleep Mode

Symbol	Parameter	Conditions	f_{HCLK}	Typ.		Unit
				All Peripherals Enabled	All Peripherals Disabled	
I_{DD}	Supply Current in Sleep Mode	High speed external crystal (HEXT) (1)(2)	96 MHz	14.2	3.03	mA
			72 MHz	10.8	2.45	
			48 MHz	7.77	2.19	
			36 MHz	6.01	1.82	
			24 MHz	4.56	1.77	
			16 MHz	3.29	1.43	
			8 MHz	1.65	0.80	
			4 MHz	1.16	0.74	
			2 MHz	0.92	0.71	
			1 MHz	0.80	0.69	
			500 kHz	0.74	0.69	
			125 kHz	0.69	0.68	
		High speed internal clock (HICK) (2)	96 MHz	14.1	2.87	mA
			72 MHz	10.7	2.29	
			48 MHz	7.66	2.03	
			36 MHz	5.88	1.67	
			24 MHz	4.42	1.61	
			16 MHz	3.14	1.26	
			8 MHz	1.49	0.63	
			4 MHz	1.00	0.57	
			2 MHz	0.75	0.54	
			1 MHz	0.63	0.53	
			500 kHz	0.57	0.52	
			125 kHz	0.53	0.51	

Note: 1. External clock is 8 MHz.
2. PLL is on when f_{HCLK} > 8 MHz.

Table 18. Maximum Current Consumption in Run Mode

Symbol	Parameter	Conditions	f_{HCLK}	Max.		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply Current in Run Mode	High speed external crystal (HEXT) (Note), all peripherals enabled	96 MHz	17.9	18.1	mA
			72 MHz	13.7	13.9	
			48 MHz	9.72	9.90	
			36 MHz	7.52	7.70	
			24 MHz	5.64	5.83	
			16 MHz	4.08	4.26	
			8 MHz	2.17	2.36	
		High speed external crystal (HEXT) (Note), all peripherals disabled	96 MHz	8.08	8.25	mA
			72 MHz	6.30	6.48	
			48 MHz	4.83	5.01	
			36 MHz	3.86	4.04	
			24 MHz	3.21	3.39	
			16 MHz	2.46	2.64	
			8 MHz	1.44	1.61	

Note: External clock is 8 MHz, and PLL is on when f_{HCLK} > 8 MHz.

Table 19. Maximum Current Consumption in Sleep Mode

Symbol	Parameter	Conditions	f_{HCLK}	Max.		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply Current in Sleep Mode	High speed external crystal (HEXT) (Note), all peripherals enabled	96 MHz	14.4	14.6	mA
			72 MHz	11.1	11.3	
			48 MHz	7.99	8.17	
			36 MHz	6.22	6.40	
			24 MHz	4.78	4.96	
			16 MHz	3.51	3.69	
			8 MHz	1.89	2.07	
		High speed external crystal (HEXT) (Note), all peripherals disabled	96 MHz	3.25	3.44	mA
			72 MHz	2.68	2.87	
			48 MHz	2.42	2.60	
			36 MHz	2.05	2.23	
			24 MHz	2.00	2.18	
			16 MHz	1.65	1.84	
			8 MHz	1.03	1.22	

Note: External clock is 8 MHz, and PLL is on when f_{HCLK} > 8 MHz.

Table 20. Typical and Maximum Current Consumptions in Deepsleep and Standby Modes

Symbol	Parameter	Conditions	Typ.(1)		Max.(2)			Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply Current in Deepsleep Mode (3)	LDO in Run mode, HICK and HEXT OFF, WDT OFF	243	246	275	468	675	µA
		LDO in low-power mode, VREXLPEN=1, HICK and HEXT OFF, WDT OFF	121	123	135	259	402	
	Supply Current in Standby Mode	LEXT and ERTC OFF	2.3	3.5	4.5	5.9	8.2	µA
		LEXT and ERTC ON	3.3	5.0	5.7	7.2	9.6	

Note: 1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results, not tested in production.
3. CRM_AHBEN[4] (FLASHEN) must be set to 1 before entering Deepsleep mode; otherwise, an additional power consumption of around 50 µA would be added.

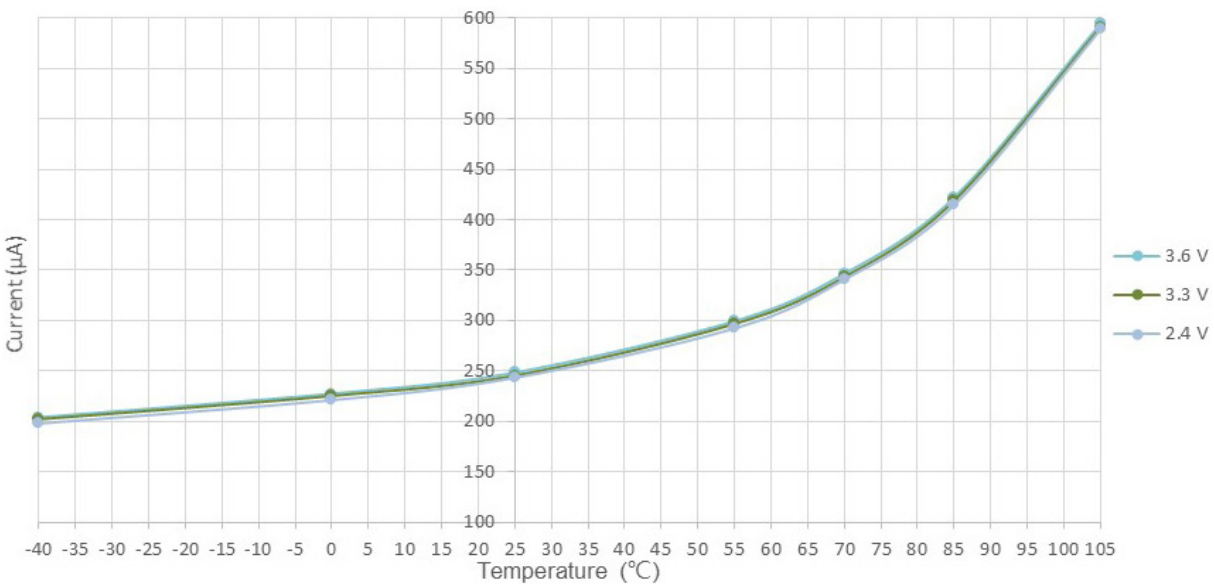


Figure 10. Typical Current Consumption in Deepsleep Mode with LDO in Run Mode vs. Temperature at Different V_{DD}

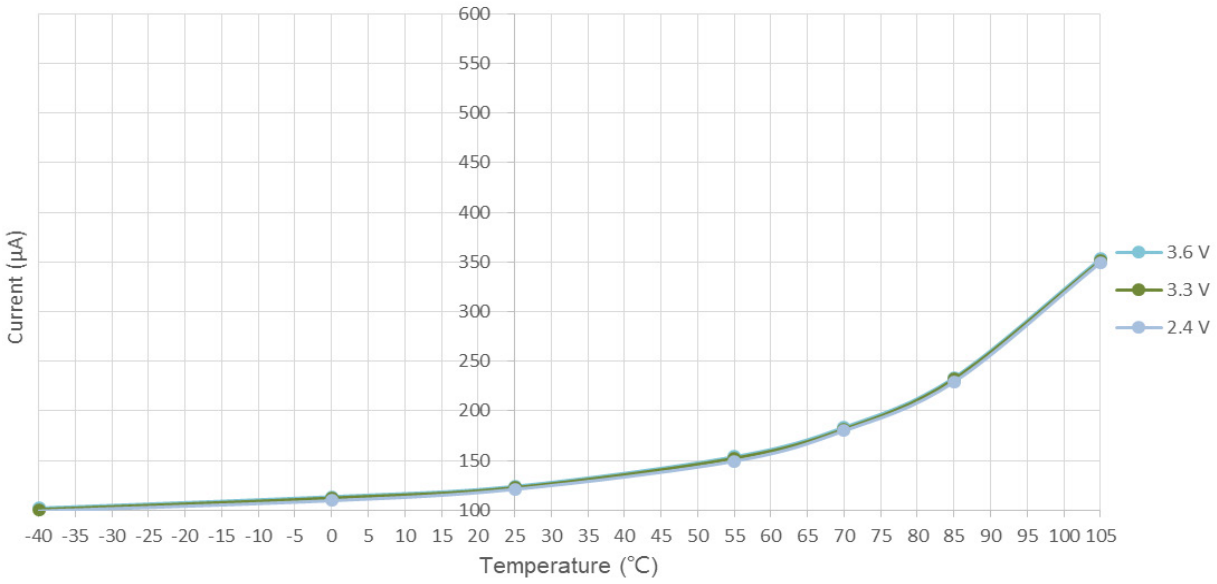


Figure 11. Typical Current Consumption in Deepsleep Mode with LDO in Low-power Mode vs. Temperature at Different V_{DD}

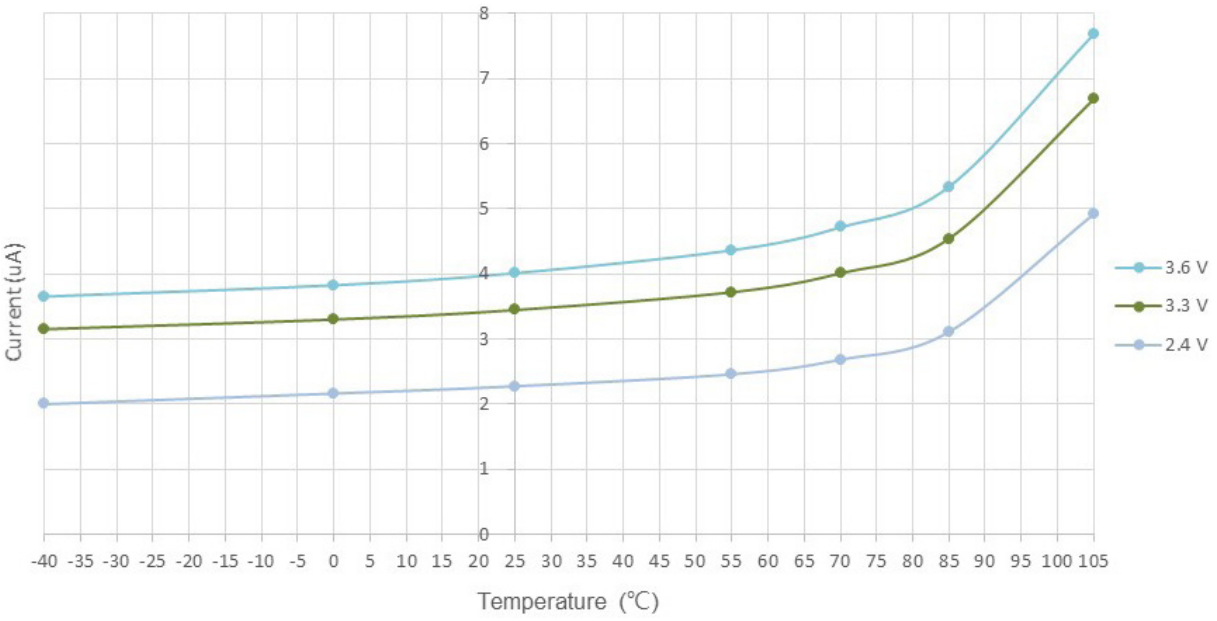


Figure 12. Typical Current Consumption in Standby Mode vs. Temperature at Different V_{DD}

On-chip Peripheral Current Consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between "all peripherals clocked OFF" and "only one peripheral clocked ON".

Table 21. Peripheral Current Consumption

Peripheral		Typ.	Unit
AHB	DMA1	2.20	μA/MHz
	SRAM	0.56	
	Flash	11.6	
	CRC	0.53	
	OTGFS1	23.6	
	GPIOA	0.62	
	GPIOB	0.58	
	GPIOC	0.57	
	GPIOD	0.55	
	GPIOF	0.56	
APB1	TMR2	9.47	
	TMR3	6.71	
	TMR6	0.86	
	TMR7	0.86	
	TMR13	2.63	
	TMR14	2.58	
	WWDT	0.33	
	SPI2/I²S2	1.91	
	SPI3/I²S3	1.92	
	USART2	2.06	
	USART3	2.09	
	USART4	2.11	
	I²C1	6.11	
	I²C2	5.88	
	CAN1	2.26	
	ACC	0.26	
	PWC	6.27	
APB2	SCFG	0.17	
	ADC1	1.90	
	TMR1	9.21	
	SPI1/I²S1	1.88	
	USART1	2.11	
	TMR15	5.16	
	TMR16	3.55	
	TMR17	3.62	

External Clock Source Characteristics

High-speed External Clock Generated from a Crystal / Ceramic Resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 22. HEXT 4 ~ 25 MHz Crystal Characteristics (1)(2)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HEXT_IN}	Oscillator Frequency	—	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup Time	V_{DD} is stabilized	—	2	—	ms

Note: 1. Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by characterization results, not tested in production.

3. $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be taken into account (10 pF can be used as a rough estimate of the combined pin and board capacitance) when selecting C_{L1} and C_{L2}.

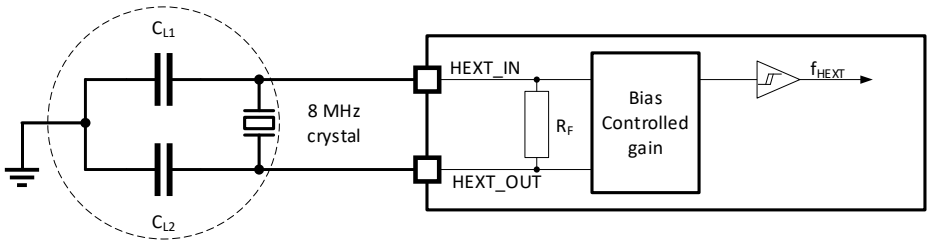


Figure 13. HEXT Typical Application with an 8 MHz Crystal

High-speed External Clock Generated from an External Source

The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 23. HEXT External Source Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HEXT_ext}	User External Clock Source Frequency (Note)	—	1	8	25	MHz
V_{HEXTH}	HEXT_IN Input Pin High Level Voltage		0.7V_{DD}	—	V_{DD}	V
V_{HEXTL}	HEXT_IN Input Pin Low Level Voltage		V_{SS}	—	0.3V_{DD}	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN High or Low Time(Note)		5	—	—	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN Rising or Falling time(Note)		—	—	20	
$C_{in(HEXT)}$	HEXT_IN Input Capacitance (Note)	—	—	5	—	pF
$Duty_{(HEXT)}$	Duty Cycle	—	45	—	55	%
I_L	HEXT_IN Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	±1	μA

Note: Guaranteed by design, not tested in production.

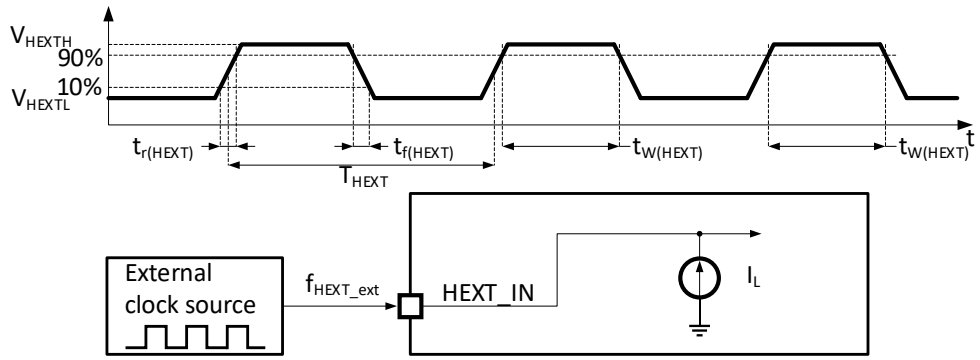


Figure 14. HEXT External Source AC Timing Diagram

Low-speed External Clock Generated from a Crystal / Ceramic Resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal / ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. LEXT 32.768 kHz Crystal Characteristics (1)(2)

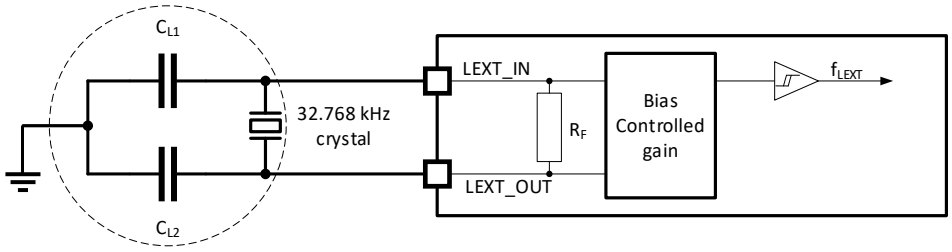
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{SU(LEXT)}$	Startup Time	V_{DD} is stabilized	—	200	—	ms

Note: 1. Oscillator characteristics given by the crystal / ceramic resonator manufacturer.

2. Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range and select to meet the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Figure 15. LEXT Typical Application with a 32.768 kHz Crystal

Low-speed External Clock Generated from an External Source

The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 25. LEXT External Source Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LEXT_ext}	User External Clock Source Frequency (Note)	—	—	32.768	1000	kHz
V_{LEXTH}	LEXT_IN Input Pin High Level Voltage	—	$0.7V_{DD}$	—	V_{DD}	V
V_{LEXTL}	LEXT_IN Input Pin Low Level Voltage	—	V_{SS}	—	$0.3V_{DD}$	V
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN High or Low Time (Note)	—	450	—	—	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN Rising or Falling Time (Note)	—	—	—	50	ns
$C_{in(LEXT)}$	LEXT_IN Input Capacitance (Note)	—	—	5	—	pF
$Duty_{(LEXT)}$	Duty Cycle	—	30	—	70	%
I_L	LEXT_IN Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	—	—	±1	μA

Note: Guaranteed by design, not tested in production.

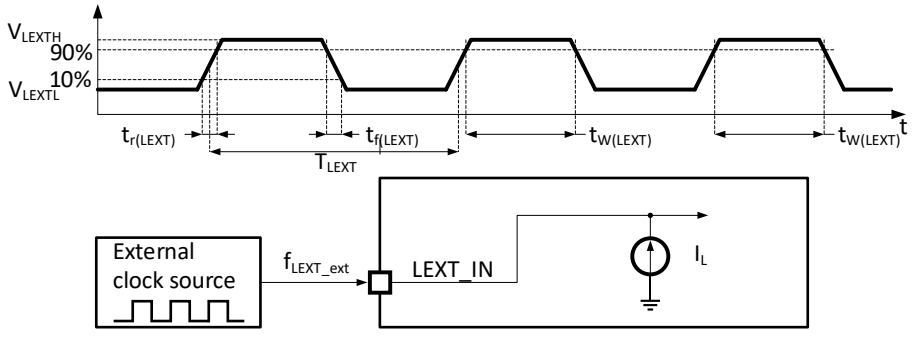


Figure 16. LEXT External Source AC Timing Diagram

Internal Clock Source Characteristics

High-speed Internal Clock (HICK)

Table 26. HICK Clock Characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
f_{HICK}	Frequency	—		—	48	—	MHz
$DuCy_{(HICK)}$	Duty Cycle	—		45	—	55	%
ACC_{HICK}	Accuracy of the HICK Oscillator	User-trimmed with the CRM_CTRL register(1)		-1	—	1	%
		ACC-trimmed(1)		-0.25	—	0.25	
		Factory-calibrated (2)	T_A = -40 ~ 105 °C	-2	—	2	
			T_A = -40 ~ 85 °C	-1.5	—	1.5	
			T_A = 0 ~ 70 °C	-1	—	1	
			T_A = 25 °C	-1	0.5	1	
$t_{SU(HICK)}$(2)	HICK Oscillator Startup Time	—		—	—	10	μs
$I_{DD(HICK)}$(2)	HICK Oscillator Power Consumption	—		—	230	240	μA

Note: 1. Guaranteed by design, not tested in production.
2. Guaranteed by characterization results, not tested in production.

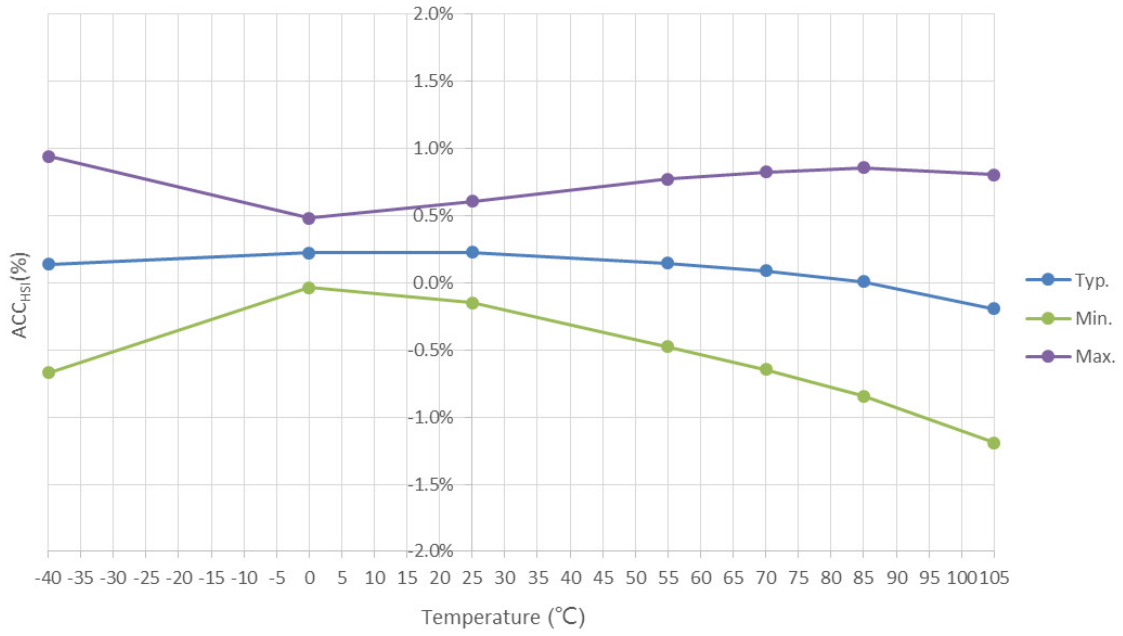


Figure 17. HICK Clock Frequency Accuracy vs. Temperature

Low-speed Internal Clock (LICK)

Table 27. LICK Clock Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LICK}(Note)	Frequency	—	25	35	45	kHz

Note: Guaranteed by characterization results, not tested in production.

PLL Characteristics

Table 28. PLL Characteristics

Symbol	Parameter	Min.(1)	Typ.	Max.(1)	Unit
f_{PLL_IN}	PLL Input Clock (2)	2	8	16	MHz
	PLL Input Clock Duty Cycle	40	—	60	%
f_{PLL_OUT}	PLL Multiplier Output Clock	16	—	96	MHz
t_{LOCK}	PLL Lock Time	—	—	200	μs
Jitter	Cycle-to-Cycle Jitter	—	—	300	ps

Note: 1. Guaranteed by design, not tested in production.

2. Take care of using the appropriate multiplier factors to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

Wakeup Time from Low-power Mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK.

Table 29. Low-power Mode Wakeup Time

Symbol	Parameter	Typ.	Unit
$t_{WUSLEEP}$	Wakeup from Sleep Mode	3.3	μs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep Mode (LDO in Run Mode)	380	μs
	Wakeup from Deepsleep Mode (LDO in Low-power Mode)	450	
$t_{WUSTDBY}$	Wakeup from Standby Mode	800	μs

EMC Characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (Electromagnetic Susceptibility)

- EFT: A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 30. EMS Characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional error, V_{DD} and V_{SS} input has one 47 μF capacitor and each V_{DD} and V_{SS} pin pair 0.1 μF	V_{DD} = 3.3 V, 48LQFP, T_A = +25 °C, f_{HCLK} = 96 MHz, HalfCycle = 0, conforms to IEC 61000-4-4	4A (±4 kV)
		V_{DD} = 3.3 V, 48LQFP, T_A = +25 °C, f_{HCLK} = 80 MHz, HalfCycle = 1, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

GPIO Port Characteristics

General Input / Output Characteristics

All GPIOs are CMOS and TTL compliant.

Table 31. GPIO Static Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	GPIO Input Low Level Voltage	—	-0.3	—	$0.28\times V_{DD}$ + 0.1	V
V_{IH}	TC GPIO Input High Level Voltage	—	$0.31 \times V_{DD}$ + 0.8	—	V_{DD} + 0.3	V
	FTa GPIO Input High Level Voltage	Analog mode				
	FT and FTf GPIO Input High Level Voltage	—		—	5.5	
	FTa GPIO Input High Level Voltage	Input floating, input pull-up, or input pull-down mode				
V_{hys}	Schmitt Trigger Voltage Hysteresis (1)	—	200	—	—	mV
			5% V_{DD}	—	—	
I_{lkg}	Input Floating Leakage Current (2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIO	—	—	±1	μA
		$V_{SS} \le V_{IN} \le 5.5$ V FT, FTf and FTa GPIOs	—	—	±1	
R_{PU}	Weak Pull-up Equivalent Resistor (3)	$V_{IN} = V_{SS}$	65	80	130	kΩ
R_{PD}	Weak Pull-down Equivalent Resistor (3)(4)	$V_{IN} = V_{DD}$	65	70	130	kΩ
C_{IO}	GPIO Pin Capacitance	—	—	9	—	pF

Note: 1. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.

2. Leakage could be higher than max if negative current is injected on adjacent pins.

3. Internal pull-up/pull-down resistors must be disabled when FT, FTf and FTa input voltage is higher than V_{DD} + 0.3V.

4. The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output Driving Current

In the user application, the number of GPIO pins that can drive current must be controlled to respect the absolute maximum rating defined in the “Absolute Maximum Values → Ratings” section.

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see Table 3).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see Table 3).

Output Voltage Levels

All GPIOs are CMOS and TTL compliant.

Table 32. Output Voltage Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
Normal Sourcing/Sinking Strength					
V_{OL}(1)	Output Low Level Voltage	CMOS port, I_{IO} = 4 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-0.4	—	
V_{OL}(1)	Output Low Level Voltage	TTL port, I_{IO} = 2 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		2.4	—	
V_{OL}(1)	Output Low Level Voltage	I_{IO} = 9 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	1.3	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-1.3	—	
V_{OL}(1)	Output Low Level Voltage	I_{IO} = 2 mA 2.4 V ≤ V_{DD} < 2.7 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-0.4	—	
Large Sourcing/Sinking Strength					
V_{OL}	Output Low Level Voltage	CMOS port, I_{IO} = 6 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OH}	Output High Level Voltage		V_{DD}-0.4	—	
V_{OL}(1)	Output Low Level Voltage	TTL port, I_{IO} = 5 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		2.4	—	
V_{OL}(1)	Output Low Level Voltage	I_{IO} = 18 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	1.3	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-1.3	—	
V_{OL}(1)	Output Low Level Voltage	I_{IO} = 4 mA 2.4 V ≤ V_{DD} < 2.7 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-0.4	—	
Maximum Sourcing/Sinking Strength					
V_{OL}(1)	Output Low Level Voltage	CMOS port, I_{IO} = 15 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-0.4	—	
V_{OL}(1)	Output Low Level Voltage	TTL port, I_{IO} = 12 mA 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		2.4	—	
V_{OL}(1)	Output Low Level Voltage	I_{IO} = 12 mA 2.4 V ≤ V_{DD} < 2.7 V	—	0.4	V
V_{OH}(1)	Output High Level Voltage		V_{DD}-0.4	—	
Ultra High Sinking Strength (2)					
V_{OL}	Output Low Level Voltage	I_{IO} = 25 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	—	0.4	V
V_{OL}(1)	Output Low Level Voltage	I_{IO} = 18 mA, 2.4 V ≤ V_{DD} < 2.7 V			

Note: 1. Guaranteed by characterization results, not tested in production.

2. When GPIO ultra high sinking strength is enabled, its V_{OH} is the same as that of maximum sourcing strength.

Input AC Characteristics

The definition and values of input AC characteristics are given as follows.

Table 33. Input AC Characteristics

Symbol	Parameter	Min.	Max.	Unit
$t_{EXINTpw}$	Pulse Width of External Signals Detected by EXINT Controller	10	—	ns

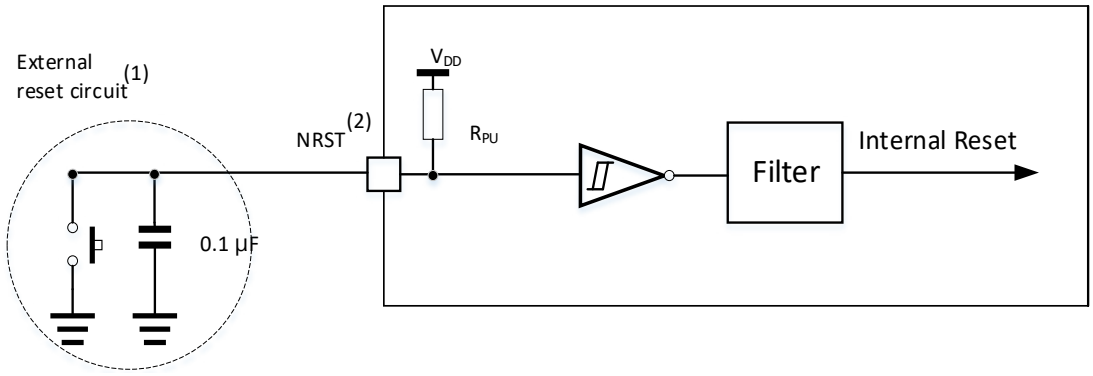
NRST Pin Characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 34. NRST Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}$(Note)	NRST Input Low Level Voltage	—	-0.5	—	0.8	V
$V_{IH(NRST)}$(Note)	NRST Input High Level Voltage	—	2	—	V_{DD} + 0.3	
$V_{hys(NRST)}$	NRST Schmitt Trigger Voltage Hysteresis	—	—	500	—	mV
R_{PU}	Weak Pull-up Equivalent Resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(Note)	NRST Input Low Level Invalid Time	—	—	—	40	μs
$t_{ILNV(NRST)}$(Note)	NRST Input Low Level Valid Time	—	80	—	—	μs

Note: Guaranteed by design, not tested in production.



Note: 1. The reset network protects the device against parasitic resets.

2. The user must ensure that the level on the NRST pin can go below the $V_{IL\ (NRST)}$ max level specified in Table 31. Otherwise, the reset will not be performed by the device.

Figure 18. Recommended NRST Pin Protection

TMR Timer Characteristics

The parameters given in the table below are guaranteed by design.

Table 35. TMR Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{res(TMR)}$	Timer Resolution Time	—	1	—	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 96 MHz	10.42	—	ns
f_{EXT}	Timer External Clock Frequency on CH1 to CH4	—	0	$f_{TMRxCLK}$/2	MHz

SPI Characteristics

Table 36. SPI Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
f_{SCK} (1) $t_{c(SCK)}$)(1)	SPI Clock Frequency(2)(3)	Master mode	—	36	MHz
		Slave receive mode	—	36	
		Slave transmit mode	—	32	
$t_{su(CS)}$(1)	CS Setup Time	Slave mode	$4t_{PCLK}$	—	ns
$t_{h(CS)}$(1)	CS Hold Time	Slave mode	$2t_{PCLK}$	—	ns
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK High and Low Time	Master mode, prescaler = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}$(1)	Data Input Setup Time	Master mode	6	—	ns
$t_{su(SI)}$(1)		Slave mode	5	—	
$t_{h(MI)}$(1)	Data Input Hold Time	Master mode	4	—	ns
$t_{h(SI)}$(1)		Slave mode	5	—	
$t_{a(SO)}$(1)(4)	Data Output Access Time	Slave mode	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{dis(SO)}$(1)(5)	Data Output Disable Time	Slave mode	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{v(SO)}$(1)	Data Output Valid Time	Slave mode (after enable edge)	—	25	ns
$t_{v(MO)}$(1)	Data Output Valid Time	Master mode (after enable edge)	—	10	ns
$t_{h(SO)}$(1)	Data Output Hold Time	Slave mode (after enable edge)	9	—	ns
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	—	

Note: 1. Guaranteed by design, not tested in production.
2. The maximum SPI clock frequency should not exceed $f_{PCLK}/2$.
3. The maximum SPI clock frequency is highly related with devices and the PCB layout.
4. Min time is the minimum time to drive the output and the max time is for the maximum time to validate the data.
5. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

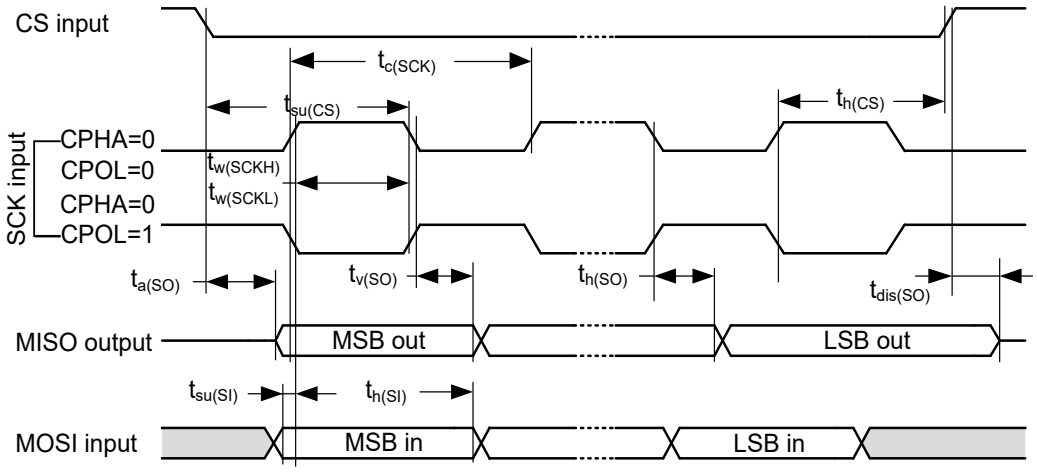


Figure 19. SPI Timing Diagram – Slave Mode and CPHA = 0

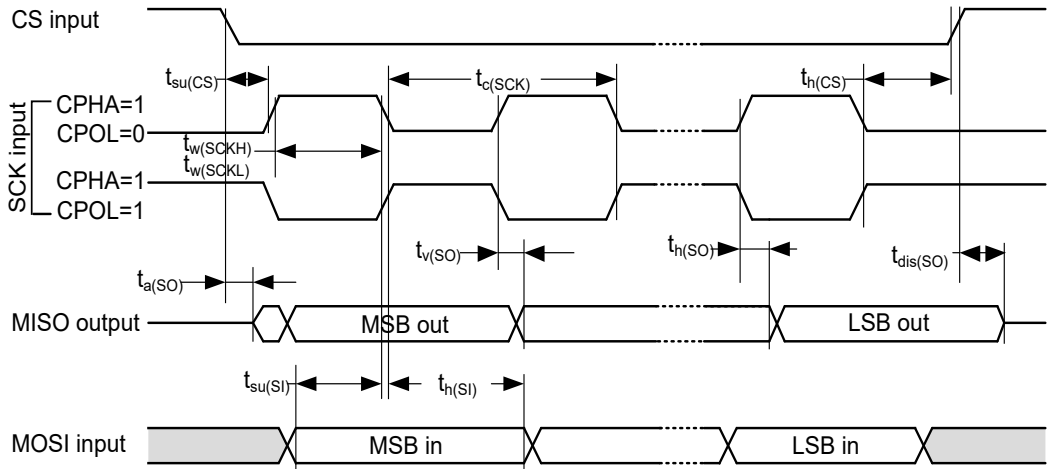


Figure 20. SPI Timing Diagram – Slave Mode and CPHA = 1

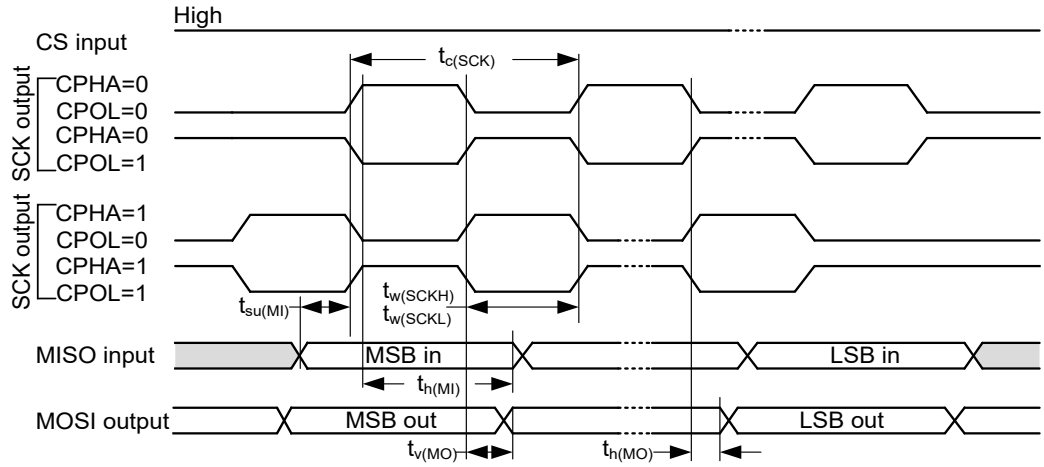


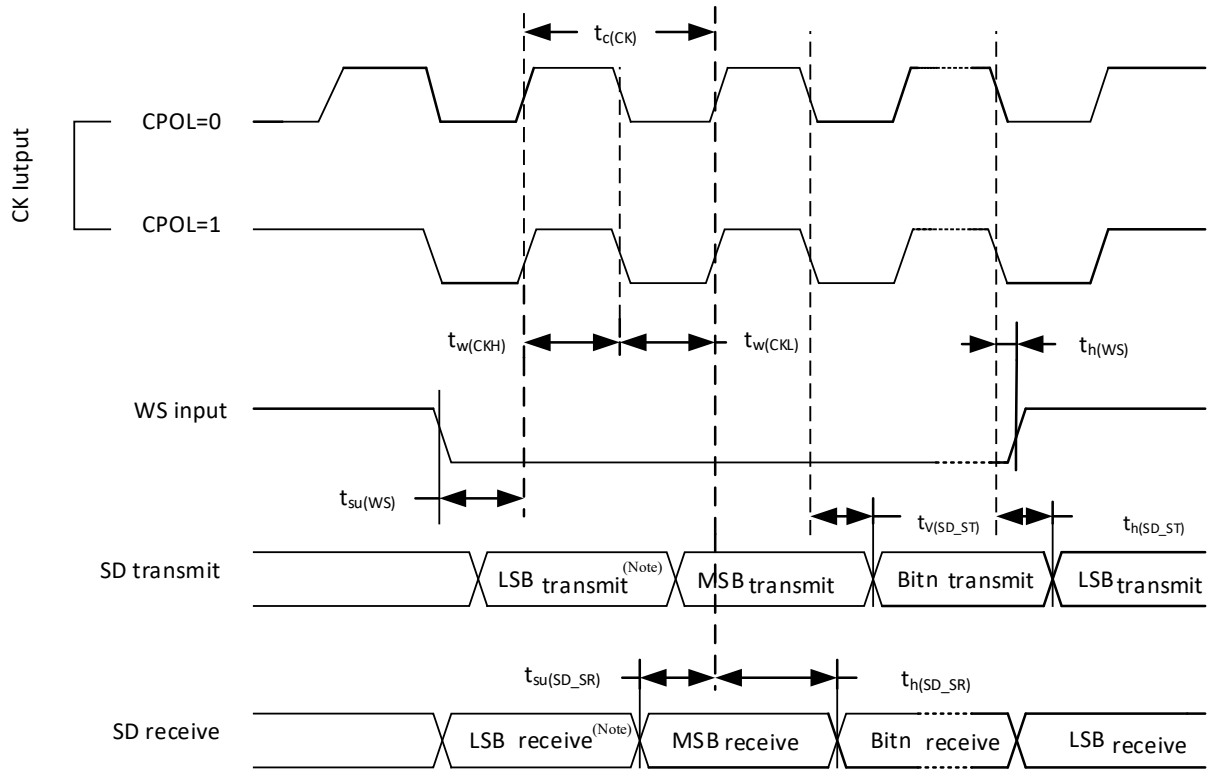
Figure 21. SPI Timing Diagram – Master Mode

I²S Characteristics

Table 37. I²S Characteristics

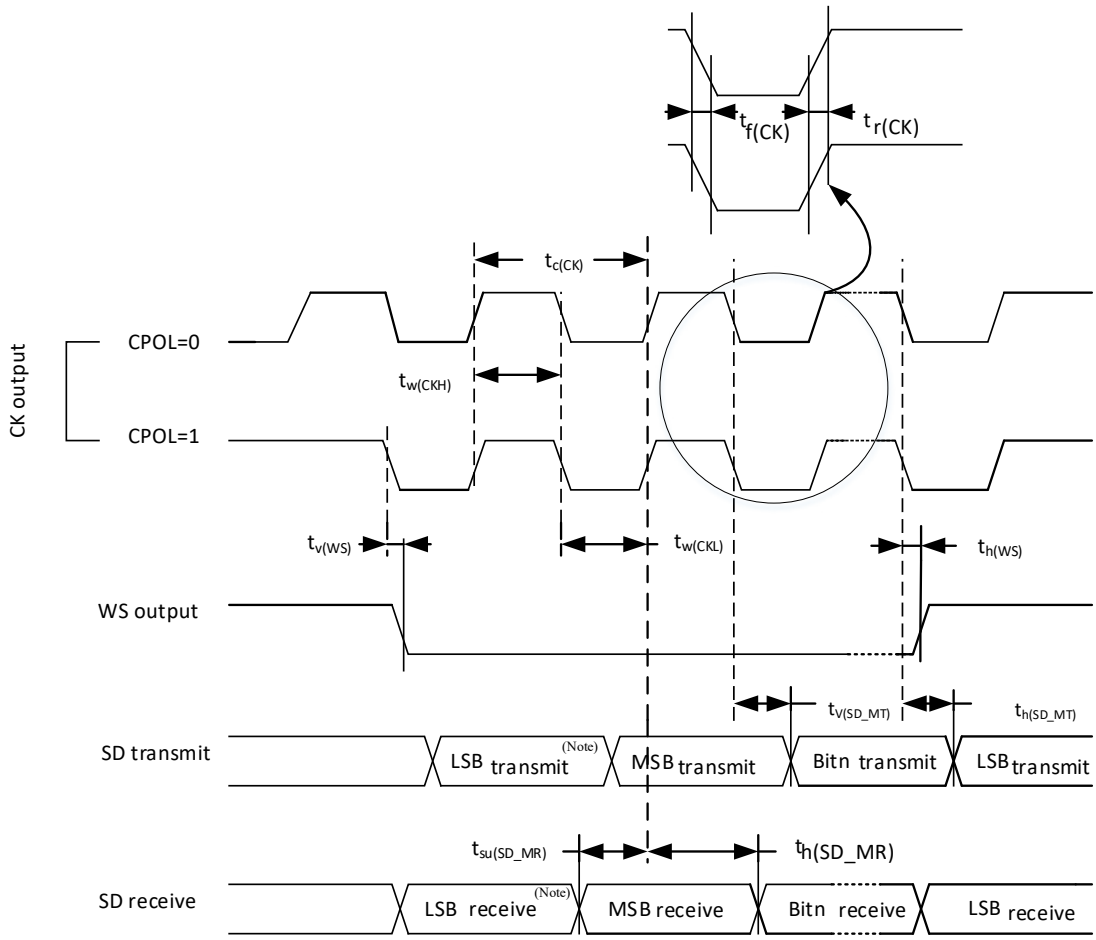
Symbol	Parameter	Conditions	Min.	Max.	Unit.
$t_{r(CK)}$ $t_{f(CK)}$	I²S Clock Rising and Falling time	Capacitive load: C = 15 pF	—	12	ns
$t_{v(WS)}$(1)	WS Valid Time	Master mode	0	4	
$t_{h(WS)}$(1)	WS Hold Time	Master mode	0	4	
$t_{su(WS)}$(1)	WS Setup Time	Slave mode	9	—	
$t_{h(WS)}$(1)	WS Hold Time	Slave mode	0	—	
$t_{su(SD\_MR)}$(1)	Data Input Setup Time	Master receiver	6	—	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	—	
$t_{h(SD\_MR)}$(1)(2)	Data Input Hold Time	Master receiver	0.5	—	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	—	
$t_{v(SD\_ST)}$(1)(2)	Data Output Valid Time	Slave transmitter (after enable edge)	—	20	
$t_{h(SD\_ST)}$(1)	Data Output Hold Time	Slave transmitter (after enable edge)	9	—	
$t_{v(SD\_MT)}$(1)(2)	Data Output Valid Time	Master transmitter (after enable edge)	—	15	
$t_{h(SD\_MT)}$(1)	Data Output Hold Time	Master transmitter (after enable edge)	0	—	

Note: 1. Guaranteed by design and/or characterization results.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = 1/f_{PCLK} =125 ns.



Note: LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 22. I²S Slave Timing Diagram (Philips Protocol)



Note: LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 23. I²S Master Timing Diagram (Philips Protocol)

I²C Characteristics

GPIO pins SDA and SCL have limitation as follows: they are not "true" open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

The I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz), and fast mode plus (max. 1 MHz).

OTGFS Characteristics

Table 38. OTGFS Startup Time

Symbol	Parameter	Max.	Unit
$t_{STARTUP}$(Note)	OTGFS Transceiver Startup Time	1	μs

Note: Guaranteed by design, not tested in production.

Table 39. OTGFS DC Electrical Characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input Levels	V_{DD}	OTGFS Operating Voltage	—	3.0(2)	—	3.6	V
	V_{DI}(3)	Differential Input Sensitivity	I (OTGFS_D+/D-)	0.2	—	—	V
	V_{CM}(3)	Differential Common Mode Range	Include V_{DI} range	0.8	—	2.5	
	V_{SE}(3)	Single Ended Receiver Threshold	—	1.3	—	2.0	
Output Levels	V_{OL}	Static Output Level Low	1.24 kΩ R_L to 3.6 V(4)	—	—	0.3	V
	V_{OH}	Static Output Level High	15 kΩ R_L to V_{SS}(4)	2.8	—	3.6	
R_{PU}		OTGFS_D+ Internal Pull-up	Idle state, $V_{IN} = V_{SS}$	0.97	1.24	1.58	kΩ
		Reception state, $V_{IN} = V_{SS}$	1.66	2.26	3.09	—	
R_{PD}		OTGFS_D+/D- Internal Pull-down	$V_{IN} = V_{DD}$	15	19	25	kΩ

Note: 1. All the voltages are measured from the local ground potential.

2. The device USB functionality is ensured down to 2.7 V but not the full USB electrical characteristics that are degraded in the 2.7 to 3.0 V V_{DD} voltage range.

3. Guaranteed by design, not tested in production.

4. R_L is the load connected on the USB drivers.

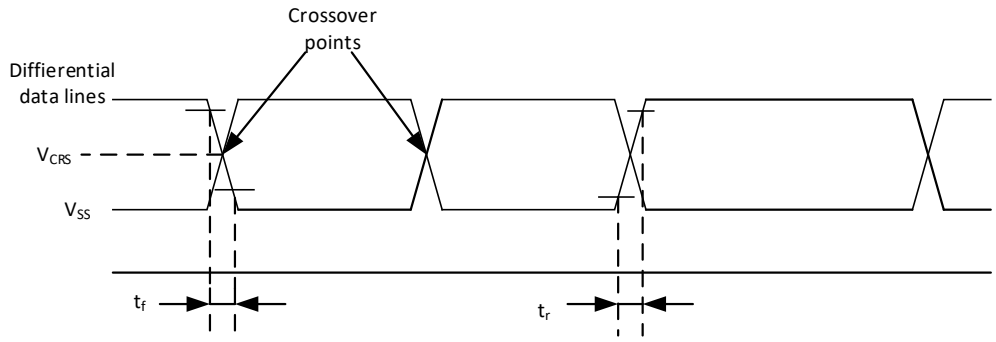


Figure 24. OTGFS Timings: Definition of Data Signal Rising and Falling time

Table 40. OTGFS Electrical Characteristics

Symbol	Parameter	Conditions	Min.(1)	Max.(1)	Unit
t_r	Rising Time (2)	$C_L \le 50$ pF	4	20	ns
t_f	Falling Time (2)	$C_L \le 50$ pF	4	20	ns
t_{rfm}	Rising/Falling Time Matching	t_r/t_f	90	110	%
V_{CRS}	Output Signal Crossover Voltage	—	1.3	2.0	V

Note: 1. Guaranteed by design, not tested in production.

2. Measured from 10% to 90% of the data signal. For more detailed information, please refer to USB Specification Chapter 7 (version 2.0).

12-bit ADC Characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in Table 7.

Note: It is recommended to perform a calibration after each power-up.

Table 41. ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DDA}	Power Supply	—	2.4	—	3.6	V
I_{DDA}	Current on the V_{DDA} Input Pin	—	—	295(1)	355	μA
f_{ADC}	ADC Clock Frequency	—	0.6	—	28	MHz
f_S(2)	Sampling Rate	—	0.05	—	2	MHz
f_{TRIG}(2)	External Trigger Frequency	f_{ADC} = 28 MHz	—	—	1.65	MHz
		—	—	—	17	$1/f_{ADC}$
V_{AIN}	Conversion Voltage Range(3)	—	0 (V_{REF-} internally connected to ground)	—	V_{REF+}	V
R_{AIN}(2)	External Input Impedance	—	See Table 39 and Table 40 for details			Ω
C_{ADC}(2)	Internal Sample and Hold Capacitor	—	—	8.5	13	pF
t_{CAL}(2)	Calibration Time	f_{ADC} = 28 MHz	6.61			μs
		—	185			$1/f_{ADC}$
t_{latr}(2)	Regular Trigger Conversion Latency	f_{ADC} = 28 MHz	—	—	71.4	ns
		—	—	—	2(4)	$1/f_{ADC}$
t_S(2)	Sampling Time	f_{ADC} = 28 MHz	0.053	—	8.55	μs
		—	1.5	—	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up Time	—	42			$1/f_{ADC}$
t_{CONV}(2)	Total Conversion Time (Including Sampling Time)	f_{ADC} = 28 MHz	0.5	—	9	μs
		—	14~252 (t_S for sampling + 12.5 for successive approximation)			$1/f_{ADC}$

Note: 1. Guaranteed by characterization results, not tested in production.

2. Guaranteed by design, not tested in production.

3. V_{REF+} can be internally connected to V_{DDA}, whereas V_{REF-} is internally connected to V_{SSA}.

4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in Table 38.

Table 39 and Table 40 are used to define the maximum external impedance allowed for an error below 1 of LSB in 12-bit resolution.

Table 42. Max. R_{AIN} when f_{ADC} = 14 MHz (1)

T_S (cycle)	t_S (μs)	Max. R_{AIN} (kΩ)
1.5	0.11	0.35
7.5	0.54	3.9
13.5	0.96	7.4
28.5	2.04	16.3
41.5	2.96	24.0
55.5	3.96	32.3
71.5	5.11	41.8
239.5	17.11	50.0

Note: Guaranteed by design.

Table 43. Max. R_{AIN} when f_{ADC} = 28 MHz (1)

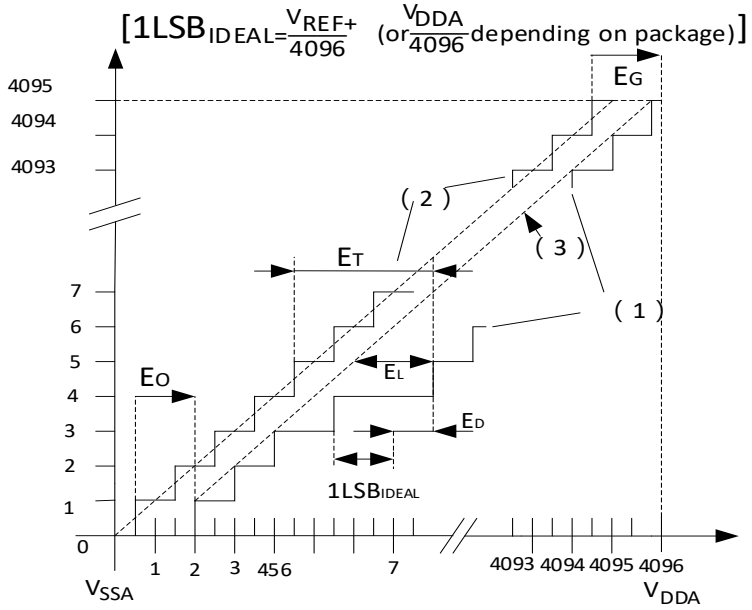
T_S (cycle)	t_S (μs)	Max. R_{AIN} (kΩ)
1.5	0.05	0.1
7.5	0.27	1.6
13.5	0.48	3.4
28.5	1.02	7.9
41.5	1.48	11.7
55.5	1.98	15.9
71.5	2.55	20.6
239.5	8.55	50.0

Note: Guaranteed by design.

Table 44. ADC Accuracy (1)(2)

Symbol	Parameter	Test Conditions	Typ	Max	Unit
E_T	Total Unadjusted Error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 3.0~3.6 V, T_A = 25 °C	±1.5	±3	LSB
E_O	Offset Error		±1	±1.5	
E_G	Gain Error		+1.5	-2/+2.5	
E_D	Differential Linearity Error		±0.7	±1	
E_L	Integral Linearity Error		±1	±1.5	
E_T	Total Unadjusted Error	f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4~3.6 V, T_A = -40 ~ 105 °C	±2	±3	LSB
E_O	Offset Error		±1.5	±3	
E_G	Gain Error		+1.5	±2.5	
E_D	Differential Linearity Error		±1	-1/+2	
E_L	Integral Linearity Error		±1.5	±2.5	

Note: 1. ADC DC accuracy values are measured after internal calibration.
2. Guaranteed by characterization results, not tested in production.



Note: 1. Example of an actual transfer curve.

2. Ideal transfer curve.

3. End point correlation line.

4. E_T = Maximum deviation between the actual and the ideal transfer curves.

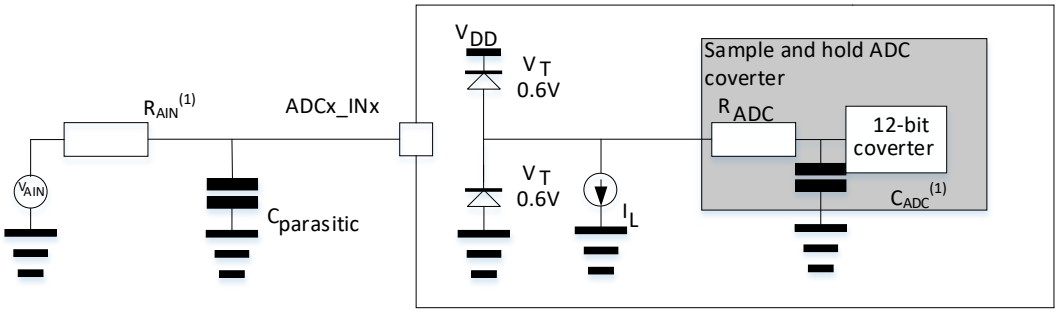
E_O = Deviation between the first actual transition and the first ideal one.

E_G = Deviation between the last ideal transition and the last actual one.

E_D = Maximum deviation between actual steps and the ideal one.

E_L = Maximum deviation between any actual transition and the end point correlation line.

Figure 25. ADC Accuracy Characteristics



Note: 1. Refer to Table 38 for the values of RAIN and CADC.

2. Cparasitic represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

Figure 26. Typical Connection Diagram Using the ADC

General PCB Design Guidelines

Power supply decoupling should be performed as shown in Figure 2. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

If HEXT is enabled while ADC uses any input channel of ADC1_IN0~13, following PCB layout guide line below to isolate the high frequency interference from HEXT emitting to ADC input signals nearby.

- Use different PCB layers to route ADC_IN signal apart from HEXT path.
- Do not route ADC_IN signals and HEXT path parallel.

Internal Reference Voltage (V_{INTRV}) Characteristics

Table 45. Internal Reference Voltage Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{INTRV}(1)	Internal Reference Voltage	—	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature Coefficient	—	—	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC Sampling Time when Reading the Internal Reference Voltage	—	5.1	—	—	μs

Note: 1. Guaranteed by characterization results, not tested in production.
2. Guaranteed by design, not tested in production.

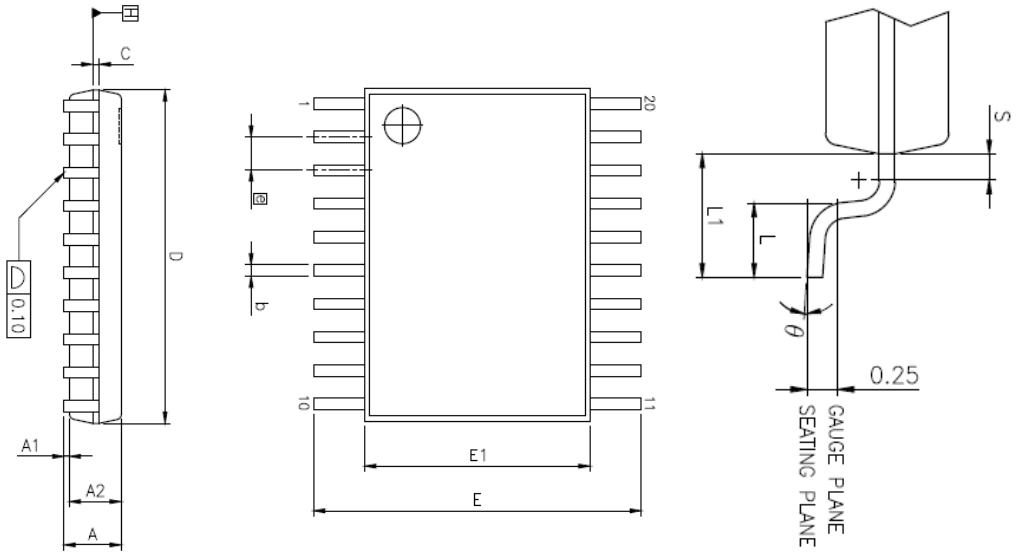
6 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website for the latest version of the Package/Carton Information.

Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

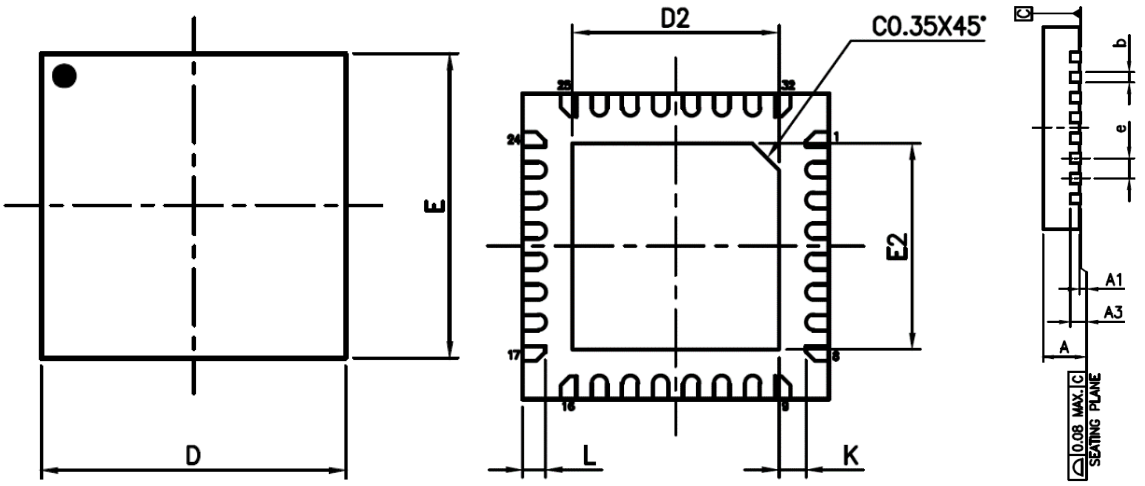
- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- The Operation Instruction of Packing Materials
- Carton information

20-pin TSSOP (6.5 mm × 4.4 mm) Outline Dimensions



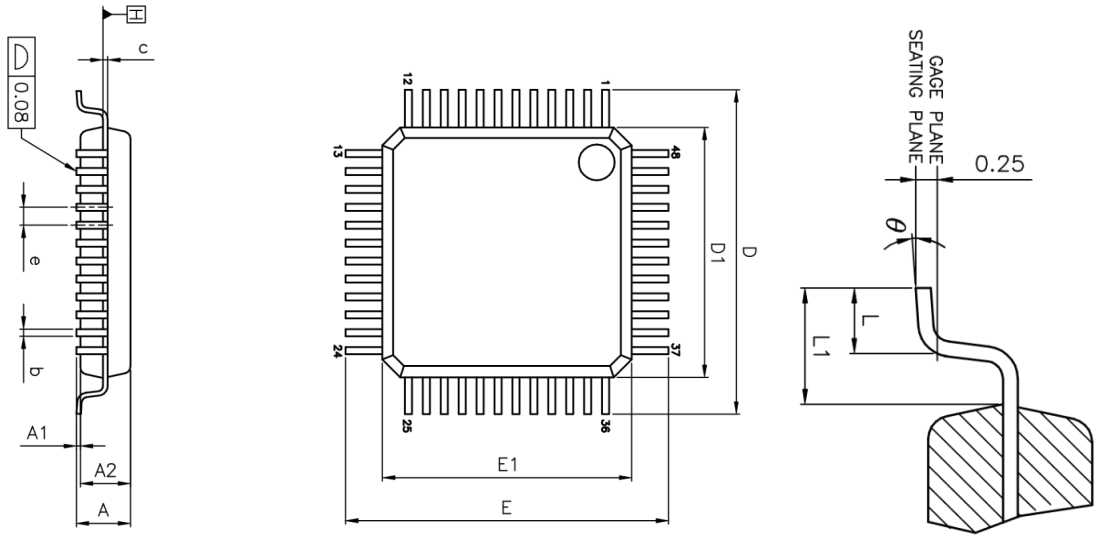
Symbol	Dimensions in mm		
	Min.	Typ.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
C	0.09	—	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC.		
L1	1.00 REF.		
L	0.50	0.60	0.75
S	0.20	—	—
Θ	0°	—	8°

32-pin QFN (4 mm × 4 mm) Outline Dimensions



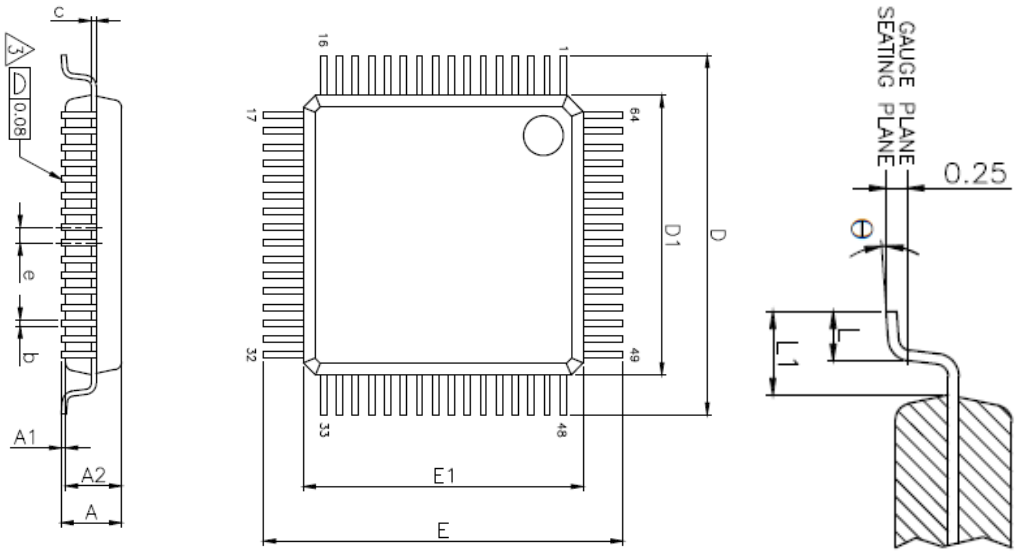
Symbol	Dimensions in mm		
	Min.	Typ.	Min.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

48-pin LQFP (7 mm × 7 mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Typ.	Min.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

64-pin LQFP (7 mm × 7 mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Typ.	Min.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

Thermal Characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6mm thickness. They are guaranteed by design, not tested in production.

Table 46. Package Thermal Characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient 64LQFP – 7 mm × 7 mm	85.1	
	Thermal Resistance Junction-Ambient 48LQFP – 7 mm × 7 mm	85.1	
	Thermal Resistance Junction-Ambient 32QFN – 4 mm × 4 mm	54.0	
	Thermal Resistance Junction-Ambient 20TSSOP – 6.5 mm × 4.4 mm	102.6	